PRELIMINARY

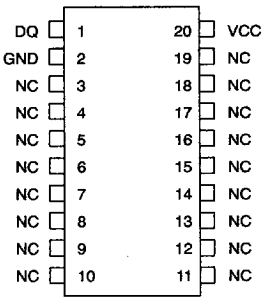
DALLAS SEMICONDUCTOR

DS2430
256–Bit Shadow RAM with 64–Bit ID

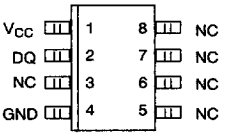
FEATURES

- 256 bits of scratchpad (SRAM) memory (one 32 byte page)
- 256 bits of non–volatile EEPROM user memory available for storage of data (one 32 byte page)
- User Determined 64–bit ID number can be made read only by a user command
- Write data transfers occur to 256 bit scratchpad so that temporary data can be stored without corrupting the contents of EEPROM
- Unlimited read and write to scratchpad
- Automatic recall from EEPROM to scratchpad during power–up routine
- Status register shows when the 64 bit ID has been locked and when scratchpad memory is being copied to non–volatile memory
- Able to be read or written at voltages from 2.7V to 5.5V
- Operating Range –40°C to +85°C
- Applications include portable computers, portable/ cellular phones, consumer electronics, handheld instrumentation, and industrial controls

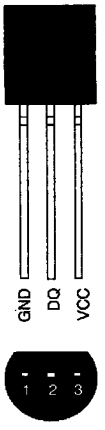
PIN ASSIGNMENT



20–PIN TSSOP
See Mech. Drawing – Pg. 969



8-PIN SOIC (150 MIL)
See Mech. Drawing – Pg. 967



TO-92 Package
See Mech. Drawing
Pg. 970

PIN DESCRIPTION

GND	– Ground
DQ	– Data In/Out
V_{CC}	– Supply
NC	– No Connect

ORDERING INFORMATION

DS2430	TO–92 Package
DS2430E	20–Pin TSSOP Package
DS2430Z	8–Pin SOIC Package

DESCRIPTION

The DS2430 combines the high performance of SRAM with the non–volatility of EEPROM. Data can be written or read from the scratchpad anytime power is applied to the device. Anytime that power is applied to V_{CC} following a power failure, the contents of the EEPROM are transferred to the scratchpad.

The DS2430 contains a 64–bit ID which can be programmed and locked by the user. Once locked, this 64–bit ID becomes read only memory.

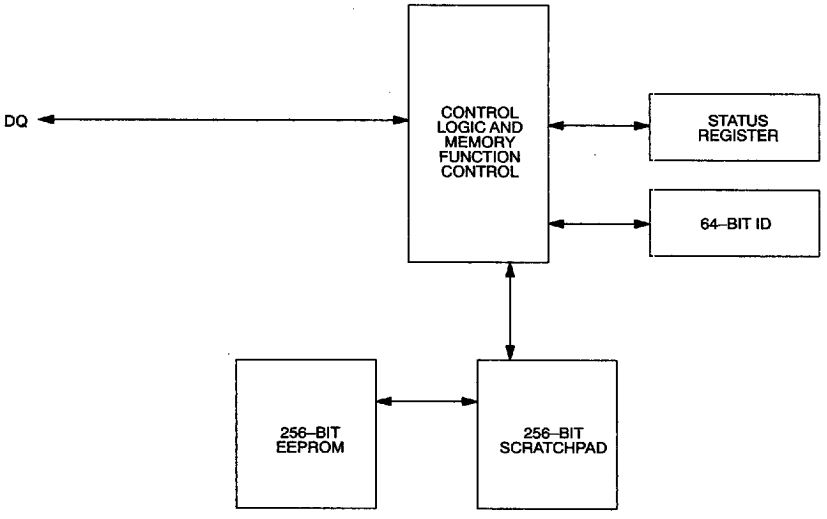
Data is sent to/from the DS2430 over a 1–wire interface, requiring only three connections: power, ground, and the data I/O pin.

OVERVIEW

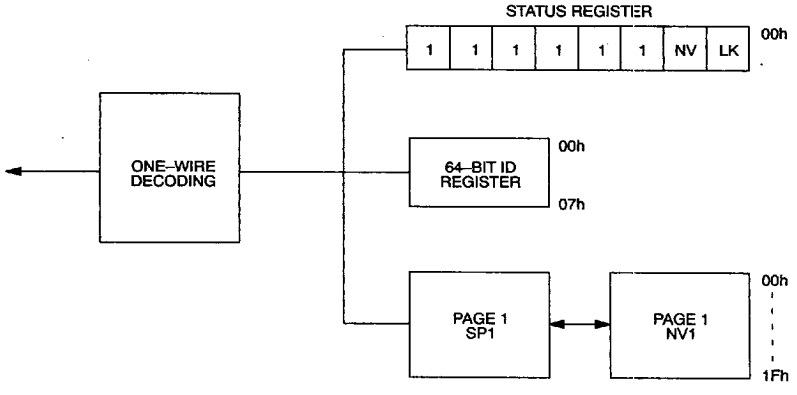
The DS2430 has four major components: 1) 256 bits of scratchpad memory, 2) 256 bits of EEPROM non–volatile memory, 3) 64–bit non–volatile ID number, and 4) a status register.

Access to the DS2430 is over a 1–wire interface and all data is read and written LSB first.

DS2430 BLOCK DIAGRAM Figure 1



DS2430 ADDRESSABLE RAM MEMORY MAP Figure 2



STATUS REGISTER (00h)

The status register contains eight bits; only the two least significant bits are used. This register is read only, and shifts out 1's for the 6 most significant bits during a read status command. A logic 1 in bit 1, the NV bit, indicates that the scratchpad page is writing to it's non–volatile counterpart. If logic 0, this bit indicates that no scratchpad to non–volatile memory transfers are occurring.

Bit 0, the LK bit, indicates with a logic 1 that the 64–bit ID has been lock protected and that the accompanying register will no longer accept writes. If this bit is logic 0, then users may modify the 64–bit ID register as they wish (note, the 64–bit ID is volatile until the Lock ID command is performed, permanently storing it in write–protected non–volatile memory).

ID REGISTERS (00h to 07h)

The ID Registers contain a 64–bit ID number that can be used as an identification code. This ID number is programmed by the user by writing the desired data into the ID's eight 8–bit registers. The ID number is volatile and may be changed indefinitely until the Lock ID command is executed. Once the Lock ID command is executed, the contents of the ID register are moved into non–volatile memory and any write to these registers is no longer accepted. **The Lock ID command can only be used once.** The ID register is accessed through the commands 41h, 42h, and 43h (see Table 1).

MEMORY (00h to 1Fh)

The DS2430 memory is configured around a paged scratchpad/EEPROM memory structure. The page is 32 bytes long, and has identical arrays of scratchpad and EEPROM non–volatile memory. The scratchpad helps insure data integrity when communicating over the 1–wire bus. Data is first written to the scratchpad where it can be read back. After the data has been verified, a copy scratchpad command will transfer the data to the EEPROM. This process insures data integrity when modifying the memory.

MEMORY FUNCTION COMMANDS

The protocols necessary for accessing the DS2430 are described in this section. These are summarized in Table 1 and a memory function example is provided in Table 2.

Read scratchpad [11h]

This command reads the contents of the scratchpad on the DS2430. This command is followed by a start byte address. After issuing this command and providing the start address, the user may begin reading the data. Addresses are internally incremented to provide continuous read capability. Upon reaching address 1Fh, the part wraps to address 00h and reading continues until another command is issued.

Write scratchpad [12h]

This command writes to the scratchpad on the DS2430. This command is followed by a start byte address. After issuing this command and providing the start address, the user may begin writing data. Addresses are internally incremented to provide continuous write capability. Upon reaching address 1Fh, the part wraps to address 00h and writing continues until another command is issued. This command should not be issued if the status register NV bit is 1.

Read Status Register [13h]

This command reads the status of the DS2430, indicating whether the 64–bit ID has been locked, and whether or not a scratchpad to non–volatile memory transfer is taking place. (See Status Register 00h above.)

Copy SP1 to NV1 [21h]

This command copies the entire contents of the scratchpad to the non–volatile EEPROM memory. While this memory transfer is taking place, the NV bit in the status register will be logic 1. This command should not be issued if the status register NV bit is 1.

Copy NV1 to SP1 [31h]

This command copies the entire contents of the non–volatile EEPROM memory into the accompanying scratchpad. The NV bit in the status register is unaffected by this transfer, remaining at logic 0. This command should not be issued if the status register NV bit is logic 1. This command should not be issued if the status register NV bit is 1.

Read ID Registers [41h]

This command reads the contents of the ID registers. This command is followed by a start address. After issuing this command and providing the start address, the user may begin reading the data. Addresses are inter-

nally incremented to provide continuous read capability. Upon reaching address 07h, the part wraps to address 00h and reading continues until another command is issued. If the Lock ID command has not yet been performed, then whatever contents were last stored in the ID registers are retrieved. If the Lock ID command has been performed, leaving the LK bit of the status register at logic 1, then the ID registers contain the locked 64–bit ID number.

Write ID Registers [42h]

This command writes information into the contents of the ID registers. This command is followed by a start address. After issuing this command and providing the start address, the user may begin writing data. Addresses a re internally incremented to provide continuous write capability. Upon reaching address 07h, the part wraps to address 00h and writing continues until another command is issued. If the Lock ID command has not yet been performed, then whatever contents are transferred with this command are written in the ID registers. If the Lock ID command has been performed, leaving the LK bit of the status register as logic 1, then this command is invalid, and any data transferred will not be written in the ID register. This command should not be issued if the status register NV bit is 1.

Lock ID [43h]

This command executes the memory transfer from the ID registers to write–protected non–volatile memory. **This command can only be executed once.** Executing it makes the contents of the ID registers the DS2430's permanent 64–bit ID number, and sets the LK bit to 1 in the status register. Since this command is a "one time only" command, it must be accompanied by a software key, A5h, to allow the command to execute. While this transfer is taking jplace, the NV bit in the status register will be logic 1. This command should not be issued if the status register NV bit is 1.

DS2430 COMMAND SET Table 1

INSTRUCTION	DESCRIPTION	PROTOCOL	1–WIRE BUS MASTER STATUS AFTER ISSUING PROTOCOL	1–WIRE BUS DATA AFTER ISSUING PROTOCOL
Read Scratchpad	Read data from scratchpad beginning at specified address.	11h + address (00h to 1Fh)	RX	<read data>
Write Scratchpad	Write data to the scratchpad beginning at specified address.	12h + address (00h to 1Fh)	TX	<write data>
Read Status Register	Reads contents of the status register.	13h + 00h	TX	<read data>
Copy SP1 to NV1	Copies entire contents of SP1 to NV1.	21h	idle	idle
Copy NV1 to SP1	Copies entire contents of NV1 to SP1.	31h	idle	idle
Read ID Register	Reads contents of ID registers beginning at specified address.	41h + address (00h to 07h)	RX	<read data>
Write ID Register	Writes data to the ID registers beginning at specified address.	42h + address (00h to 07h)	TX	<write data>
Lock ID (One Time Programmable)	Copies and write protects contents of ID registers to ID nonvolatile memory.	43h + A5h (A5 is a key and must be used)	idle	idle

MEMORY FUNCTION EXAMPLE Table 2
Bus Master writes 32 bytes of data to DS2430 scratchpad, then copies to it to NV1.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480–960 µs)
RX	Presence	Presence pulse
TX	12h	Issue "Write scratchpad" command
TX	00h	Start address
TX	<32 bytes>	Write 32 bytes of data to scratchpad
TX	Reset	Reset Pulse
RX	Presence	Presence pulse
TX	11h	Issue "Read scratchpad" command
TX	00h	Start address
RX	<32 data bytes>	Read scratchpad data and verify
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	21h	Issue "Copy SP1 to NV1" command
RX	<busy indicator>	Wait until NV in status register=0 (5–10 ms typical)
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

1–WIRE BUS SYSTEM

The DS2430 1–wire bus is a system which has a single bus master and one slave. The DS2430 behaves as a slave. The DS2430 is not able to be multidropped, unlike other 1–wire devices from Dallas Semiconductor.

The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1–wire signaling (signal types and timing).

HARDWARE CONFIGURATION

The 1–wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1–wire bus must have open drain or 3–state outputs. The 1–wire port of the DS2430 is open drain with an internal circuit equivalent to that shown in Figure 3. The 1–wire bus requires a pull–up resistor of approximately 4.7KΩ.

The idle state for the 1–wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 480 µs, the DS2430 will be reset.

TRANSACTION SEQUENCE

The protocol for accessing the DS2430 via the 1–wire port is as follows:

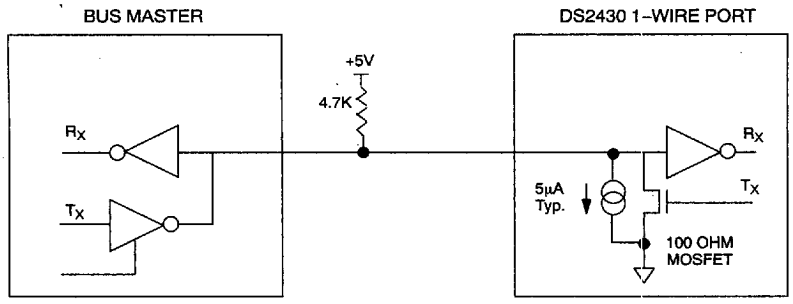
- Initialization
- Memory Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1–wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by a presence pulse transmitted by the slave.

The presence pulse lets the bus master know that the DS2430 is on the bus and is ready to operate.

HARDWARE CONFIGURATION Figure 3



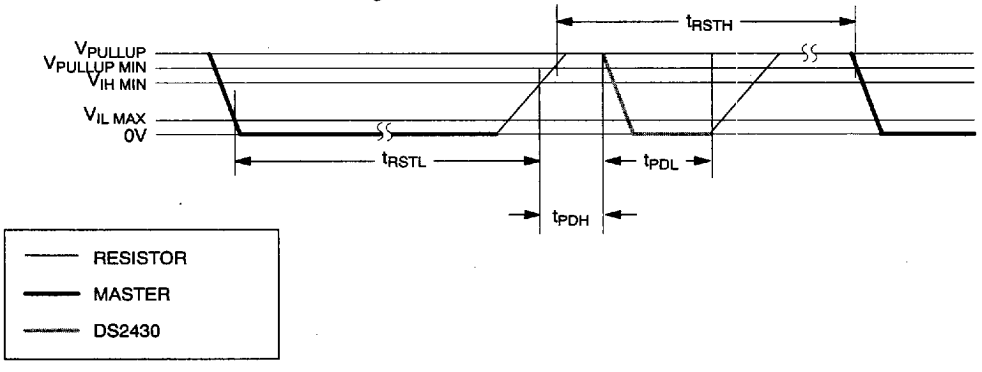
I/O SIGNALING

The DS2430 requires strict protocols to insure data integrity. The protocol consists of several types of signaling on one line: reset pulse, presence pulse, write 0, write 1, read 0, and read 1. All of these signals, with the exception of the presence pulse, are initiated by the bus master.

The initialization sequence required to begin any communication with the DS2430 is shown in Figure 4. A reset pulse followed by a presence pulse indicates the DS2430 is ready to send or receive data given the correct memory function command.

The bus master transmits (TX) a reset pulse (a low signal for a minimum of 480 µs). The bus master then releases the line and goes into a receive mode (RX). The 1–wire bus is pulled to a high state via the 4.7KΩ pull–up resistor. After detecting the rising edge on the I/O pin, the DS2430 waits 15–60 µs and then transmits the presence pulse (a low signal for 60–240 µs).

RESET AND PRESENCE PULSE Figure 4



READ/WRITE TIME SLOTS

DS2430 data is read and written through the use of time slots to manipulate bits and a command word to specify the transaction.

Write Time Slots

A write time slot is initiated when the host pulls the data line from a high logic level to a low logic level. There are two types of write time slots: Write One time slots and Write Zero time slots. All write time slots must be a minimum of 60 µs in duration with a minimum of a 1 µs recovery time between individual write cycles.

The DS2430 samples the I/O line in a window of 15 µs to 60 µs after the I/O line falls. If the line is high, a Write One occurs. If the line is low, a Write Zero occurs (see Figures 5a and 5b).

For the host to generate a Write One time slot, the data line must be pulled to a logic low level and then released, allowing the data line to pull up to a high level within 15 µs after the start of the write time slot.

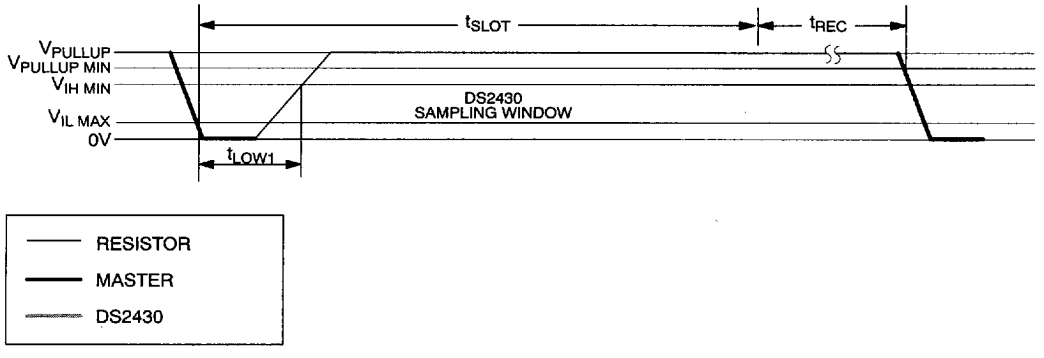
For the host to generate a Write Zero time slot, the data line must be pulled to a logic low level and remain low for the duration of the write time slot. At the end of each time slot, the DS2430 needs a recovery time, t_{REC}, at a minimum of 1 µs to prepare for the next bit.

Read Time Slots

The host generates read time slots when data is to be read from the DS2430. A read time slot is initiated when the host pulls the data line from a logic high level to logic low level. The data line must remain at a low logic level for a minimum of 1 µs; output data from the DS2430 is then valid for the next 14 µs maximum. The host therefore must stop driving the I/O pin low in order to read its state 15 µs from the start of the read slot (see Figure 6). Following t_{RDV} there is an additional time interval, $t_{RELEASE}$, after which the DS2430 releases the I/O pin so that its voltage can return to V_{PULLUP}. All read time slots must be a minimum of 60 µs in duration with a minimum of a 1 µs recovery time between individual read slots.

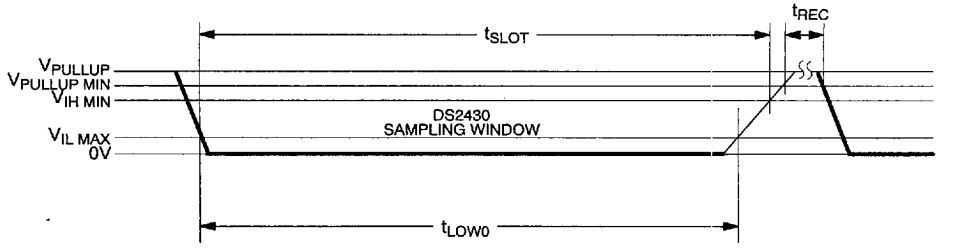
WRITE TIMING DIAGRAMS Figure 5

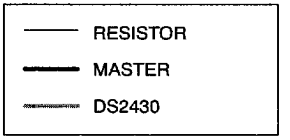
a) Write–One Time Slot



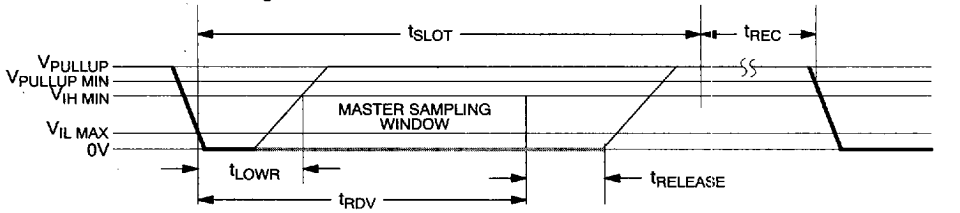
WRITE TIMING DIAGRAMS (cont'd) Figure 5

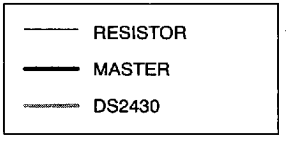
b) Write–Zero Time Slot





READ–DATA TIME SLOT Figure 6





$1\ \mu s \le t_{LOWR} < 15\ \mu s$

$0 \le t_{RELEASE} < 45\ \mu s$

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	–40°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	2.7		5.5	V	
Data Pin	DQ	–0.3		5.5	V	

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC}=2.7V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}		2.2		5.5	V	1
Logic 0	V_{IL}		–0.3		+0.8	V	1
Sink Current	I_L	$V_{I/O}$=0.4V	–4.0			mA	
Standby Current	I_Q			100	150	nA	
Active Current	I_{CC}			250	500	µA	
Input Resistance	R_I			500		KΩ	2

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance	$C_{IN/OUT}$			25	pF	

AC ELECTRICAL CHARACTERISTICS: 1–WIRE INTERFACE

(–40°C to +85°C; V_{CC}=2.7V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Recover Time	t_{REC}	1			µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Read Data Valid	t_{RDV}			15	µs	
Reset Time High	t_{RSTH}	480			µs	
Reset Time Low	t_{RSTL}	480		960	µs	
Presence Detect High	t_{PDHIGH}	15		60	µs	
Presence Detect Low	t_{PDLOW}	60		240	µs	
Release Time	$t_{RELEASE}$	0		45	µs	
Read Low Time	t_{LOWR}	1		15	µs	

NOTES:

1. All voltages are referenced to ground.
2. I/O line in high impedance state and $I_{I/O}$=0.