

HM53462 Series

65,536-Word x 4-Bit Multiport CMOS Video RAM (with Logic Operation Mode)

■ DESCRIPTION

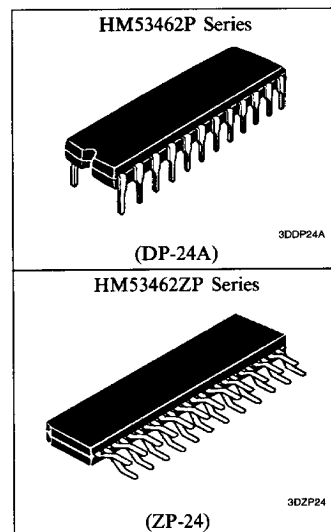
The HM53462 is a 262,144-bit multiport memory equipped with a 64k-word x 4-bit Dynamic RAM port and a 256-word x 4-bit Serial Access Memory (SAM) port. The SAM port is connected to an internal 1,024-bit data register through a 256-word x 4-bit serial read or write access control. In the read transfer cycle, the memory cell data is transferred from a selected word line of the RAM port to the data register. The RAM port has a write mask capability in addition to the conventional operation mode. Write bit selection out of 4 data bit can be achieved. RAM port has another new function, logic operation capability. By this function logic operation between memory data and input data can be done in one cycle. Utilizing the Hitachi 2 μ m CMOS process, fast serial access operation and low power dissipation are realized. All inputs and outputs, including clocks, are TTL compatible.

■ FEATURES

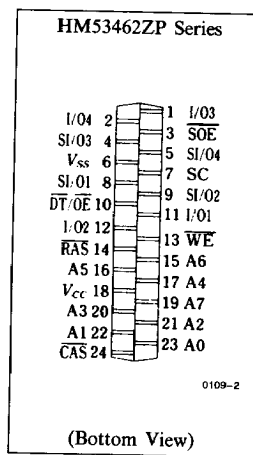
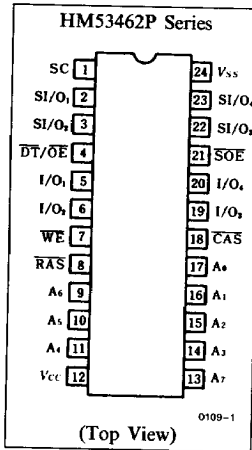
- Multiport Organization
(RAM; 64k-word x 4-bit and SAM; 256-word x 4-bit)
- Double Layer Polysilicon/Polycide N-Well CMOS Process
- Single 5V ($\pm 10\%$)
- Low Power
 - Active RAM 380 mW (max)
 - SAM 220 mW (max)
 - Standby 40 mW (max)
- Access Time
 - RAM 100 ns/120 ns/150 ns
 - SAM 40 ns/40 ns/60 ns
- Cycle Time
 - Random Read or Write Cycle Time (RAM) 190 ns/220 ns/260 ns
 - Serial Read or Write Cycle Time (SAM) 40 ns/40 ns/60 ns
- TTL Compatible
- 256 Refresh Cycles 4 ms
- Refresh Function
 - RAS Only Refresh
 - CAS Before RAS Refresh
 - Hidden Refresh
- Bidirectional Data Transfer Operation (RAM $\longleftrightarrow$ SAM)
- Fast Serial Access Operation Asynchronized with RAM Port except Data Transfer Cycle
- Real Time Read Transfer Capability
- Write Mask Mode Capability
- Logic Operation Capability between D_{in} and D_{out}
- SAM Organization Can Be Changed to 1024 x 1

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM53462P-10	100 ns	400 mil 24-pin
HM53462P-12	120 ns	Plastic DIP
HM53462P-15	150 ns	(DP-24A)
HM53462ZP-10	100 ns	24-pin
HM53462ZP-12	120 ns	Plastic DIP
HM53462ZP-15	150 ns	(ZP-24)



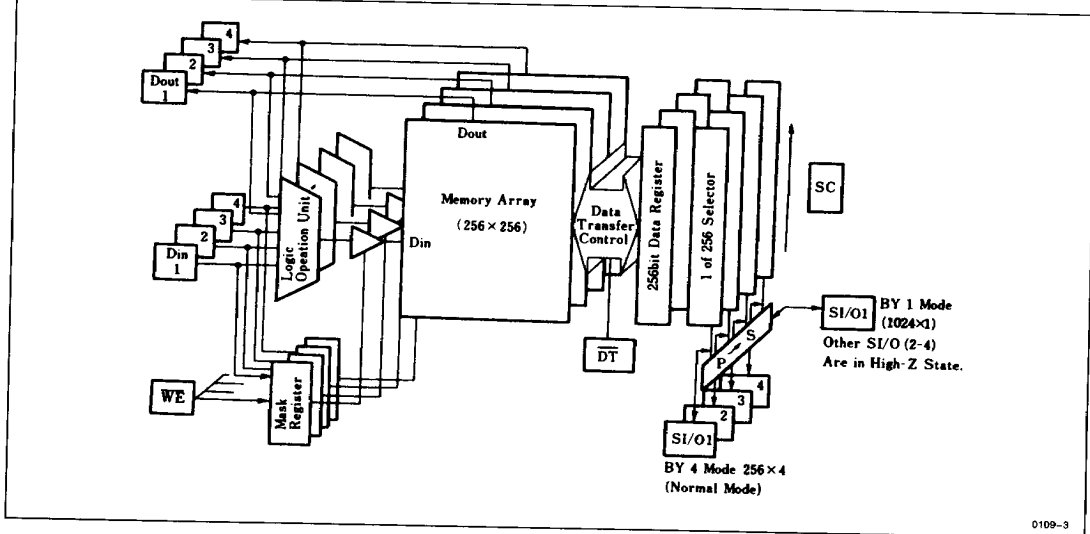
■ PIN OUT



■ PIN DESCRIPTION

Pin Name	Function
A ₀ -A ₇	Address Input
I/O ₁ -I/O ₄	RAM Port Data Input/Output
SI/O ₁ -SI/O ₄	SAM Port Data Input/Output
RAS	Row Address Strobe
CAS	Column Address Strobe
SC	Serial Clock
WE	Write Enable
DT/OE	Data Transfer/Output Enable
SOE	SAM Port Enable
V _{CC}	Power Supply
V _{SS}	Ground

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-1.0 to +7.0	V
Power Supply Voltage Relative to V_{SS}	V_{CC}	-0.5 to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W

■ INPUT/OUTPUT CAPACITANCE

Parameter	Symbol	Typ	Max	Unit	Note
Address	C_{I1}	—	5	pF	
Clocks	C_{I2}	—	5	pF	
I/O, SI/O	$C_{I/O}$	—	7	pF	

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions ($T_A = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.4	—	6.5	V	
Input Low Voltage	V_{IL}	-0.5	—	0.8	V	2

Notes: 1. All voltages referenced to V_{SS} .
 2. -3.0V for pulse width ≤ 10 ns.

• DC Electrical Characteristics ($T_A = 0$ to +70°C, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$)

RAM Port	Symbol	SAM Port		HM53462 -10	HM53462 -12	HM53462 -15	Unit	Note
		Standby	Active					
Operating Current $\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = \min$	I_{CC1}	—	×	70	60	50	mA	
	I_{CC7}	×	—	110	100	80	mA	
Standby Current $\overline{RAS}$, $\overline{CAS} = V_{IH}$	I_{CC2}	—	×	7	7	7	mA	
	I_{CC8}	×	—	40	40	30	mA	
RAS Only Refresh Current $CAS = V_{IH}$, $\overline{RAS}$ Cycling $t_{RC} = \min$	I_{CC3}	—	×	60	50	40	mA	
	I_{CC9}	×	—	100	90	70	mA	
Page Mode Current $\overline{RAS} = V_{IL}$, CAS Cycling $t_{pC} = \min$	I_{CC4}	—	×	50	40	35	mA	
	I_{CC10}	×	—	90	80	65	mA	
CBR Refresh Current $\overline{RAS}$ Cycling $t_{RC} = \min$	I_{CC5}	—	X	60	50	40	mA	
	I_{CC11}	×	—	100	90	70	mA	
Data Transfer Current $\overline{RAS}$, CAS Cycling $t_{RC} = \min$	I_{CC6}	—	×	75	65	55	mA	
	I_{CC12}	×	—	115	105	85	mA	

Parameter	Symbol	Min	Max	Unit	Note
Input Leakage	I_{LI}	-10	10	μA	
Output Leakage	I_{LO}	-10	10	μA	
Output High Voltage $I_{OH} = -2$ mA	V_{OH}	2.4	—	V	
Output Low Voltage $I_{OL} = 4.2$ mA	V_{OL}	—	0.4	V	



• Electrical Characteristics and Recommended AC Operating Conditions

(T_A = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)^{1, 10, 11}

Parameter	Symbol	HM53462-10		HM53462-12		HM53462-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t _{RC}	190	—	220	—	260	—	ns	
Read-Modify-Write Cycle Time	t _{RWC}	260	—	300	—	355	—	ns	
Page Mode Cycle Time	t _{PC}	70	—	85	—	105	—	ns	
Access Time from RAS	t _{RAC}	—	100	—	120	—	150	ns	2, 3
Access Time from CAS	t _{CAC}	—	50	—	60	—	75	ns	3, 4
Output Buffer Turn-off Delay Referenced to CAS	t _{OFF1}	0	25	0	30	0	40	ns	5
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	ns	6
RAS Precharge Time	t _{RP}	80	—	90	—	100	—	ns	
RAS Pulse Width	t _{RAS}	100	10000	120	10000	150	10000	ns	
CAS Pulse Width	t _{CAS}	50	10000	60	10000	75	10000	ns	
RAS to CAS Delay Time	t _{RCD}	25	50	25	60	30	75	ns	7
RAS Hold Time	t _{RSH}	50	—	60	—	75	—	ns	
CAS Hold Time	t _{CSH}	100	—	120	—	150	—	ns	
CAS to RAS Precharge Time	t _{CRP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t _{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	15	—	15	—	20	—	ns	
Column Address Setup Time	t _{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t _{CAH}	20	—	20	—	25	—	ns	
Write Command Setup Time	t _{WCS}	0	—	0	—	0	—	ns	8
Write Command Hold Time	t _{WCH}	25	—	25	—	30	—	ns	
Write Command Pulse Width	t _{WP}	15	—	20	—	25	—	ns	
Write Command to RAS Lead Time	t _{RWL}	35	—	40	—	45	—	ns	
Write Command to CAS Lead Time	t _{CWL}	35	—	40	—	45	—	ns	
Data-in Setup Time	t _{DS}	0	—	0	—	0	—	ns	9
Data-in Hold Time	t _{DH}	25	—	25	—	30	—	ns	8, 9
Read Command Setup Time	t _{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t _{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to RAS	t _{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t _{REF}	—	4	—	4	—	4	ms	
RAS Pulse Width (Read-Modify-Write Cycle)	t _{RWS}	170	10000	200	10000	245	10000	ns	
CAS to WE Delay	t _{CWD}	85	—	100	—	125	—	ns	8
CAS Setup Time (CAS Before RAS Refresh)	t _{CSR}	10	—	10	—	10	—	ns	
CAS Hold Time (CAS Before RAS Refresh)	t _{CHR}	20	—	25	—	30	—	ns	
RAS Precharge to CAS Hold Time	t _{RPC}	10	—	10	—	10	—	ns	
CAS Precharge Time	t _{CP}	10	—	15	—	20	—	ns	
Access Time from OE	t _{OAC}	—	30	—	35	—	40	ns	
Output Buffer Turn-off Delay Referenced to OE	t _{OFF2}	0	25	0	30	0	40	ns	
OE to Data-in Delay Time	t _{ODD}	25	—	30	—	40	—	ns	
OE Hold Time Referenced to WE	t _{OEH}	10	—	15	—	20	—	ns	



HM53462 Series

• Electrical Characteristics and Recommended AC Operating Conditions (continued)

(T_A = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)^{1, 10, 11}

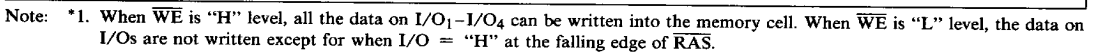
Parameter	Symbol	HM53462-10		HM53462-12		HM53462-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Data-in to CAS Delay Time	t _{DZC}	0	—	0	—	0	—	ns	
Data-in to OE Delay Time	t _{DZO}	0	—	0	—	0	—	ns	
OE to RAS Delay Time	t _{ORD}	35	—	40	—	45	—	ns	
Serial Clock Cycle Time	t _{SCC}	40	—	40	—	60	—	ns	
Access Time from SC	t _{SCA}	—	40	—	40	—	60	ns	10
Access Time from SOE	t _{SEA}	—	25	—	30	—	40	ns	10
SC Pulse Width	t _{SC}	10	—	10	—	10	—	ns	
SC Precharge Width	t _{SCP}	10	—	10	—	10	—	ns	
Serial Data-out Hold Time after SC High	t _{SOH}	10	—	10	—	10	—	ns	
Serial Output Buffer Turn-off Delay from SOE	t _{SEZ}	0	25	0	25	0	30	ns	
Serial Data-in Setup Time	t _{SIS}	0	—	0	—	0	—	ns	
Serial Data-in Hold Time	t _{SIH}	15	—	20	—	25	—	ns	
DT to RAS Setup Time	t _{DTS}	0	—	0	—	0	—	ns	
DT to RAS Hold Time (Read Transfer Cycle)	t _{RDH}	80	—	90	—	110	—	ns	
DT to RAS Hold Time	t _{DTH}	15	—	15	—	20	—	ns	
DT to CAS Hold Time	t _{CDH}	20	—	30	—	45	—	ns	
Last SC to DT Delay Time	t _{SDD}	5	—	5	—	10	—	ns	
First SC to DT Hold Time	t _{SDH}	25	—	25	—	30	—	ns	
DT to RAS Delay Time	t _{DTR}	10	—	10	—	10	—	ns	
WE to RAS Setup Time	t _{WS}	0	—	0	—	0	—	ns	
WE to RAS Hold Time	t _{WH}	15	—	15	—	20	—	ns	
I/O to RAS Setup Time	t _{MS}	0	—	0	—	0	—	ns	
I/O to RAS Hold Time	t _{MH}	15	—	15	—	20	—	ns	
Serial Output Buffer Turn-off Delay from RAS	t _{SRZ}	10	50	10	60	10	75	ns	
SC to RAS Setup Time	t _{SRS}	30	—	40	—	45	—	ns	
RAS to SC Delay Time	t _{SRD}	25	—	30	—	35	—	ns	
Serial Data Input Delay Time from RAS	t _{SID}	50	—	60	—	75	—	ns	
Serial Data Input to DT Delay Time	t _{SZD}	0	—	0	—	0	—	ns	
SOE to RAS Setup Time	t _{ES}	0	—	0	—	0	—	ns	
SOE to RAS Hold Time	t _{EH}	15	—	15	—	20	—	ns	
Serial Write Enable Setup Time	t _{SWS}	0	—	0	—	0	—	ns	
Serial Write Enable Hold Time	t _{SWH}	35	—	35	—	55	—	ns	
Serial Write Disable Setup Time	t _{SWIS}	0	—	0	—	0	—	ns	
Serial Write Disable Hold Time	t _{SWIH}	35	—	35	—	55	—	ns	
DT to Sout in Low-Z Delay Time	t _{DLZ}	5	—	10	—	10	—	ns	



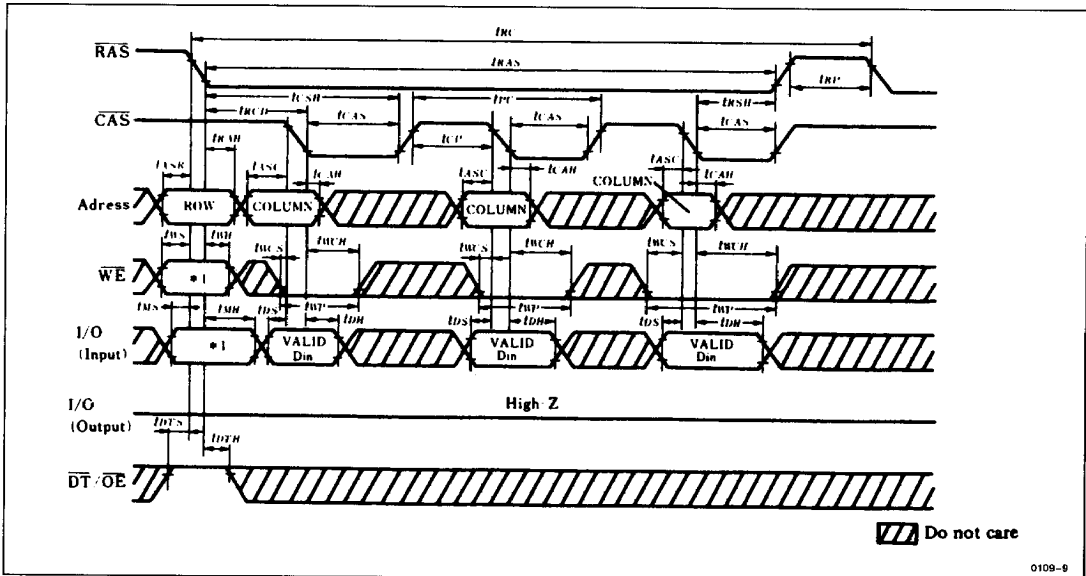


- **Delayed Write Cycle**





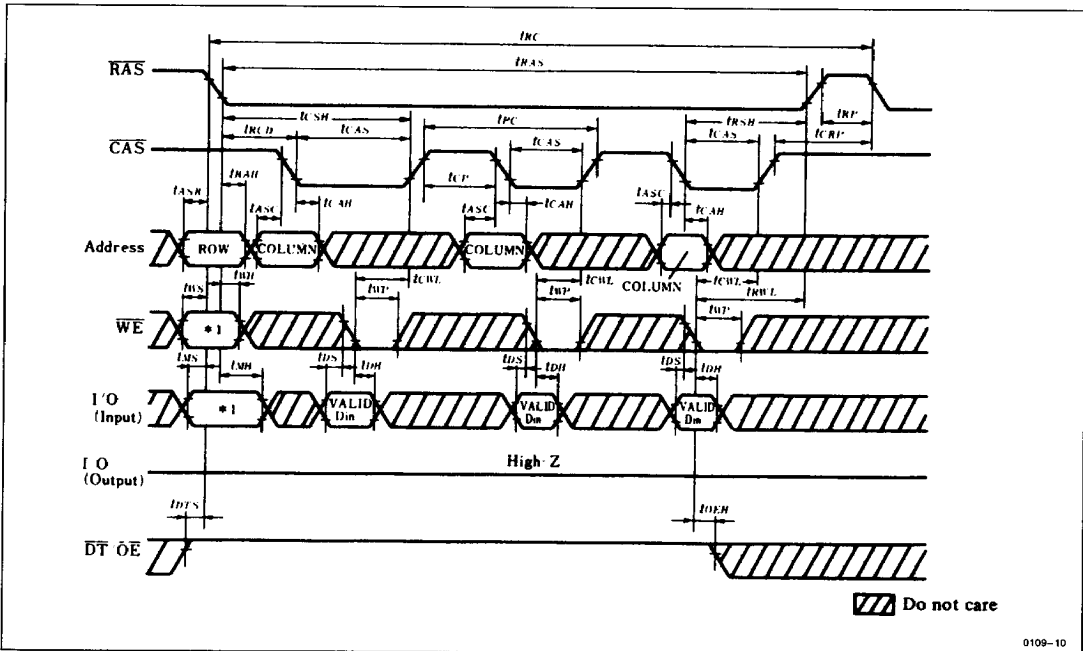
• Page Mode Write Cycle (Early Write)



0109-9

Note: *1. When $\overline{WE}$ is "H" level, all the data on I/O₁–I/O₄ can be written into the memory cell. When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of RAS.

• Page Mode Write Cycle (Delayed Write)

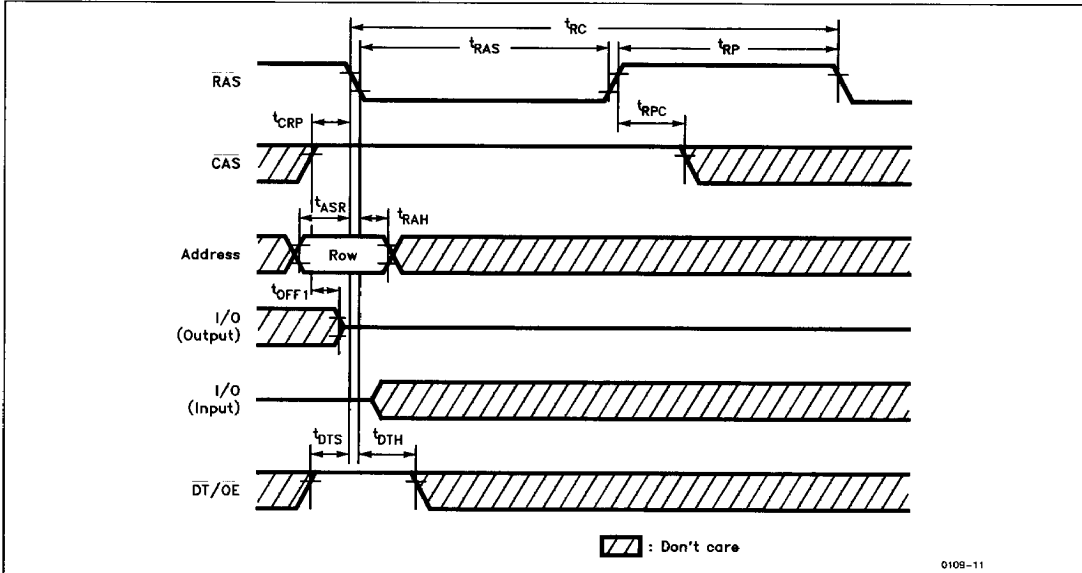


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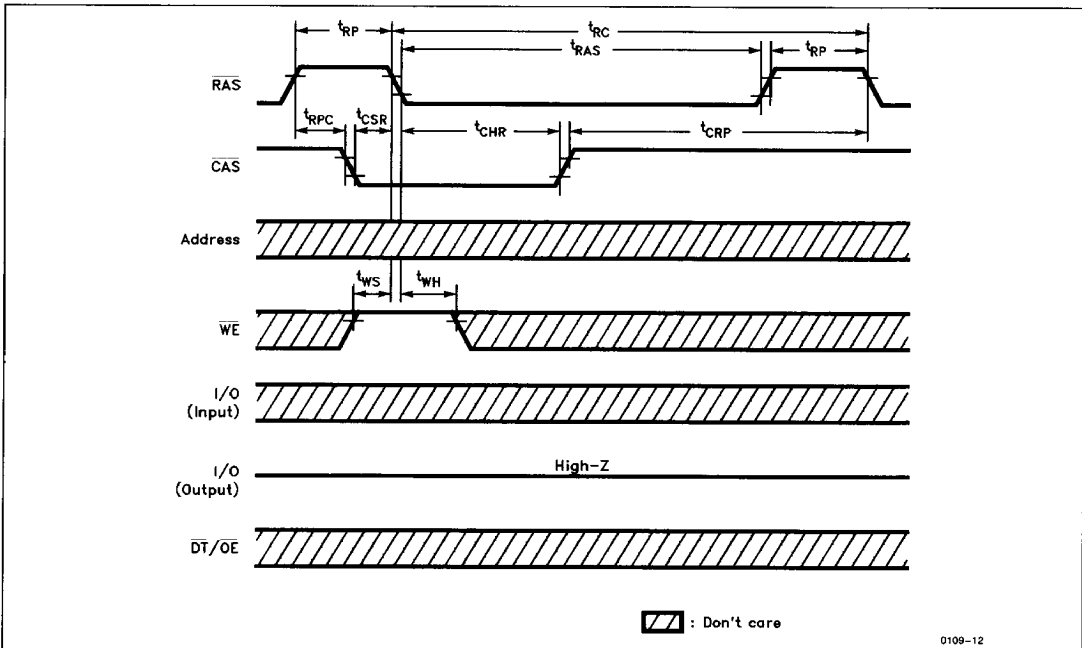
Note: *1. When $\overline{WE}$ is "H" level, all the data on I/O₁–I/O₄ can be written into the memory cell. When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of RAS.



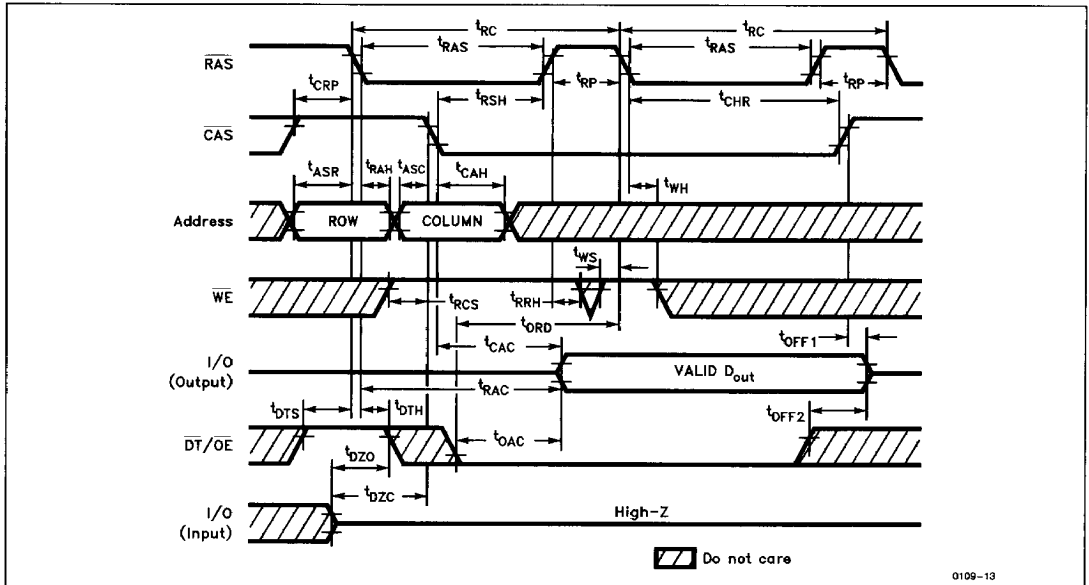
• **RAS Only Refresh Cycle**



• **CAS Before RAS Refresh Cycle**

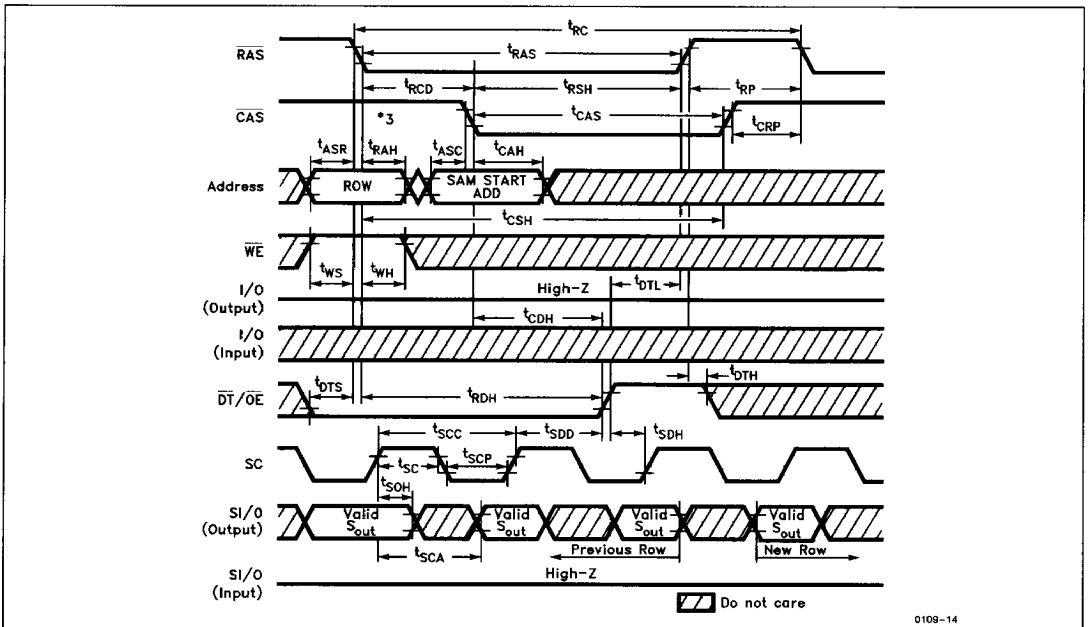


• Hidden Refresh Cycle



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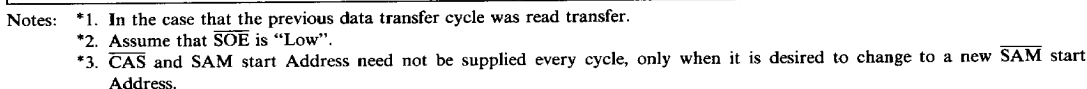
• Read Transfer Cycle (1)*1, *2



0109-14

Notes: *1. In the case that the previous data transfer cycle was read transfer.

*2. Assume that $\overline{SOE}$ is "Low".*3. $\overline{CAS}$ and SAM start Address need not be supplied every cycle, only when it is desired to change to a new SAM start Address.

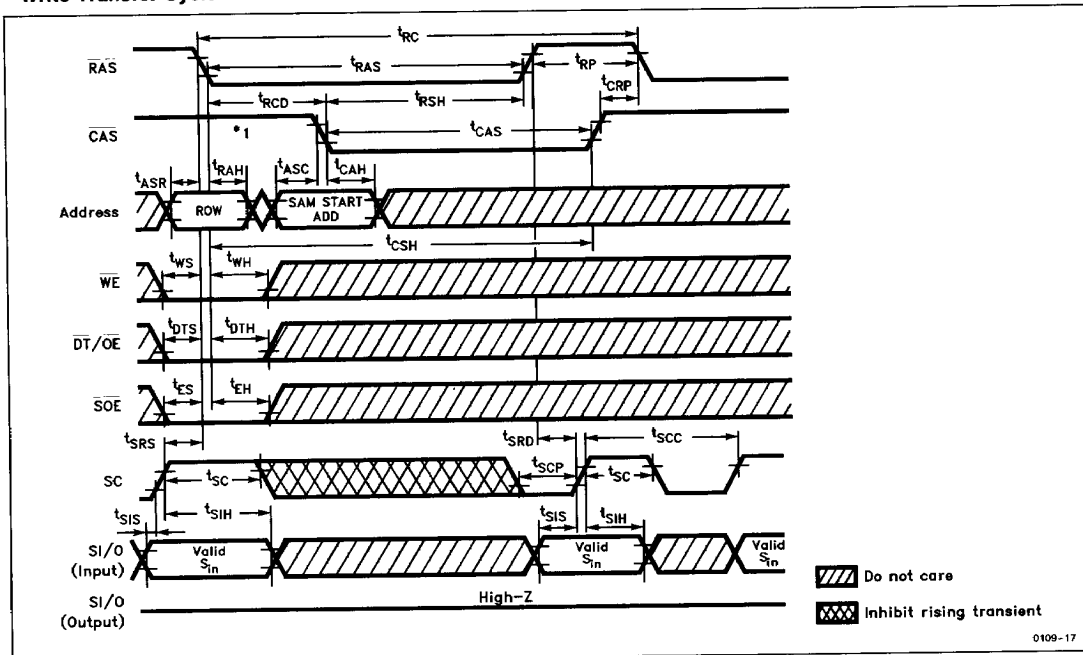


Timing diagram for the 6264 16K1T1 DRAM. The diagram shows the relationship between RAS, CAS, Address, WE, DT/OE, SOE, SC, and SI/O signals. Key timing parameters are labeled: t_{RC} , t_{RAS} , t_{RP} , t_{RCD} , t_{RSH} , t_{CAS} , t_{CRP} , t_{ASR} , t_{RAH} , t_{ASC} , t_{CAH} , t_{CSH} , t_{WS} , t_{WH} , t_{DS} , t_{DTH} , t_{ES} , t_{EH} , t_{SC} , t_{SCP} , t_{SC} , t_{SRS} , t_{SID} , t_{SRZ} , t_{SIS} , t_{SIH} , t_{SCA} , t_{SOH} , and t_{SRD} . The diagram also indicates "Do not care" regions with diagonal hatching and "Inhibit rising transient" regions with cross-hatching. A "VALID S_{in} " period is shown for the data input/output.

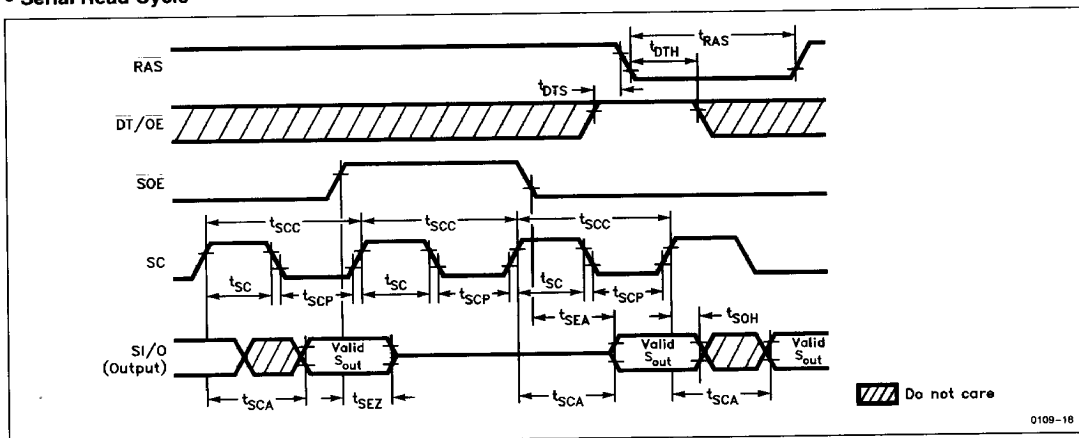


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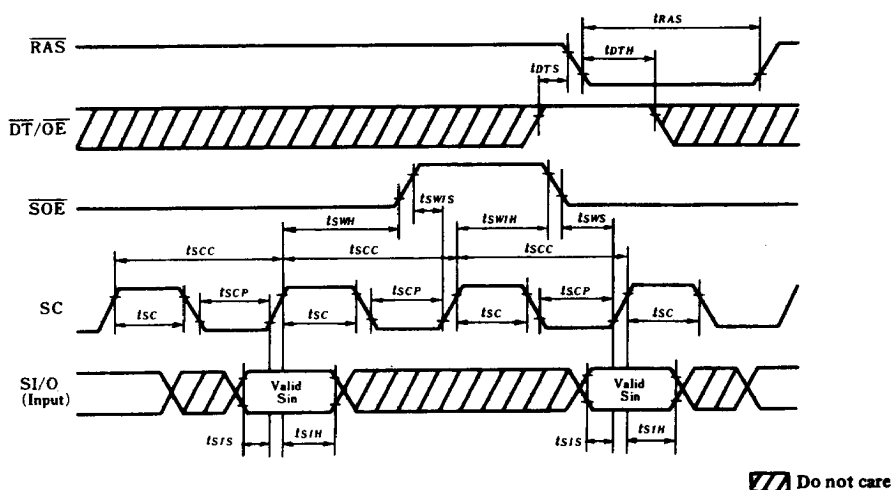
• Write Transfer Cycle



• Serial Read Cycle



• Serial Write Cycle



0109-19

• Electrical AC Characteristics (Logic Operation Mode)

Parameter	Symbol	HM53462-10		HM53462-12		HM53462-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{FRC}	230	—	265	—	310	—	ns	
RAS Pulse Width in Write Cycle	t_{RFS}	140	10000	165	10000	200	10000	ns	
CAS Pulse Width in Write Cycle	t_{CFS}	80	10000	95	10000	105	10000	ns	
CAS Hold Time in Write Cycle	t_{FCSH}	140	—	165	—	200	—	ns	
RAS Hold Time in Write Cycle	t_{FRSH}	80	—	95	—	105	—	ns	
Page Mode Cycle Time (Write Cycle)	t_{FPC}	100	—	120	—	135	—	ns	
CAS Hold Time (Logic Operation Set/Reset Cycle)	t_{FCHR}	90	—	100	—	120	—	ns	
CAS Hold Time from RAS Precharge (x4 → x1 Set Cycle)	t_{PSCH}	10	—	10	—	10	—	ns	



• Logic Code (FC0-3 are AX0-AX3 in Logic Operation Set Cycle)

FC3	FC2	FC1	FC0	LOGIC	
				Symbol	Write Data
0	0	0	0	0	Zero
0	0	0	1	AND1	$Di \cdot Mi$
0	0	1	0	AND2	$\overline{Di} \cdot Mi$
0	0	1	1	X4 → X1	—
0	1	0	0	AND3	$Di \cdot \overline{Mi}$
0	1	0	1	THROUGH	Di
0	1	1	0	EOR	$\overline{Di} \cdot Mi + Di \cdot \overline{Mi}$
0	1	1	1	OR1	$Di + Mi$
1	0	0	0	NOR	$\overline{Di} \cdot \overline{Mi}$
1	0	0	1	ENOR	$Di \cdot Mi + \overline{Di} \cdot \overline{Mi}$
1	0	1	0	INV1	$\overline{Di}$
1	0	1	1	OR2	$\overline{Di} + Mi$
1	1	0	0	INV2	$\overline{Mi}$
1	1	0	1	OR3	$Di + \overline{Mi}$
1	1	1	0	NAND	$\overline{Di} + \overline{Mi}$
1	1	1	1	1	ONE

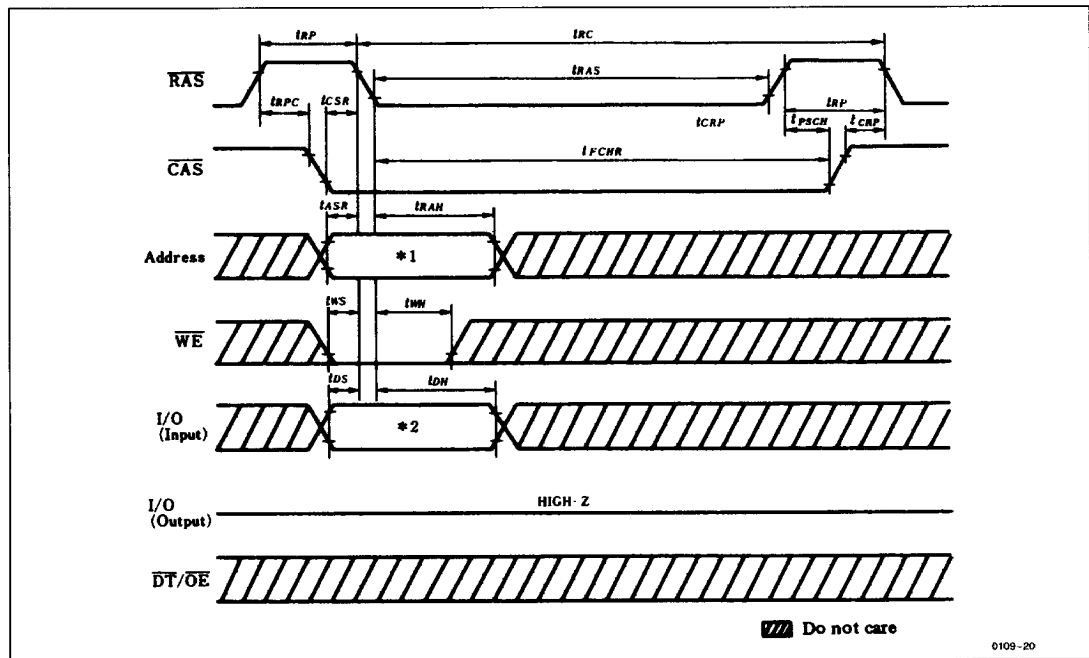
→ SAM Organization Changes to 1024 x 1

→ Logic Operation Mode Reset

Di :External Data-in

Mi :The Data of the Memory Cell

• Logic Operation Set Reset Cycle (With $\overline{CAS}$ Before $\overline{RAS}$ Refresh)



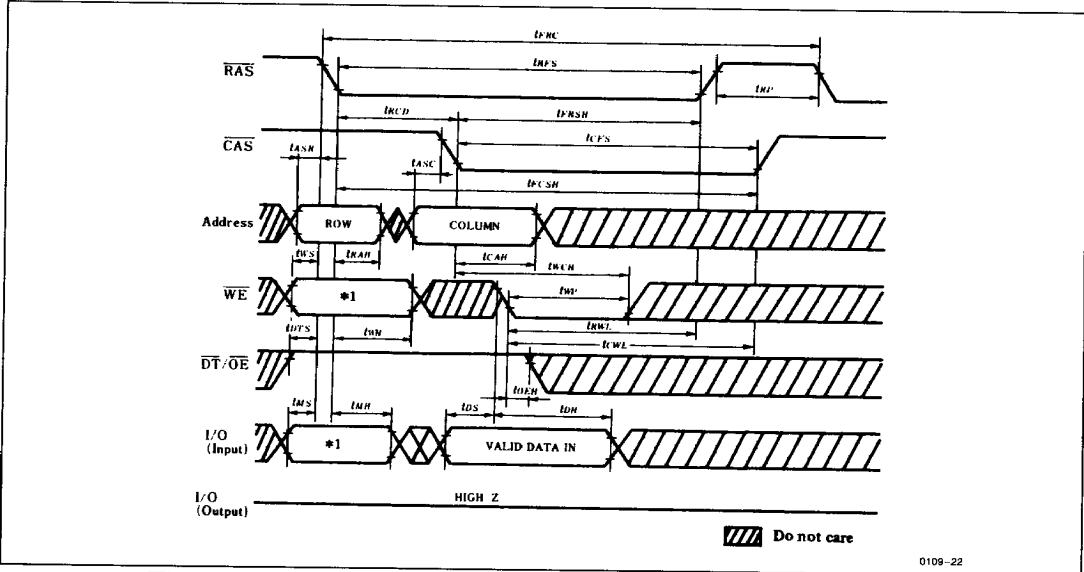
Notes: *1. Logic code A₀-A₃ (A₄-A₇: don't care)

*2. Write mask data.



[illegible]

- **Delayed Write Cycle**



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- **Page Mode Write Cycle (Early Write)**



DESCRIPTION

1. LOGIC OPERATION MODE

HM53462 has an internal logic operation unit which makes a process of graphics simple. The logic is determined in "Logic operation set/reset cycle", and the operation is executed in every write cycle succeeding to the logic operation set/reset cycle. In this mode the internal read-modify-write operation is executed and the cell data is converted into the new data given by the logic operation between D_{in} and the old cell data.

2. LOGIC OPERATION SET/RESET CYCLE

A logic operation set/reset cycle is performed by bringing $\overline{CAS}$ and $\overline{WE}$ low when $\overline{RAS}$ falls (Fig. 1). The logic code and the bits to be masked are determined respectively by $AX0-3$ state and I/O_{1-4} state at the falling edge of $\overline{RAS}$. Furthermore, in this cycle $\overline{CAS}$ before $\overline{RAS}$ refresh operation is executed, too. In this case of executing the conventional $\overline{CAS}$ before $\overline{RAS}$ refresh operation, $\overline{WE}$ must be high when $\overline{RAS}$ falls.

2.1 Logic Code

The logic code is shown in Table 1. When power is turned on, at least one logic reset cycle including write mask reset is required to initialize logic code. If the logic code is $(AX3, AX2, AX1, AX0) = (0, 0, 1, 1)$, the SAM organization is changed converter (Fig. 2). In the case that the SAM organization is changed to 1024×1 , one data transfer cycle is needed to initialize the SAM selector.

One the SAM organization is changed to 1024×1 , this code is maintained unless power is turned off.

2.2 Write Mask

HM53462 has two kinds of mask registers (register 1, 2). The register 1 is set by bringing $\overline{WE}$ low at the falling edge of $\overline{RAS}$ during the write cycle, and the mask data is available only in this cycle. The register 2 is set by level of I/O in the logic operation set/reset cycle, and the mask data is available until the next logic operation set/reset cycle. If the register 1 is set during the current logic operation mode, the mask data of the register 1 is preferred (that of the register 2 is ignored) and the logic becomes "THROUGH" only in this cycle (Fig. 3).

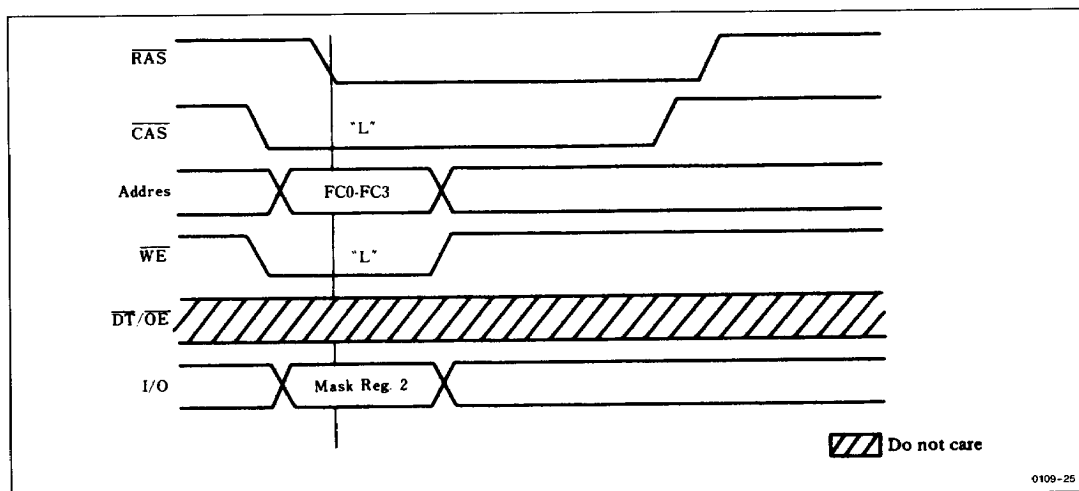


Figure 1. Logic Operation Set/Reset Cycle



• Table 1. Logic Code (FC0–FC3 are AX0–AX3 in Logic Operation Set Cycle)

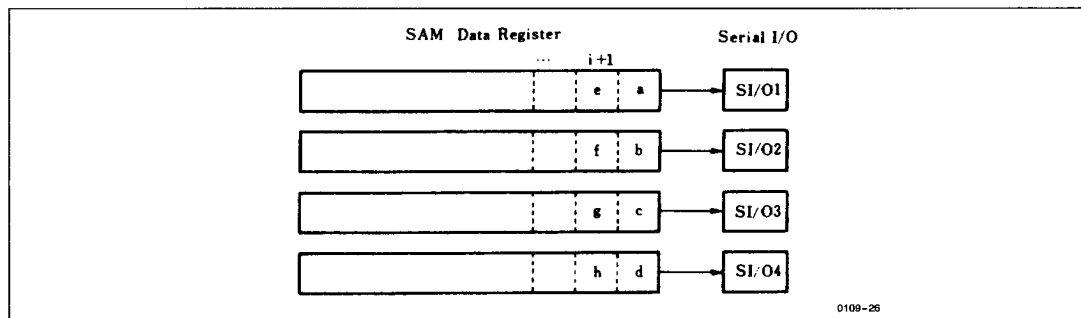
FC3	FC2	FC1	FC0	LOGIC	
				Symbol	Write Data
0	0	0	0	0	Zero
0	0	0	1	AND1	$Di \cdot Mi$
0	0	1	0	AND2	$\overline{Di} \cdot Mi$
0	0	1	1	$X4 \rightarrow X1$	—
0	1	0	0	AND3	$Di \cdot \overline{Mi}$
0	1	0	1	THROUGH	Di
0	1	1	0	EOR	$\overline{Di} \cdot Mi + Di \cdot \overline{Mi}$
0	1	1	1	OR1	$Di + Mi$
1	0	0	0	NOR	$\overline{Di} \cdot \overline{Mi}$
1	0	0	1	ENOR	$Di \cdot Mi + \overline{Di} \cdot \overline{Mi}$
1	0	1	0	INV1	$\overline{Di}$
1	0	1	1	OR2	$\overline{Di} + Mi$
1	1	0	0	INV2	$\overline{Mi}$
1	1	0	1	OR3	$Di + \overline{Mi}$
1	1	1	0	NAND	$\overline{Di} + \overline{Mi}$
1	1	1	1	1	ONE

→ SAM Organization Changes to 1024 x 1

→ Logic Operation Mode Reset

Di : External Data-in

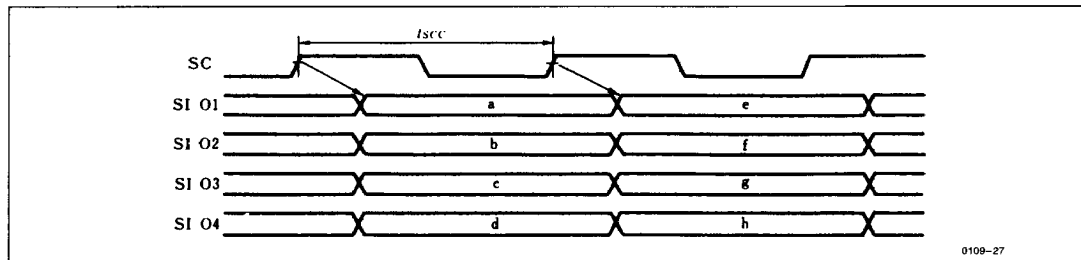
Mi : The Data of the Memory Cell



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Figure 2. The Shift Way of SAM Data

1) By 4 Mode (SAM Organization: 256 x 4)



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2) By 1 Mode (SAM Organization: 1024 x 1)

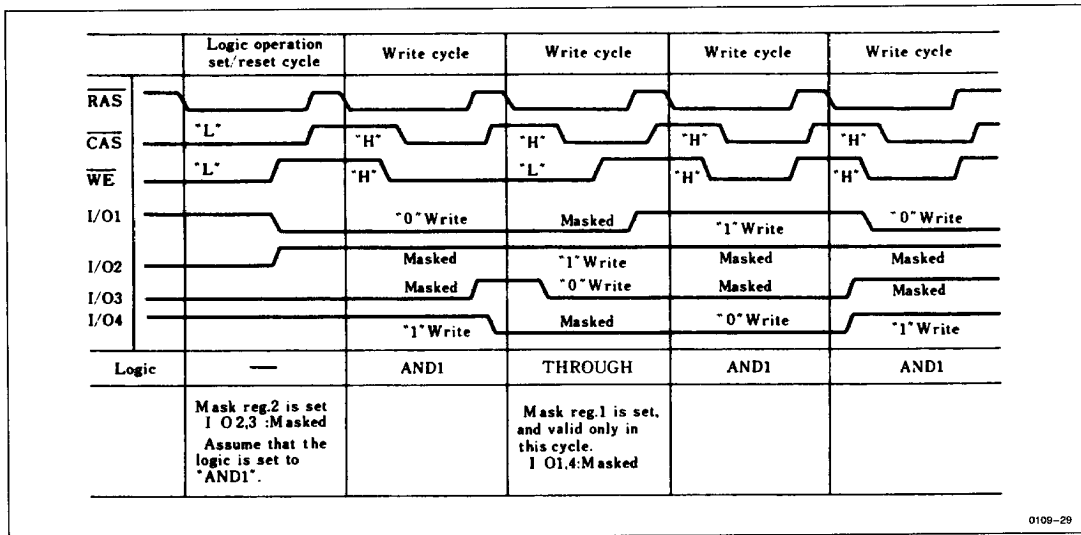
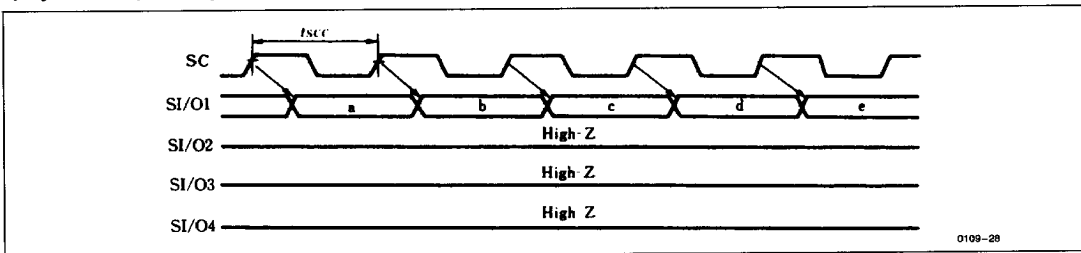


Figure 3. Example of Logic Operation Mode

