PIC16F7X7

PIC16F7X7 (Rev. A2 Silicon) Data Sheet Errata

The PIC16F7X7 Rev. A2 parts you have received conform functionally to the Device Data Sheet (DS30498**B**), except for the anomalies described below.

All the problems listed here will be addressed in future revisions of the PIC16F7X7 silicon.

None.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS30498**B**), the following clarifications and corrections should be noted.

Revision A2 Silicon can be identified by the following:

Device	Device ID	Rev. ID
PIC16F737	00 1011 101	0x1
PIC16F747	00 1011 111	0x1
PIC16F767	00 1101 111	0x1
PIC16F777	00 1110 101	0x1

1. Module: DC Characteristics (BOR Specifications)

The revision A2 silicon for the PIC16F7X7 family is not conforming to the BOR (parameter D005) specifications listed in Section 18.1 of the device data sheet.

The following table shows the current test limits (modified values are shown in **bold**).

18.1 DC Characteristics: PIC16F737/747/767/777 (Industrial, Extended) PIC16LF737/747/767/777 (Industrial)

PIC16LF737/747/767/777 (Industrial)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
PIC16F737/747/767/777 (Industrial, Extended)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VBOR	**Brown-out Reset Voltage**					
		PIC16LF7X7	Industrial Low Voltage				
D005		BORV1:BORV0 = 11	N/A	**N/A**	N/A	V	Reserved
		BORV1:BORV0 = 10	**2.45**	2.72	**2.99**	V	
		BORV1:BORV0 = 01	**3.88**	4.22	**4.64**	V	
		BORV1:BORV0 = 00	**4.09**	4.54	**4.99**	V	
D005		PIC16F7X7	Industrial				
		BORV1:BORV0 = 1x	N/A	—	N/A	V	Not in operating voltage range of device
		BORV1:BORV0 = 01	**3.80**	4.22	**4.64**	V	
		BORV1:BORV0 = 00	**4.09**	4.54	**4.99**	V	

2. Module: LVD Specifications

The revision A2 silicon for the PIC16F7X7 family is not conforming to the LVD (parameter D420) specifications listed in Table 18-3 of the device data sheet.

The following table shows the current test limits (modified values are shown in **bold**).

TABLE 18-3: LOW-VOLTAGE DETECT CHARACTERISTICS

PIC16LF7X7 (Industrial)				**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
PIC16F7X7 (Industrial, Extended)				**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Symbol**	**Characteristic**		**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D420		LVD Voltage on VDD Transition High to Low		Industrial				
		PIC16LF7X7	LVDL<3:0> = 0000	N/A	N/A	N/A	V	Reserved
			LVDL<3:0> = 0001	N/A	N/A	N/A	V	Reserved
			LVDL<3:0> = 0010	**2.08**	2.26	**2.44**	V	
			LVDL<3:0> = 0011	**2.25**	2.45	**2.65**	V	
			LVDL<3:0> = 0100	**2.35**	2.55	**2.75**	V	
			LVDL<3:0> = 0101	**2.55**	2.77	**2.99**	V	
			LVDL<3:0> = 0110	**2.64**	2.87	**3.10**	V	
			LVDL<3:0> = 0111	**2.82**	3.07	**3.32**	V	
			LVDL<3:0> = 1000	**3.09**	3.36	**3.63**	V	
			LVDL<3:0> = 1001	**3.28**	3.57	**3.86**	V	
			LVDL<3:0> = 1010	**3.38**	3.67	**3.96**	V	
			LVDL<3:0> = 1011	**3.56**	3.87	**4.18**	V	
			LVDL<3:0> = 1100	**3.74**	4.07	**4.40**	V	
			LVDL<3:0> = 1101	**3.94**	4.28	**4.62**	V	
			LVDL<3:0> = 1110	**4.23**	4.60	**4.97**	V	
D420		LVD Voltage on VDD Transition High to Low		Industrial				
		PIC16F7X7	LVDL<3:0> = 1011	**3.56**	3.87	**4.18**	V	
			LVDL<3:0> = 1100	**3.74**	4.07	**4.40**	V	
			LVDL<3:0> = 1101	**3.94**	4.28	**4.62**	V	
			LVDL<3:0> = 1110	**4.23**	4.60	**4.97**	V	

Legend: Shading of rows is to assist in readability of the table.

† Production tested at TAMB = 25°C. Specifications over temperature limits ensured by characterization.

3. Module: LVDCON Register

The Low-Voltage Detect Control register, Register 15-3 in the device data sheet, does not show the current low-voltage detection limits for bits 3-0.

The following register shows the current test limits (changes are shown in bold).

REGISTER 15-3: LVDCON REGISTER

U-0	U-0	R-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1
—	—	IRVST	LVDEN	LVDL3	LVDL2	LVDL1	LVDL0
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **IRVST:** Internal Reference Voltage Stable Flag bit

1 = Indicates that the Low-Voltage Detect logic will generate the interrupt flag at the specified voltage range

0 = Indicates that the Low-Voltage Detect logic will not generate the interrupt flag at the specified voltage range and the LVD interrupt should not be enabled

bit 4 **LVDEN:** Low-Voltage Detect Power Enable bit

1 = Enables LVD, powers up LVD circuit

0 = Disables LVD, powers down LVD circuit

bit 3-0 **LVDL3:LVDL0:** Low-Voltage Detection Limit bits

1111 = External analog input is used (input comes from the LVDIN pin)

1110 = **4.23V-4.97V**

1101 = **3.94V-4.62V**

1100 = **3.74V-4.40V**

1011 = **3.56V-4.18V**

1010 = **3.38V-3.96V**

1001 = **3.28V-3.86V**

1000 = **3.09V-3.63V**

0111 = **2.82V-3.32V**

0110 = **2.64V-3.10V**

0101 = **2.55V-2.99V**

0100 = **2.35V-2.75V**

0011 = **2.25V-2.65V**

0010 = **2.08V-2.44V**

0001 = Reserved

0000 = Reserved

Note: LVDL3:LVDL0 modes which result in a trip point below the valid operating voltage of the device are not tested.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REVISION HISTORY

Rev A Document (1/2004)
Original version of this document. Data Sheet Clarification issues 1 (BOR Specifications), 2 (LVD Specifications) and 3 (LVDCON Register).

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