2.5 V 184-pin Unbuffered DDR-I SDRAM Modules

128MByte, 256 MByte & 512 MByte Modules
PC1600, PC2100, PC2700
Preliminary Datasheet revision 0.94

- 184-pin Unbuffered 8-Byte Dual-In-Line DDR-I SDRAM non-parity and ECC-Modules for PC and Server main memory applications
- One bank 16M x 64, 32M × 64, 32M x 72 and two bank 64M x 64, 64M × 72 organization
- JEDEC standard Double Data Rate Synchronous DRAMs (DDR-I SDRAM) Single + 2.5 V (± 0.2 V) power supply
- Built with 256 Mbit DDR-I SDRAMs in 66-Lead TSOPII package
- Programmable $\overline{\text{CAS}}$ Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL_2 compatible
- Serial Presence Detect with E^2PROM
- Jedec standard MO-206 form factor: 133.35 mm × 31.75 mm × 4.00 mm max.
- Jedec standard reference layout
- Gold plated contacts

- Performance:

		-6	-7/-7F	-8	Unit
	Component Speed Grade	DDR333B	DDR266A/F	DDR200	
	Module Speed Grade	PC2700	PC2100	PC1600	
f_{CK}	Clock Frequency (max.) @ CL = 2.5	166	143	125	MHz
f_{CK}	Clock Frequency (max.) @ CL = 2	133	133	100	MHz

The HYS64/72D32000GU and HYS64/72D64020GU are industry standard 184-pin 8-byte Dual in-line Memory Modules (DIMMs) organized as 32M × 64 and 64M × 64 for non-parity and 32M x 72 and 64M x 72 for ECC main memory applications. The memory array is designed with 256Mbit Double Data Rate Synchronous DRAMs. A variety of decoupling capacitors are mounted on the PC board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.

Ordering Information

Type	Compliance Code	Description	SDRAM Technology
PC2700 (CL=2):			
HYS64D16301GU-6-B	PC2700-20330-C0	one bank 128 MB DIMM	256 MBit
HYS64D32300GU-6-B	PC2700-20330-A0	one bank 256 MB DIMM	256 MBit
HYS72D32300GU-6-B	PC2700-20330-A0	one bank 256 MB ECC-DIMM	256 Mbit
HYS64D64320GU-6-B	PC2700-20330-B0	two banks 512 MB DIMM	256 MBit
HYS72D64320GU-6-B	PC2700-20330-B0	two banks 512 MB ECC-DIMM	256 MBit
PC2100 (CL=2):			
HYS64D16301GU-7-B	PC2100-20330-C0	one bank 128 MB DIMM	256 MBit
HYS64D32000GU-7-B	PC2100-20330-A1	one bank 256 MB DIMM	256 MBit
HYS72D32000GU-7F-B	PC2100-20220-A1	one bank 256 MB ECC-DIMM	256 Mbit
HYS72D32000GU-7-B	PC2100-20330-A1	one bank 256 MB ECC-DIMM	256 Mbit
HYS64D64020GU-7-B	PC2100-20330-B1	two banks 512 MB DIMM	256 MBit
HYS72D64020GU-7F-B	PC2100-20220-B1	two banks 512 MB ECC-DIMM	256 MBit
HYS72D64020GU-7-B	PC2100-20330-B1	two banks 512 MB ECC-DIMM	256 MBit
PC1600 (CL=2):			
HYS64D16301GU-8-B	PC2100-20330-C0	one bank 128 MB DIMM	256 MBit
HYS64D32000GU-8-B	PC1600-20220-A1	one bank 256 MB DIMM	256 MBit
HYS72D32000GU-8-B	PC1600-20220-A1	one bank 256 MB ECC-DIMM	256 Mbit
HYS64D64020GU-8-B	PC1600-20220-B1	two banks 512 MB DIMM	256 MBit
HYS72D64020GU-8-B	PC1600-20220-B1	two banks 512 MB ECC-DIMM	256 MBit

Note: All part numbers end with a place code, designating the silicon-die revision. Reference information available on request. Example: HYS 72D32000GU-8-B, indicating Rev.B dies are used for the SDRAM components.
The Compliance Code is printed on the module labels and describes the speed sort fe. “PC2100”, the latencies (f.e. “20330” means CAS latency = 2, trcd latency = 3 and trp latency =3) and the Raw Card used for this module.

Pin Definitions and Functions

A0 - A12	Address Inputs	$\overline{S0}$, $\overline{S1}$	Chip Selects
BA0, BA1	Bank Selects	V_{DD}	Power (+ 2.5 V)
DQ0 - DQ63	Data Input/Output	V_{SS}	Ground
CB0 - CB7	Check Bits (x72 organization only)	V_{DDQ}	I/O Driver power supply
$\overline{RAS}$	Row Address Strobe	V_{DDID}	VDD Indentification flag
$\overline{CAS}$	Column Address Strobe	V_{REF}	I/O reference supply
$\overline{WE}$	Read/Write Input	V_{DDSPD}	Serial EEPROM power supply
CKE0 - CKE1	Clock Enable	SCL	Serial bus clock
DQS0 - DQS8	SDRAM low data strobes	SDA	Serial bus data line
CLK0 - CLK2,	SDRAM clock (positive lines)	SA0 - SA2	slave address select
$\overline{CLK0}$ - $\overline{CLK2}$	SDRAM clock (negative lines)	NC	no connect
DM0 - DM8 DQS9 - DQS17	SDRAM low data mask/ high data strobes		

note: $\overline{S1}$ and CKE1 are used on two bank modules only

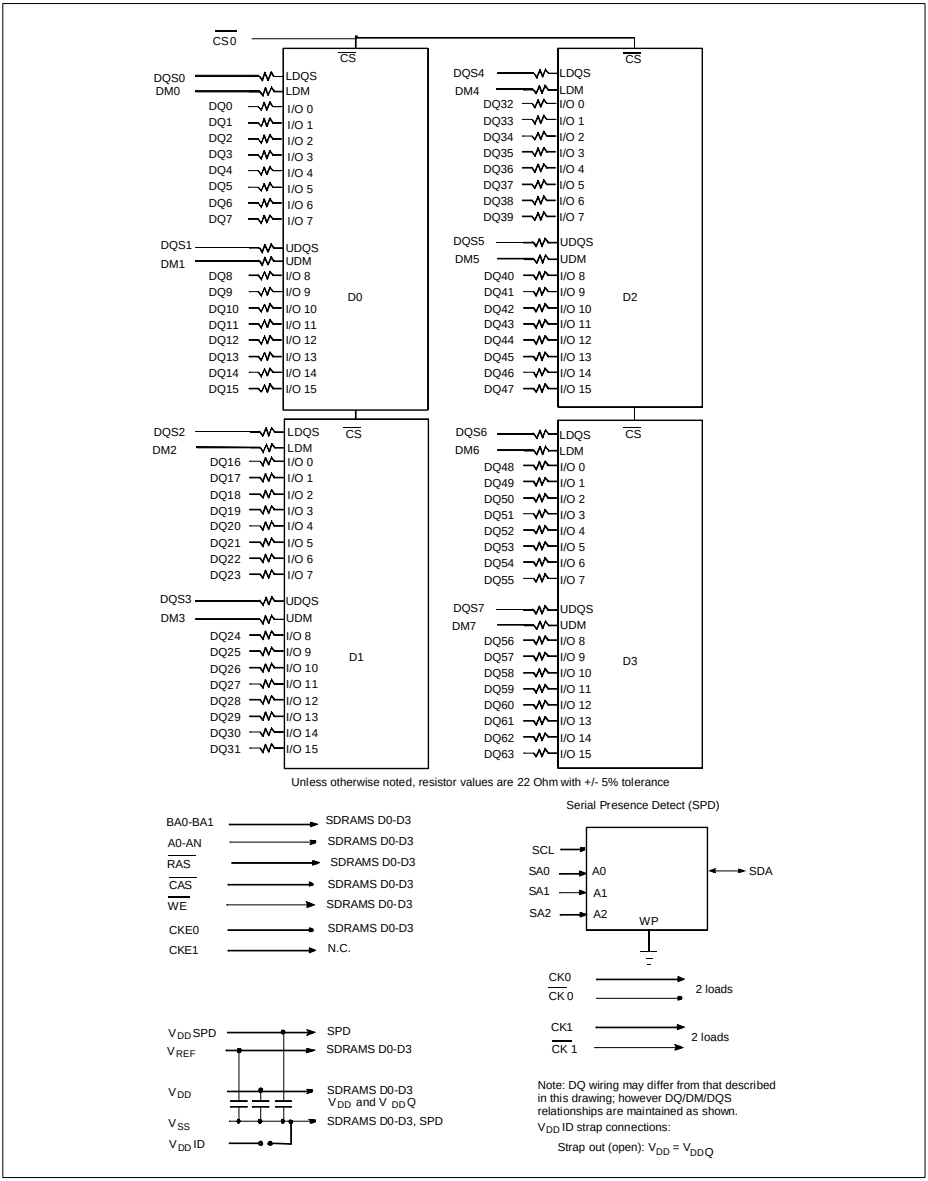
Address Format

Density	Organization	Memory Banks	SDRAMs	# of SDRAMs	# of row/bank/ columns bits	Refresh	Period	Interval
256 MB	32M x 64	1	32M x 8	8	13/2/10	8k	64 ms	7.8 µs
256 MB	32M x 72	1	32M x 8	9	13/2/10	8k	64 ms	7.8 µs
512 MB	64M × 64	2	32M x 8	16	13/2/10	8k	64 ms	7.8 µs
512 MB	64M × 72	2	32M x 8	18	13/2/10	8k	64 ms	7.8 µs

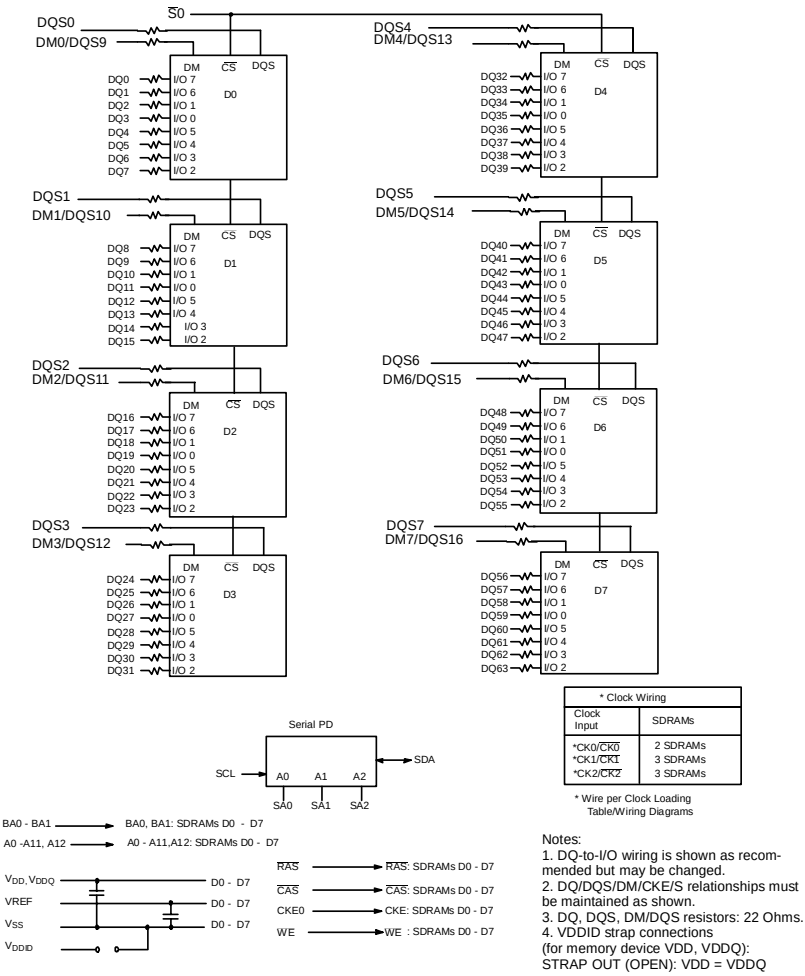
Pin Configuration

Frontside		Frontside		Backside		Backside	
PIN#	Symbol	PIN#	Symbol	PIN#	Symbol	PIN#	Symbol
1	VREF	48	A0	93	VSS	140	NC / DM8/DQS17
2	DQ0	49	NC / CB2	94	DQ4	141	A10
3	VSS	50	VSS	95	DQ5	142	NC / CB6
4	DQ1	51	NC / CB3	96	VDDQ	143	VDDQ
5	DQS0	52	BA1	97	DM0/DQS9	144	NC / CB7
6	DQ2	KEY		98	DQ6	KEY	
7	VDD	53	DQ32	99	DQ7	145	VSS
8	DQ3	54	VDDQ	100	VSS	146	DQ36
9	NC	55	DQ33	101	NC	147	DQ37
10	NC	56	DQS4	102	NC	148	VDD
11	VSS	57	DQ34	103	NC	149	DM4/DQS13
12	DQ8	58	VSS	104	VDDQ	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	VSS
15	VDDQ	61	DQ40	107	DM1/DQS10	153	DQ44
16	CLK1	62	VDDQ	108	VDD	154	$\overline{RAS}$
17	$\overline{CLK1}$	63	$\overline{WE}$	109	DQ14	155	DQ45
18	VSS	64	DQ41	110	DQ15	156	VDDQ
19	DQ10	65	$\overline{CAS}$	111	CKE1	157	$\overline{S0}$
20	DQ11	66	VSS	112	VDDQ	158	$\overline{S1}$
21	CKE0	67	DQS5	113	NC (BA2)	159	DM5/DQS14
22	VDDQ	68	DQ42	114	DQ20	160	VSS
23	DQ16	69	DQ43	115	NC / A12	161	DQ46
24	DQ17	70	VDD	116	VSS	162	DQ47
25	DQS2	71	NC	117	DQ21	163	NC
26	VSS	72	DQ48	118	A11	164	VDDQ
27	A9	73	DQ49	119	DM2/DQS11	165	DQ52
28	DQ18	74	VSS	120	VDD	166	DQ53
29	A7	75	$\overline{CLK2}$	121	DQ22	167	NC (A13)
30	VDDQ	76	CLK2	122	A8	168	VDD
31	DQ19	77	VDDQ	123	DQ23	169	DM6/DQS15
32	A5	78	DQS6	124	VSS	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	VSS	80	DQ51	126	DQ28	172	VDDQ
35	DQ25	81	VSS	127	DQ29	173	NC
36	DQS3	82	VDDID	128	VDDQ	174	DQ60
37	A4	83	DQ56	129	DM3/DQS12	175	DQ61
38	VDD	84	DQ57	130	A3	176	VSS
39	DQ26	85	VDD	131	DQ30	177	DM7/DQS16
40	DQ27	86	DQS7	132	VSS	178	DQ62
41	A2	87	DQ58	133	DQ31	179	DQ63
42	VSS	88	DQ59	134	NC / CB4	180	VDDQ
43	A1	89	VSS	135	NC / CB5	181	SA0
44	NC / CB0	90	NC	136	VDDQ	182	SA1
45	NC / CB1	91	SDA	137	CK0	183	SA2
46	VDD	92	SCL	138	$\overline{CK0}$	184	VDDSPD
47	NC / DQS8			139	VSS		

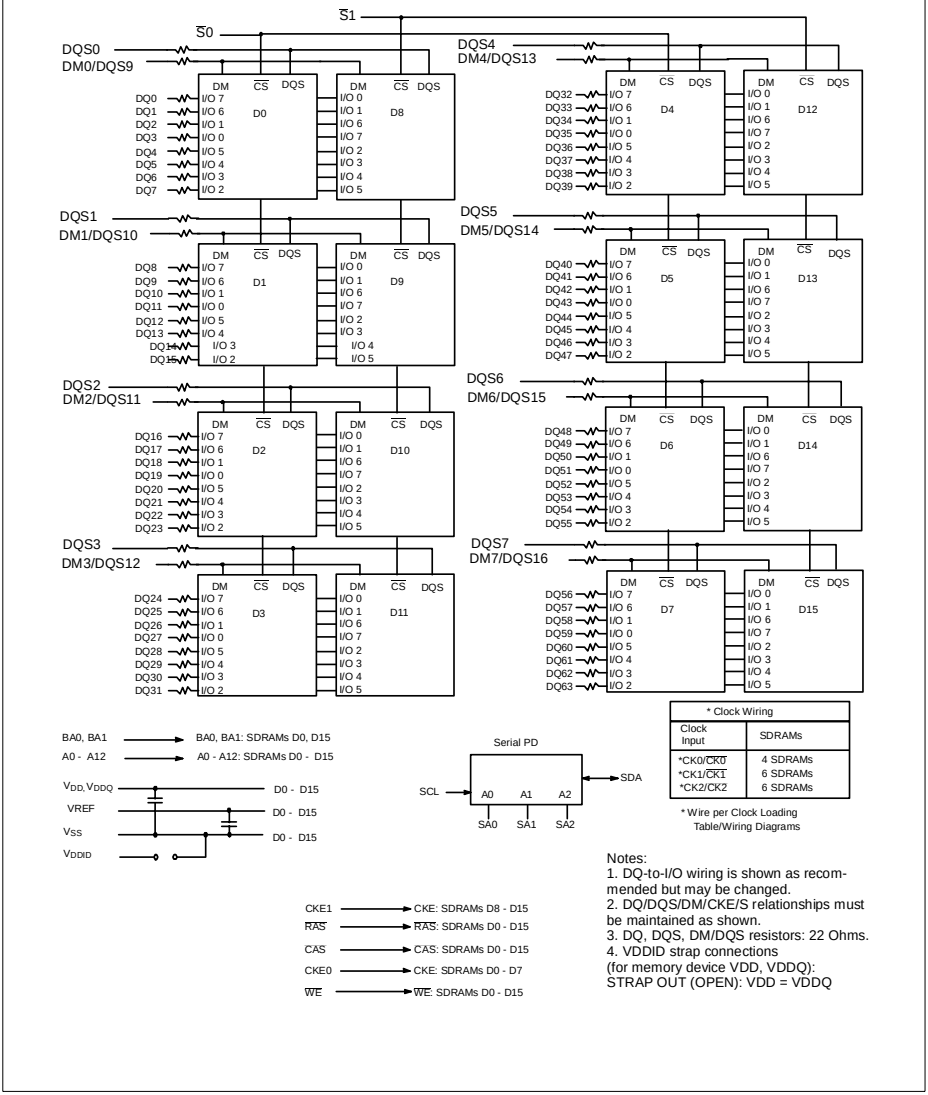
Note: Pins 44, 45, 47, 49, 51, 134, 135, 140 and 144 are NC (“no-connects”) on x64 organised non-ECC modules.



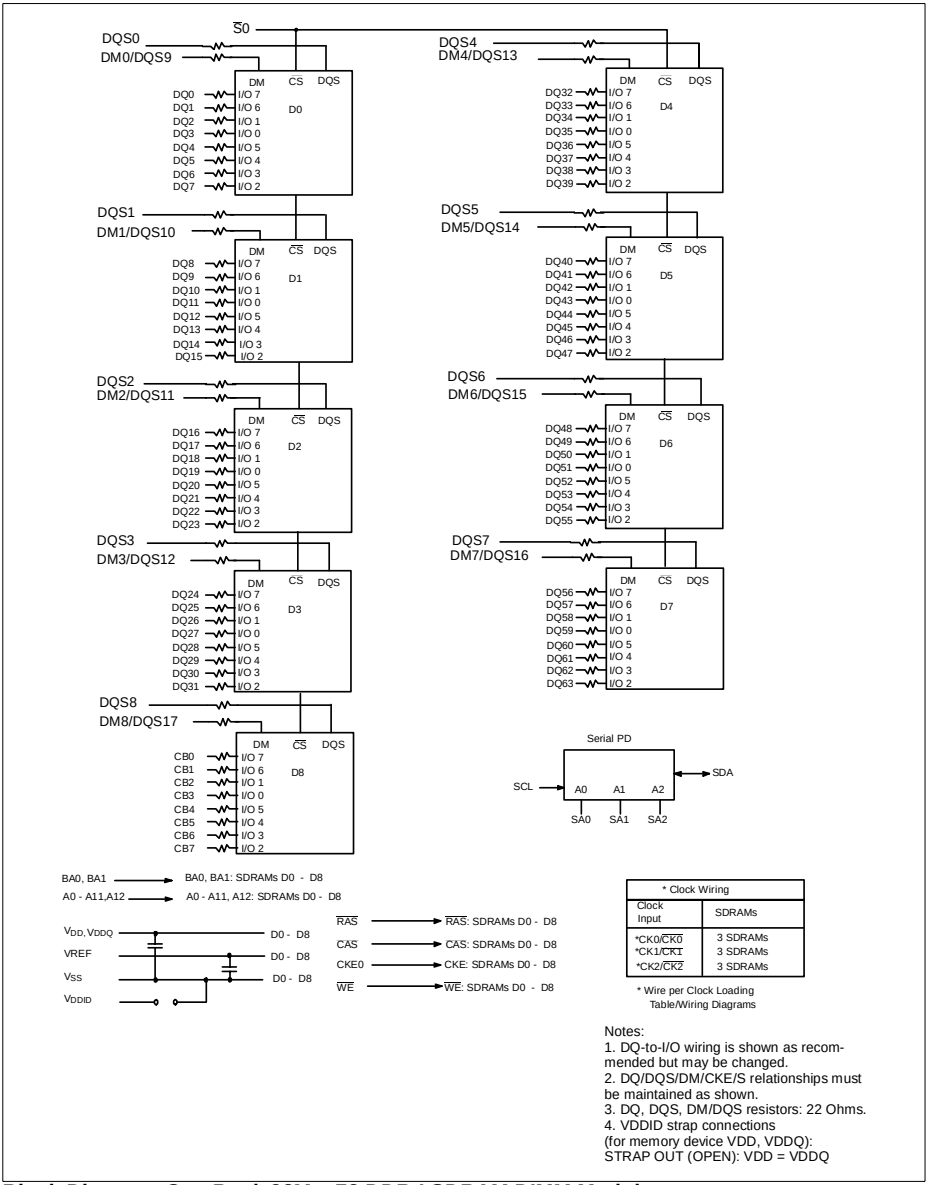
Block Diagram: One Bank 16M x 64 DDR-I SDRAM DIMM Module HYS64D32001GU using x16 organized SDRAMs



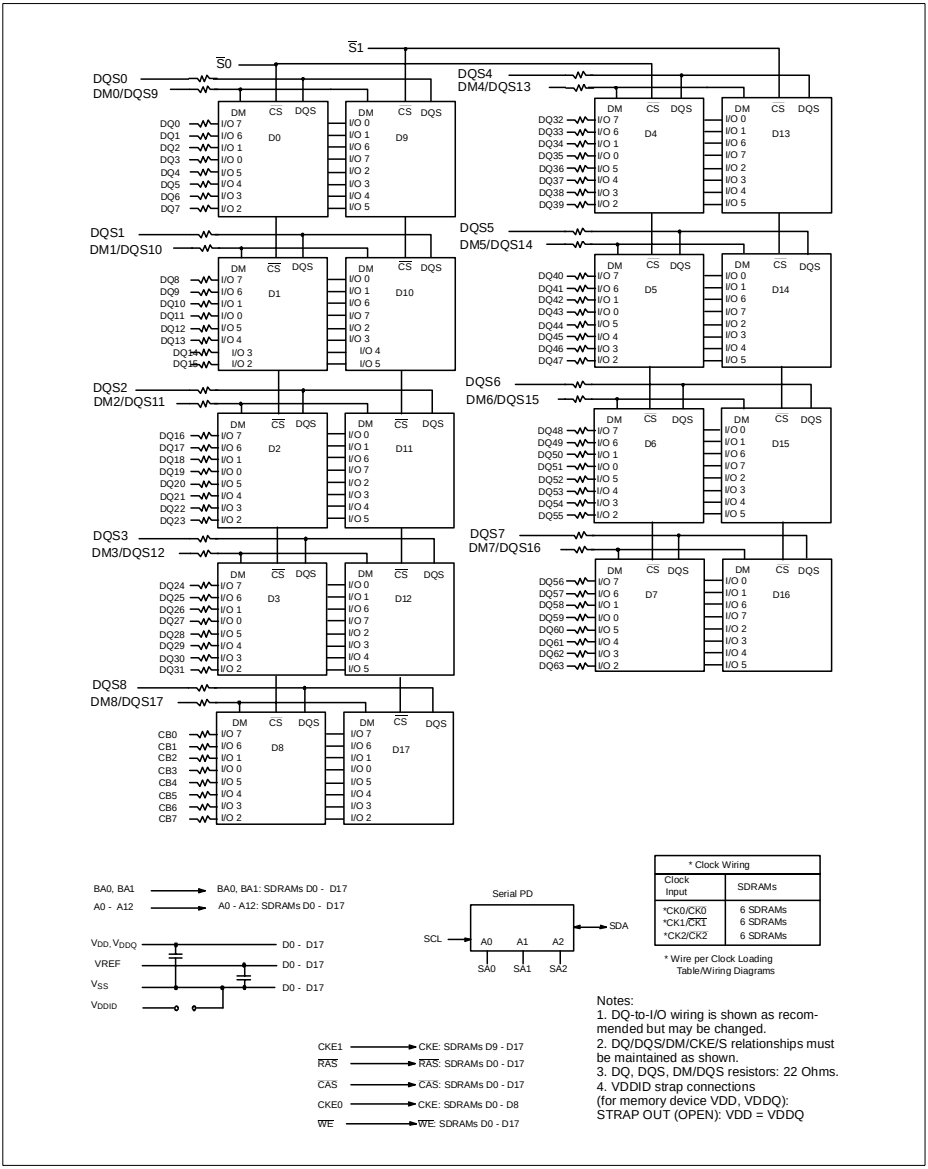
Block Diagram: One Bank 32M x 64 DDR-I SDRAM DIMM Module
HYS64D32000GU using x8 organized SDRAMs



Block Diagram: Two Bank 64M x 64 DDR-I SDRAM DIMM Modules
HYS64D64020GU using x8 Organized SDRAMs

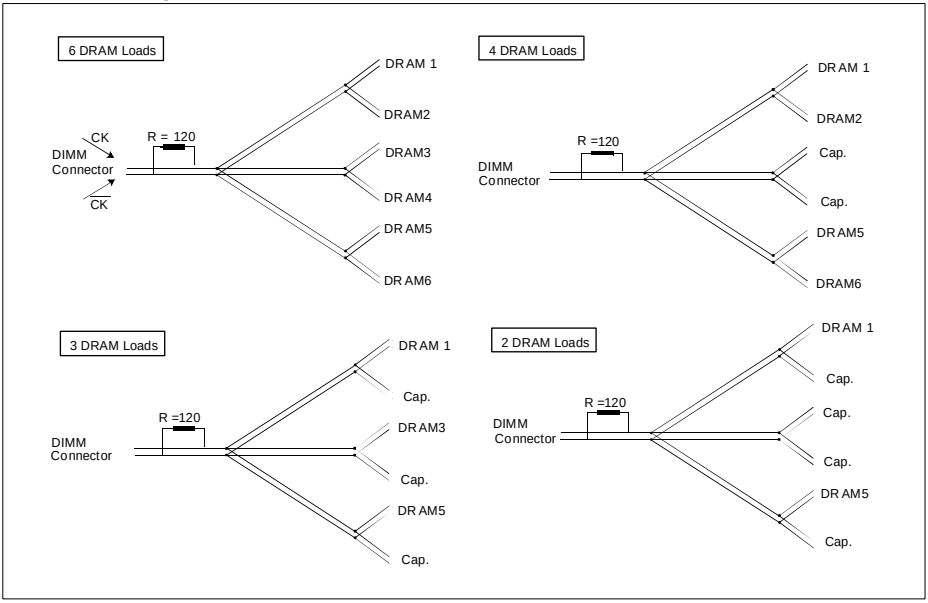


Block Diagram: One Bank 32M x 72 DDR-I SDRAM DIMM Module HYS72D32000GU using x8 organized SDRAMs



Block Diagram: Two Bank 64M x 72 DDR-I SDRAM DIMM Modules
HYS72D64020GU using x8 Organized SDRAMs

Clock Net Wiring



Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input / Output voltage relative to V_{SS}	V_{IN}, V_{OUT}	– 0.5	3.6	V
Power supply voltage on V_{DD}/V_{DDQ} to V_{SS}	V_{DD}, V_{DDQ}	– 0.5	3.6	V
Storage temperature range	T_{STG}	-55	+150	°C
Power dissipation (per SDRAM component)	P_D	–	1	W
Data out current (short circuit)	I_{OS}	–	50	mA

Permanent device damage may occur if “Absolute Maximum Ratings” are exceeded.
Functional operation should be restricted to recommended operation conditions.
Exposure to higher than recommended voltage for extended periods of time affect device reliability

Supply Voltage Levels

Parameter	Symbol	Limit Values			Unit	Notes
		min.	nom.	max.		
Device Supply Voltage	V_{DD}	2.3	2.5	2.7	V	–
Output Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V	1)
Input Reference Voltage	V_{REF}	0.49 x V_{DDQ}	0.5 x V_{DDQ}	0.51 x V_{DDQ}	V	2)
Termination Voltage	V_{TT}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V	3)
EEPROM supply voltage	V_{DDSPD}	2.3	2.5	3.6	V	

1) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}.

2) Peak to peak AC noise on V_{REF} may not exceed ± 2% $V_{REF\ (DC)}$. V_{REF} is also expected to track noise variations in V_{DDQ}.

3) V_{TT} of the transmitting device must track V_{REF} of the receiving device.

DC Operating Conditions (SSTL_2 Inputs)

(V_{DDQ} = 2.5 V, T_A = 70 °C, Voltage Referenced to V_{SS})

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
DC Input Logic High	$V_{IH\ (DC)}$	V_{REF} + 0.15	V_{DDQ} + 0.3	V	1)
DC Input Logic Low	$V_{IL\ (DC)}$	– 0.30	V_{REF} – 0.15	V	–
Input Leakage Current	I_{IL}	– 5	5	µA	2)
Output Leakage Current	I_{OL}	– 5	5	µA	2)

1) The relationship between the V_{DDQ} of the driving device and the V_{REF} of the receiving device is what determines noise margins. However, in the case of $V_{IH\ (max)}$ (input overdrive), it is the V_{DDQ} of the receiving device that is referenced. In the case where a device is implemented such that it supports SSTL_2 inputs but has no SSTL_2 outputs (such as a translator), and therefore no V_{DDQ} supply voltage connection, inputs must tolerate input overdrive to 3.0 V (High corner V_{DDQ} + 300 mV).

2) For any pin under test input of 0 V ≤ V_{IN} ≤ V_{DDQ} + 0.3 V. Values are shown per DDR-SDRAM component.

Operating, Standby and Refresh Currents (PC1600, -8)

Symbol	Parameter/Condition	128MB x64 1bank -8	256MB x64 1bank -8	256MB x72 1bank -8	512MB x64 2bank -8	512MB x72 2bank -8	Unit	Notes
		MAX	MAX	MAX	MAX	MAX		4
IDD0	**Operating Current**: one bank; active / precharge; tRC = tRC MIN; tCK = tCK MIN; DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles	380	720	810	1080	1215	mA	1
IDD1	**Operating Current**: one bank; active/read/precharge; Burst = 4; Refer to the following page for detailed test conditions.	420	800	900	1160	1305	mA	1, 3
IDD2P	**Precharge Power-Down Standby Current**: all banks idle; power-down mode; CKE <= VIL MAX; tCK = tCK MIN	28	56	63	112	126	mA	2
IDD2F	**Precharge Floating Standby Current**: /CS >= VIH MIN, all banks idle; CKE >= VIH MIN; tCK = tCK MIN ,address and other control inputs changing once per clock cycle, VIN = VREF for DQ, DQS and DM.	140	280	315	560	630	mA	2
IDD2Q	**Precharge Quiet Standby Current**: /CS >= VIH MIN, all banks idle; CKE >= VIH MIN; tCK = tCK MIN ,address and other control inputs stable at >= VIH MIN or <= VIL MAX; VIN = VREF for DQ, DQS and DM.	88	176	198	352	396	mA	2
IDD3P	**Active Power-Down Standby Current**: one bank active; power-down mode; CKE <= VIL MAX; tCK = tCK MIN;VIN = VREF for DQ, DQS and DM.	64	128	144	256	288	mA	2
IDD3N	**Active Standby Current**: one bank active; active / precharge;CS >= VIH MIN; CKE >= VIH MIN; tRC = tRAS MAX; tCK = tCK MIN; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	200	360	405	720	810	mA	2
IDD4R	**Operating Current**: one bank active; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR200, and DDR266A, CL=3 for DDR333; tCK = tCK MIN; IOUT = 0mA	440	760	855	1120	1260	mA	1, 3
IDD4W	**Operating Current**: one bank active; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR200, and DDR266A, CL=3 for DDR333; tCK = tCK MIN	480	840	945	1200	1350	mA	1
IDD5	**Auto-Refresh Current**: tRC = tRFC MIN, distributed refresh	680	1360	1530	1720	1935	mA	1
IDD6	**Self-Refresh Current**: CKE <= 0.2V; external clock on; tCK = tCK MIN	10	20	22,5	40	45	mA	
IDD7	**Operating Current**: four bank; four bank interleaving with BL=4; Refer to the following page for detailed test conditions.	880	1680	1890	2040	2295	mA	1, 3

1. The module IDD values are calculated from the component IDD datasheet values as:
   n * IDDx[component] for single bank modules (n: number of components per module bank)
   n * IDDx[component] + n * IDD3N[component] for two bank modules (n: number of components per module bank)
2. The module IDD values are calculated from the component IDD datasheet values as:
   n * IDDx[component] for single bank modules (n: number of components per module bank)
   2 * n * IDDx[component] for two bank modules (n: number of components per module bank)
3. DQ I/O (IDDQ) currents are not included into calculations: module IDD values will be measured differently depending on load conditions
4. Test condition for maximum values: VDD = 2.7V ,Ta = 10°C

Operating, Standby and Refresh Currents (PC2100, -7)

Symbol	Parameter/Condition	128MB x64 1bank -7	256MB x64 1bank -7	256MB x72 1bank -7	512MB x64 2bank -7	512MB x72 2bank -7	Unit	Notes
		MAX	MAX	MAX	MAX	MAX		4
IDD0	**Operating Current**: one bank; active / precharge; tRC = tRC MIN; tCK = tCK MIN; DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles	420	800	900	1240	1395	mA	1
IDD1	**Operating Current**: one bank; active/read/precharge; Burst = 4; Refer to the following page for detailed test conditions.	460	880	990	1320	1485	mA	1, 3
IDD2P	**Precharge Power-Down Standby Current**: all banks idle; power-down mode; CKE <= VIL MAX; tCK = tCK MIN	32	64	72	128	144	mA	2
IDD2F	**Precharge Floating Standby Current**: /CS >= VIH MIN, all banks idle; CKE >= VIH MIN; tCK = tCK MIN ,address and other control inputs changing once per clock cycle, VIN = VREF for DQ, DQS and DM.	160	320	360	640	720	mA	2
IDD2Q	**Precharge Quiet Standby Current**: /CS >= VIH MIN, all banks idle; CKE >= VIH MIN; tCK = tCK MIN ,address and other control inputs stable at >= VIH MIN or <= VIL MAX; VIN = VREF for DQ, DQS and DM.	100	200	225	400	450	mA	2
IDD3P	**Active Power-Down Standby Current**: one bank active; power-down mode; CKE <= VIL MAX; tCK = tCK MIN;VIN = VREF for DQ, DQS and DM.	72	144	162	288	324	mA	2
IDD3N	**Active Standby Current**: one bank active; active / precharge;CS >= VIH MIN; CKE >= VIH MIN; tRC = tRAS MAX; tCK = tCK MIN; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	240	440	495	880	990	mA	2
IDD4R	**Operating Current**: one bank active; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR200, and DDR266A, CL=3 for DDR333; tCK = tCK MIN; IOUT = 0mA	520	920	1035	1360	1530	mA	1, 3
IDD4W	**Operating Current**: one bank active; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR200, and DDR266A, CL=3 for DDR333; tCK = tCK MIN	560	1000	1125	1440	1620	mA	1
IDD5	**Auto-Refresh Current**: tRC = tRFC MIN, distributed refresh	720	1440	1620	1880	2115	mA	1
IDD6	**Self-Refresh Current**: CKE <= 0.2V; external clock on; tCK = tCK MIN	10	20	22,5	40	45	mA	
IDD7	**Operating Current**: four bank; four bank interleaving with BL=4; Refer to the following page for detailed test conditions.	940	1800	2025	2240	2520	mA	1, 3

1. The module IDD values are calculated from the component IDD datasheet values as:
   n * IDDx[component] for single bank modules (n: number of components per module bank)
   n * IDDx[component] + n * IDD3N[component] for two bank modules (n: number of components per module bank)
2. The module IDD values are calculated from the component IDD datasheet values as:
   n * IDDx[component] for single bank modules (n: number of components per module bank)
   2 * n * IDDx[component] for two bank modules (n: number of components per module bank)
3. DQ I/O (IDDQ) currents are not included into calculations: module IDD values will be measured differently depending on load conditions
4. Test condition for maximum values: VDD = 2.7V ,Ta = 10°C

Operating, Standby and Refresh Currents (PC2100, -7F)

Symbol	Parameter/Condition	256MB x72 1bank -7F	512MB x72 2bank -7F	Unit	Notes
		MAX	MAX		4
IDD0	**Operating Current**: one bank; active / precharge; tRC = tRC MIN; tCK = tCK MIN; DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles	990	1485	mA	1
IDD1	**Operating Current**: one bank; active/read/precharge; Burst = 4; Refer to the following page for detailed test conditions.	1080	1575	mA	1, 3
IDD2P	**Precharge Power-Down Standby Current**: all banks idle; power-down mode; CKE <= VIL MAX; tCK = tCK MIN	72	144	mA	2
IDD2F	**Precharge Floating Standby Current**: /CS >= VIH MIN, all banks idle; CKE >= VIH MIN; tCK = tCK MIN ,address and other control inputs changing once per clock cycle, VIN = VREF for DQ, DQS and DM.	360	720	mA	2
IDD2Q	**Precharge Quiet Standby Current**: /CS >= VIH MIN, all banks idle; CKE >= VIH MIN; tCK = tCK MIN ,address and other control inputs stable at >= VIH MIN or <= VIL MAX; VIN = VREF for DQ, DQS and DM.	225	450	mA	2
IDD3P	**Active Power-Down Standby Current**: one bank active; power-down mode; CKE <= VIL MAX; tCK = tCK MIN;VIN = VREF for DQ, DQS and DM.	162	324	mA	2
IDD3N	**Active Standby Current**: one bank active; active / precharge;CS >= VIH MIN; CKE >= VIH MIN; tRC = tRAS MAX; tCK = tCK MIN; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	495	990	mA	2
IDD4R	**Operating Current**: one bank active; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR200, and DDR266A, CL=3 for DDR333; tCK = tCK MIN; IOUT = 0mA	1035	1530	mA	1, 3
IDD4W	**Operating Current**: one bank active; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR200, and DDR266A, CL=3 for DDR333; tCK = tCK MIN	1125	1620	mA	1
IDD5	**Auto-Refresh Current**: tRC = tRFC MIN, distributed refresh	1620	2115	mA	1
IDD6	**Self-Refresh Current**: CKE <= 0.2V; external clock on; tCK = tCK MIN	22,5	45	mA	
IDD7	**Operating Current**: four bank; four bank interleaving with BL=4; Refer to the following page for detailed test conditions.	2025	2520	mA	1, 3

1. The module IDD values are calculated from the component IDD datasheet values as:
   n * IDDx[component] for single bank modules (n: number of components per module bank)
   n * IDDx[component] + n * IDD3N[component] for two bank modules (n: number of components per module bank)
2. The module IDD values are calculated from the component IDD datasheet values as:
   n * IDDx[component] for single bank modules (n: number of components per module bank)
   2 * n * IDDx[component] for two bank modules (n: number of components per module bank)
3. DQ I/O (IDDQ) currents are not included into calculations: module IDD values will be measured differently depending on load conditions
4. Test condition for maximum values: VDD = 2.7V ,Ta = 10°C

Operating, Standby and Refresh Currents (PC2700, -6)

Symbol	Parameter/Condition	128MB x64 1bank -6	256MB x64 1bank -6	256MB x72 1bank -6	512MB x64 2bank -6	512MB x72 2bank -6	Unit	Notes
		MAX	MAX	MAX	MAX	MAX		4
IDD0	**Operating Current**: one bank; active / precharge; tRC = tRC MIN; tCK = tCK MIN; DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles	460	880	990	1400	1575	mA	1
IDD1	**Operating Current**: one bank; active/read/precharge; BL 4; Refer to the following page for detailed test conditions.	500	960	1080	1480	1665	mA	1, 3
IDD2P	**Precharge Power-Down Standby Current**: all banks idle; power-down mode; CKE <= VIL MAX; tCK = tCK MIN	36	72	81	144	162	mA	2
IDD2F	**Precharge Floating Standby Current**: /CS >= VIH MIN, all banks idle; CKE >= VIH MIN; tCK = tCK MIN ,address and other control inputs changing once per clock cycle, VIN = VREF for DQ, DQS and DM.	220	440	495	880	990	mA	2
IDD2Q	**Precharge Quiet Standby Current**: /CS >= VIH MIN, all banks idle; CKE >= VIH MIN; tCK = tCK MIN ,address and other control inputs stable at >= VIH MIN or <= VIL MAX; VIN = VREF for DQ, DQS and DM.	112	224	252	448	504	mA	2
IDD3P	**Active Power-Down Standby Current**: one bank active; power-down mode; CKE <= VIL MAX; tCK = tCK MIN;VIN = VREF for DQ, DQS and DM.	84	168	189	336	378	mA	2
IDD3N	**Active Standby Current**: one bank active; active / precharge;CS >= VIH MIN; CKE >= VIH MIN; tRC = tRAS MAX; tCK = tCK MIN; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	280	520	585	1040	1170	mA	2
IDD4R	**Operating Current**: one bank active; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR200, and DDR266A, CL=3 for DDR333; tCK = tCK MIN; IOUT = 0mA	640	1120	1260	1640	1845	mA	1, 3
IDD4W	**Operating Current**: one bank active; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR200, and DDR266A, CL=3 for DDR333; tCK = tCK MIN	660	1160	1305	1680	1890	mA	1
IDD5	**Auto-Refresh Current**: tRC = tRFC MIN, distributed refresh	760	1520	1710	2040	2295	mA	1
IDD6	**Self-Refresh Current**: CKE <= 0.2V; external clock on; tCK = tCK MIN	10	20	22,5	40	45	mA	
IDD7	**Operating Current**: four bank; four bank interleaving with BL=4; Refer to the following page for detailed test conditions.	1140	2160	2430	2680	3015	mA	1, 3

1. The module IDD values are calculated from the component IDD datasheet values as:
   n * IDDx[component] for single bank modules (n: number of components per module bank)
   n * IDDx[component] + n * IDD3N[component] for two bank modules (n: number of components per module bank)
2. The module IDD values are calculated from the component IDD datasheet values as:
   n * IDDx[component] for single bank modules (n: number of components per module bank)
   2 * n * IDDx[component] for two bank modules (n: number of components per module bank)
3. DQ I/O (IDDQ) currents are not included into calculations: module IDD values will be measured differently depending on load conditions
4. Test condition for maximum values: VDD = 2.7V ,Ta = 10°C

Electrical Characteristics & AC Timing for DDR-I components

(for reference only)

(0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5V ± 0.2V; V_{DD} = 2.5V ± 0.2V)

Symbol	Parameter		DDR333 -6		DDR266F -7F		DDR266A -7		DDR200 -8		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
t_{AC}	DQ output access time from CK/$\overline{CK}$		– 0.7	+ 0.7	– 0.75	+ 0.75	– 0.75	+ 0.75	– 0.8	+ 0.8	ns	1-4
t_{DQSCK}	DQS output access time from CK/$\overline{CK}$		– 0.7	+ 0.7	– 0.75	+ 0.75	– 0.75	+ 0.75	– 0.8	+ 0.8	ns	1-4
t_{CH}	CK high-level width		0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	1-4
t_{CL}	CK low-level width		0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	1-4
t_{HP}	Clock Half Period		min (t_{CL}, t_{CH})		min (t_{CL}, t_{CH})		min (t_{CL}, t_{CH})		min (t_{CL}, t_{CH})		ns	1-4
t_{CK}	Clock cycle time	CL = 2.5	6	12	7	12	7	12	8	12	ns	1-4
t_{CK}	Clock cycle time	CL = 2.0	7.5	12	7.5	12	7.5	12	10	12	ns	1-4
t_{DH}	DQ and DM input hold time		0.45	–	0.5		0.5		0.6		ns	1-4
t_{DS}	DQ and DM input setup time		0.45	–	0.5		0.5		0.6		ns	1-4
t_{IPW}	Control and Addr. input pulse width (each input)		2.2		2.2		2.2		2.5		ns	1, 10
t_{DIPW}	DQ and DM input pulse width (each input)		1.75		1.75		1.75		2		ns	1-4, 11
t_{HZ}	Data-out high-impedence time from CK/$\overline{CK}$		– 0.7	+ 0.7	– 0.75	+ 0.75	– 0.75	+ 0.75	– 0.8	+ 0.8	ns	1-4, 5
t_{LZ}	Data-out low-impedence time from CK/$\overline{CK}$		– 0.7	+ 0.7	– 0.75	+ 0.75	– 0.75	+ 0.75	– 0.8	+ 0.8	ns	1-4, 5
t_{DQSS}	Write command to 1st DQS latching transition		0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	1-4
t_{DQSQ}	DQS-DQ skew (for DQS & associated DQ signals)			+ 0.4		+ 0.5		+ 0.5		+ 0.6	ns	1-4
t_{QHS}	Data hold skew factor		+ 0.55	–		+ 0.75		+ 0.75		+ 1.0	ns	1-4
t_{QH}	Data Output hold time from DQS		t_{HP}- t_{QHS}		t_{HP}- t_{QHS}		t_{HP}- t_{QHS}		t_{HP}- t_{QHS}		ns	1-4
$t_{DQSL,H}$	DQS input low (high) pulse width (write cycle)		0.35		0.35		0.35		0.35		t_{CK}	1-4
t_{DSS}	DQS falling edge to CK setup time (write cycle)		0.2		0.2		0.2		0.2		t_{CK}	1-4
t_{DSH}	DQS falling edge hold time from CK (write cycle)		0.2		0.2		0.2		0.2		t_{CK}	1-4
t_{MRD}	Mode register set command cycle time		12		14		14		16		ns	1-4
t_{WPRES}	Write preamble setup time		0		0		0		0		ns	1-4, 7
t_{WPST}	Write postamble		0.40	0.60	0.40	0.60	0.40	0.60	0.40	0.60	t_{CK}	1-4, 6
t_{WPRE}	Write preamble		0.25		0.25		0.25		0.25		t_{CK}	1-4
t_{IS}	Address and control input setup time	fast slew rate	0.75		0.9		0.9		1.1		ns	2-4, 10,11
t_{IS}	Address and control input setup time	slow slew rate			1.0		1.0		1.1		ns	2-4, 10,11
t_{IH}	Address and control input hold time	fast slew rate	0.75		0.9		0.9		1.1		ns	2-4, 10,11
t_{IH}	Address and control input hold time	slow slew rate			1.0		1.0		1.1		ns	2-4, 10,11
t_{RPRE}	Read preamble		0.9		0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	1-4
t_{RPST}	Read postamble		0.40		0.40	0.60	0.40	0.60	0.40	0.60	t_{CK}	1-4
t_{RAS}	Active to Precharge command		42		45	120,000	45	120,000	50	120,000	ns	1-4
t_{RC}	Active to Active/Auto-refresh command period		60		60		65		70		ns	1-4

Electrical Characteristics & AC Timing for DDR-I components

(for reference only)

(0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5V ± 0.2V; V_{DD} = 2.5V ± 0.2V)

Symbol	Parameter	DDR333 -6		DDR266F -7F		DDR266A -7		DDR200 -8		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{RFC}	Auto-refresh to Active/Auto-refresh command period	72		75		75		80		ns	1-4
t_{RCD}	Active to Read or Write delay	18		15		20		20		ns	1-4
t_{RP}	Precharge command period	18		15		20		20		ns	1-4
t_{RRD}	Active bank A to Active bank B command	12		15		15		15		ns	1-4
t_{WR}	Write recovery time	15		15		15		15		ns	1-4
t_{DAL}	Auto precharge write recovery + precharge time	(twr/tck) + (trp/tck)								t_{CK}	1-4,9
t_{WTR}	Internal write to read command delay	1		1		1		1		t_{CK}	1-4
t_{XSNR}	Exit self-refresh to non-read command	75		75		75		80		ns	1-4
t_{XSRD}	Exit self-refresh to read command	200		200		200		200		t_{CK}	1-4
t_{REFI}	Average Periodic Refresh Interval		7.8		7.8		7.8		7.8	µs	1-4, 8

1. Input slew rate >=1V/ns for DDR266 and = 1V/ns for DDR200.
2. The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is V_{REF}. CK/$\overline{CK}$ slew rate are >= 1.0 V/ns.
3. Inputs are not recognized as valid until V_{REF} stabilizes.
4. The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (Note 3) is V_{TT}.
5. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
6. The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
7. The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.
8. A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.
9. For each of the terms, if not already an integer, round to the next highest integer. tCK is equal to the actual system clock cycle time.
10. These parameters guarantee device timing, but they are not necessarily tested on each device
11. Fast slew rate >= 1.0 V/ns , slow slew rate >= 0.5 V/ns and < 1V/ns for command/address and CK & $\overline{CK}$ slew rate >1.0 V/ns, measured between VOH(ac) and VOL(ac)

SPD Codes for PC1600 Modules "-8"

Byte#	Description		128MB x64 1bank -8	256MB x64 1bank -8	256MB x72 1bank -8	512MB x64 2bank -8	512MB x72 2bank -8
			HEX	HEX	HEX	HEX	HEX
0	Number of SPD Bytes	128	80	80	80	80	80
1	Total Bytes in Serial PD	256	08	08	08	08	08
2	Memory Type	DDR-SDRAM	07	07	07	07	07
3	Number of Row Addresses	13	0D	0D	0D	0D	0D
4	Number of Column Addresses	9 / 10	09	0A	0A	0A	0A
5	Number of DIMM Banks	1 / 2	01	01	01	02	02
6	Module Data Width	x64 / x72	40	40	48	40	48
7	Module Data Width (cont'd)	0	00	00	00	00	00
8	Module Interface Levels	SSTL_2.5	04	04	04	04	04
9	SDRAM Cycle Time at CL = 2.5	8 ns	80	80	80	80	80
10	Access Time from Clock at CL = 2.5	0.8 ns	80	80	80	80	80
11	DIMM Config	non-ECC / ECC	00	00	02	00	02
12	Refresh Rate/Type	Self-Refresh, 7.8 ms	82	82	82	82	82
13	SDRAM Width, Primary	x16 / x8	10	08	08	08	08
14	Error Checking SDRAM Data Width	na / x8	00	00	08	00	08
15	Minimum Clock Delay for Back-to-Back Random Column Address	tccd = 1 CLK	01	01	01	01	01
16	Burst Length Supported	2, 4 & 8	0E	0E	0E	0E	0E
17	Number of SDRAM Banks	4	04	04	04	04	04
18	Supported CAS Latencies	CAS latency = 2 & 2.5	0C	0C	0C	0C	0C
19	CS Latencies	CS latency = 0	01	01	01	01	01
20	WE Latencies	Write latency = 1	02	02	02	02	02
21	SDRAM DIMM Module Attributes	unbuffered	20	20	20	20	20
22	SDRAM Device Attributes: General	–	C0	C0	C0	C0	C0
23	Min. Clock Cycle Time at CAS Latency = 2	10.0 ns	A0	A0	A0	A0	A0
24	Access Time from Clock for CL = 2	0.8 ns	80	80	80	80	80
25	Minimum Clock Cycle Time at CL = 1.5	not supported	00	00	00	00	00
26	Access Time from Clock at CL = 1.5	not supported	00	00	00	00	00
27	Minimum Row Precharge Time	20 ns	50	50	50	50	50
28	Minimum Row Act. to Row Act. Delay tRRD	15 ns	3C	3C	3C	3C	3C
29	Minimum RAS to CAS Delay tRCD	20 ns	50	50	50	50	50
30	Minimum RAS Pulse Width tRAS	50 ns	32	32	32	32	32
31	Module Bank Density (per bank)	256MByte	20	40	40	40	40
32	Addr. and Command Setup Time	1.1 ns	B0	B0	B0	B0	B0
33	Addr. and Command Hold Time	1.1 ns	B0	B0	B0	B0	B0
34	Data Input Setup Time	0.6 ns	60	60	60	60	60
35	Data Input Hold Time	0.6 ns	60	60	60	60	60
36-40	Superset Information	–	00	00	00	00	00
41	Minimum Core Cycle Time tRC	70 ns	46	46	46	46	46
42	Min. Auto Refresh Cmd Cycle Time tRFC	80 ns	50	50	50	50	50
43	Maximum Clock Cycle Time tck	12 ns	30	30	30	30	30
44	Max. DQS-DQ Skew tDQSQ	0.6 ns	3C	3C	3C	3C	3C
45	X-Factor tQHS	1.0 ns	A0	A0	A0	A0	A0
46-61	Superset Information	-	00	00	00	00	00
62	SPD Revision	Revision 0.0	00	00	00	00	00
63	Checksum for Bytes 0 - 62	–	8E	A7	B9	A8	BA
64	Manufacturers JEDEC ID Code	–	C1	C1	C1	C1	C1
65-71	Manufacturer	–	INFINEON	INFINEON	INFINEON	INFINEON	INFINEON
72	Module Assembly Location	–					
73-90	Module Part Number	–					
91-92	Module Revision Code	–					
93-94	Module Manufacturing Date	–					
95-98	Module Serial Number	–					
99-127	–	–					
128-255	open for Customer use	–					

SPD Codes for PC2100 Modules "-7"

Byte#	Description		128MB x64 1bank -7	256MB x64 1bank -7	256MB x72 1bank -7	512MB x64 2bank -7	512MB x72 2bank -7
			HEX	HEX	HEX	HEX	HEX
0	Number of SPD Bytes	128	80	80	80	80	80
1	Total Bytes in Serial PD	256	08	08	08	08	08
2	Memory Type	DDR-SDRAM	07	07	07	07	07
3	Number of Row Addresses	13	0D	0D	0D	0D	0D
4	Number of Column Addresses	9 / 10	09	0A	0A	0A	0A
5	Number of DIMM Banks	1 / 2	01	01	01	02	02
6	Module Data Width	x64 / x72	40	40	48	40	48
7	Module Data Width (cont'd)	0	00	00	00	00	00
8	Module Interface Levels	SSTL_2.5	04	04	04	04	04
9	SDRAM Cycle Time at CL = 2.5	7 ns	70	70	70	70	70
10	Access Time from Clock at CL = 2.5	0.75 ns	75	75	75	75	75
11	DIMM Config	non-ECC / ECC	00	00	02	00	02
12	Refresh Rate/Type	Self-Refresh, 7.8 ms	82	82	82	82	82
13	SDRAM Width, Primary	x16 / x8	10	08	08	08	08
14	Error Checking SDRAM Data Width	na / x8	00	00	08	00	08
15	Minimum Clock Delay for Back-to-Back Random Column Address	tccd = 1 CLK	01	01	01	01	01
16	Burst Length Supported	2, 4 & 8	0E	0E	0E	0E	0E
17	Number of SDRAM Banks	4	04	04	04	04	04
18	Supported CAS Latencies	CAS latency = 2 & 2.5	0C	0C	0C	0C	0C
19	CS Latencies	CS latency = 0	01	01	01	01	01
20	WE Latencies	Write latency = 1	02	02	02	02	02
21	SDRAM DIMM Module Attributes	unbuffered	20	20	20	20	20
22	SDRAM Device Attributes: General	–	C0	C0	C0	C0	C0
23	Min. Clock Cycle Time at CAS Latency = 2	7.5 ns	75	75	75	75	75
24	Access Time from Clock for CL = 2	0.75 ns	75	75	75	75	75
25	Minimum Clock Cycle Time at CL = 1.5	not supported	00	00	00	00	00
26	Access Time from Clock at CL = 1.5	not supported	00	00	00	00	00
27	Minimum Row Precharge Time	20 ns	50	50	50	50	50
28	Minimum Row Act. to Row Act. Delay tRRD	15 ns	3C	3C	3C	3C	3C
29	Minimum RAS to CAS Delay tRCD	20 ns	50	50	50	50	50
30	Minimum RAS Pulse Width tRAS	45 ns	2D	2D	2D	2D	2D
31	Module Bank Density (per bank)	128MByte / 256MByte	20	40	40	40	40
32	Addr. and Command Setup Time	0.9 ns	90	90	90	90	90
33	Addr. and Command Hold Time	0.9 ns	90	90	90	90	90
34	Data Input Setup Time	0.5 ns	50	50	50	50	50
35	Data Input Hold Time	0.5 ns	50	50	50	50	50
36-40	Superset Information	–	00	00	00	00	00
41	Minimum Core Cycle Time tRC	65 ns	41	41	41	41	41
42	Min. Auto Refresh Cmd Cycle Time tRFC	75 ns	4B	4B	4B	4B	4B
43	Maximum Clock Cycle Time tck	12 ns	30	30	30	30	30
44	Max. DQS-DQ Skew tDQSQ	0.5 ns	32	32	32	32	32
45	X-Factor tQHS	0.75 ns	75	75	75	75	75
46-61	Superset Information	–	00	00	00	00	00
62	SPD Revision	Revision 0.0	00	00	00	00	00
63	Checksum for Bytes 0 - 62	–	99	B2	C4	B3	C5
64	Manufacturers JEDEC ID Code	–	C1	C1	C1	C1	C1
65-71	Manufacturer	–	INFINEON	INFINEON	INFINEON	INFINEON	INFINEON
72	Module Assembly Location	–					
73-90	Module Part Number	–					
91-92	Module Revision Code	–					
93-94	Module Manufacturing Date	–					
95-98	Module Serial Number	–					
99-127	–	–					
128-255	open for Customer use	–					

SPD Codes for PC2100 Modules "-7F"

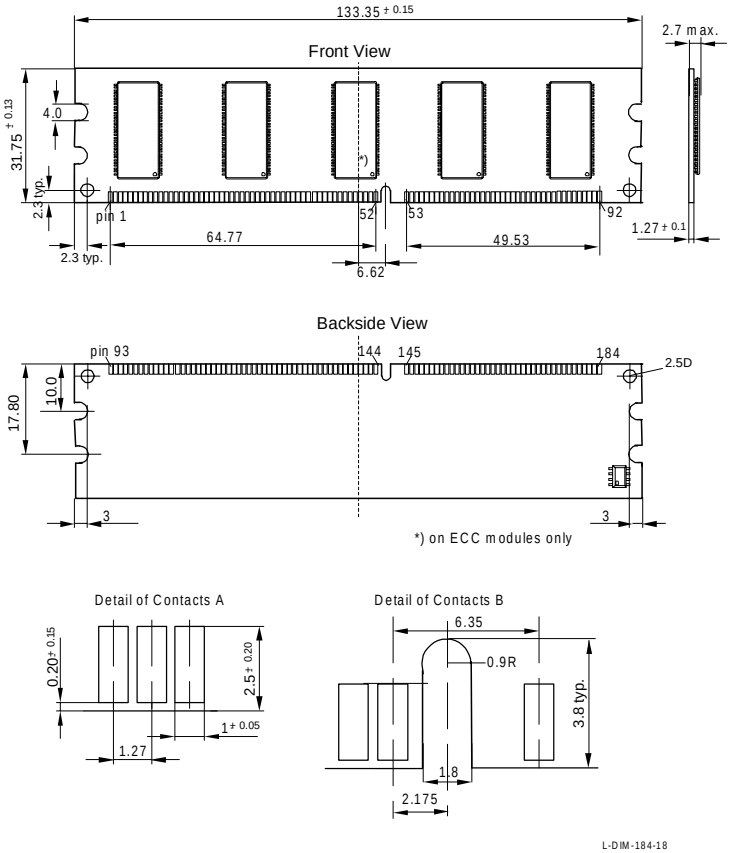
Byte#	Description		256MB x72 1bank -7	512MB x72 2bank -7
			HEX	HEX
0	Number of SPD Bytes	128	80	80
1	Total Bytes in Serial PD	256	08	08
2	Memory Type	DDR-SDRAM	07	07
3	Number of Row Addresses	13	0D	0D
4	Number of Column Addresses	9 / 10	0A	0A
5	Number of DIMM Banks	1 / 2	01	02
6	Module Data Width	x64 / x72	48	48
7	Module Data Width (cont'd)	0	00	00
8	Module Interface Levels	SSTL 2.5	04	04
9	SDRAM Cycle Time at CL = 2.5	7 ns	70	70
10	Access Time from Clock at CL = 2.5	0.75 ns	75	75
11	DIMM Config	non-ECC / ECC	02	02
12	Refresh Rate/Type	Self-Refresh, 7.8 ms	82	82
13	SDRAM Width, Primary	x16 / x8	08	08
14	Error Checking SDRAM Data Width	na / x8	08	08
15	Minimum Clock Delay for Back-to-Back Random Column Address	tccd = 1 CLK	01	01
16	Burst Length Supported	2, 4 & 8	0E	0E
17	Number of SDRAM Banks	4	04	04
18	Supported CAS Latencies	CAS latency = 2 & 2.5	0C	0C
19	CS Latencies	CS latency = 0	01	01
20	WE Latencies	Write latency = 1	02	02
21	SDRAM DIMM Module Attributes	unbuffered	20	20
22	SDRAM Device Attributes: General	–	C0	C0
23	Min. Clock Cycle Time at CAS Latency = 2	7.5 ns	75	75
24	Access Time from Clock for CL = 2	0.75 ns	75	75
25	Minimum Clock Cycle Time at CL = 1.5	not supported	00	00
26	Access Time from Clock at CL = 1.5	not supported	00	00
27	Minimum Row Precharge Time	15 ns	3C	3C
28	Minimum Row Act. to Row Act. Delay tRRD	15 ns	3C	3C
29	Minimum RAS to CAS Delay tRCD	15 ns	3C	3C
30	Minimum RAS Pulse Width tRAS	45 ns	2D	2D
31	Module Bank Density (per bank)	128MByte / 256MByte	40	40
32	Addr. and Command Setup Time	0.9 ns	90	90
33	Addr. and Command Hold Time	0.9 ns	90	90
34	Data Input Setup Time	0.5 ns	50	50
35	Data Input Hold Time	0.5 ns	50	50
36-40	Superset Information	–	00	00
41	Minimum Core Cycle Time tRC	60 ns	3C	3C
42	Min. Auto Refresh Cmd Cycle Time tRFC	75 ns	4B	4B
43	Maximum Clock Cycle Time tck	12 ns	30	30
44	Max. DQS-DQ Skew tDQSQ	0.5 ns	32	32
45	X-Factor tQHS	0.75 ns	75	75
46-61	Superset Information	–	00	00
62	SPD Revision	Revision 0.0	00	00
63	Checksum for Bytes 0 - 62	–	97	98
64	Manufacturers JEDEC ID Code	–	C1	C1
65-71	Manufacturer	–	INFINEON	INFINEON
72	Module Assembly Location	–		
73-90	Module Part Number	–		
91-92	Module Revision Code	–		
93-94	Module Manufacturing Date	–		
95-98	Module Serial Number	–		
99-127	–	–		
128-255	open for Customer use	–		

SPD Codes for PC2700 Modules "-6"

Byte#	Description		128MB x64 1bank -6	256MB x64 1bank -6	256MB x72 1bank -6	512MB x64 2bank -6	512MB x72 2bank -6
			HEX	HEX	HEX	HEX	HEX
0	Number of SPD Bytes	128	80	80	80	80	80
1	Total Bytes in Serial PD	256	08	08	08	08	08
2	Memory Type	DDR-SDRAM	07	07	07	07	07
3	Number of Row Addresses	13	0D	0D	0D	0D	0D
4	Number of Column Addresses	9 / 10	09	0A	0A	0A	0A
5	Number of DIMM Banks	1 / 2	01	01	01	02	02
6	Module Data Width	x64 / x72	40	40	48	40	48
7	Module Data Width (cont'd)	0	00	00	00	00	00
8	Module Interface Levels	SSTL_2.5	04	04	04	04	04
9	SDRAM Cycle Time at CL = 2.5	6 ns	60	60	60	60	60
10	Access Time from Clock at CL = 2.5	0.70 ns	70	70	70	70	70
11	DIMM Config	non-ECC / ECC	00	00	02	00	02
12	Refresh Rate/Type	Self-Refresh, 7.8 ms	82	82	82	82	82
13	SDRAM Width, Primary	x16 / x8	10	08	08	08	08
14	Error Checking SDRAM Data Width	na / x8	00	00	08	00	08
15	Minimum Clock Delay for Back-to-Back Random Column Address	tccd = 1 CLK	01	01	01	01	01
16	Burst Length Supported	2, 4 & 8	0E	0E	0E	0E	0E
17	Number of SDRAM Banks	4	04	04	04	04	04
18	Supported CAS Latencies	CAS latency = 2 & 2.5	0C	0C	0C	0C	0C
19	CS Latencies	CS latency = 0	01	01	01	01	01
20	WE Latencies	Write latency = 1	02	02	02	02	02
21	SDRAM DIMM Module Attributes	unbuffered	20	20	20	20	20
22	SDRAM Device Attributes: General	–	C0	C0	C0	C0	C0
23	Min. Clock Cycle Time at CAS Latency = 2	7.5 ns	75	75	75	75	75
24	Access Time from Clock for CL = 2	0.70 ns	70	70	70	70	70
25	Minimum Clock Cycle Time at CL = 1.5	not supported	00	00	00	00	00
26	Access Time from Clock at CL = 1.5	not supported	00	00	00	00	00
27	Minimum Row Precharge Time	18 ns	48	48	48	48	48
28	Minimum Row Act. to Row Act. Delay tRRD	12 ns	30	30	30	30	30
29	Minimum RAS to CAS Delay tRCD	18 ns	48	48	48	48	48
30	Minimum RAS Pulse Width tRAS	42 ns	2A	2A	2A	2A	2A
31	Module Bank Density (per bank)	128MByte / 256MByte	20	40	40	40	40
32	Addr. and Command Setup Time	0.75 ns	75	75	75	75	75
33	Addr. and Command Hold Time	0.75 ns	75	75	75	75	75
34	Data Input Setup Time	0.45 ns	45	45	45	45	45
35	Data Input Hold Time	0.45 ns	45	45	45	45	45
36-40	Superset Information	–	00	00	00	00	00
41	Minimum Core Cycle Time tRC	60 ns	3C	3C	3C	3C	3C
42	Min. Auto Refresh Cmd Cycle Time tRFC	72 ns	48	48	48	48	48
43	Maximum Clock Cycle Time tck	12 ns	30	30	30	30	30
44	Max. DQS-DQ Skew tDQSQ	0.45 ns	2D	2D	2D	2D	2D
45	X-Factor tQHS	0.55 ns	55	55	55	55	55
46-61	Superset Information	–	00	00	00	00	00
62	SPD Revision	Revision 0.0	00	00	00	00	00
63	Checksum for Bytes 0 - 62	–	E7	00	12	01	13
64	Manufacturers JEDEC ID Code	–	C1	C1	C1	C1	C1
65-71	Manufacturer	–	INFINEON	INFINEON	INFINEON	INFINEON	INFINEON
72	Module Assembly Location	–					
73-90	Module Part Number	–					
91-92	Module Revision Code	–					
93-94	Module Manufacturing Date	–					
95-98	Module Serial Number	–					
99-127	–	–					
128-255	open for Customer use	–					

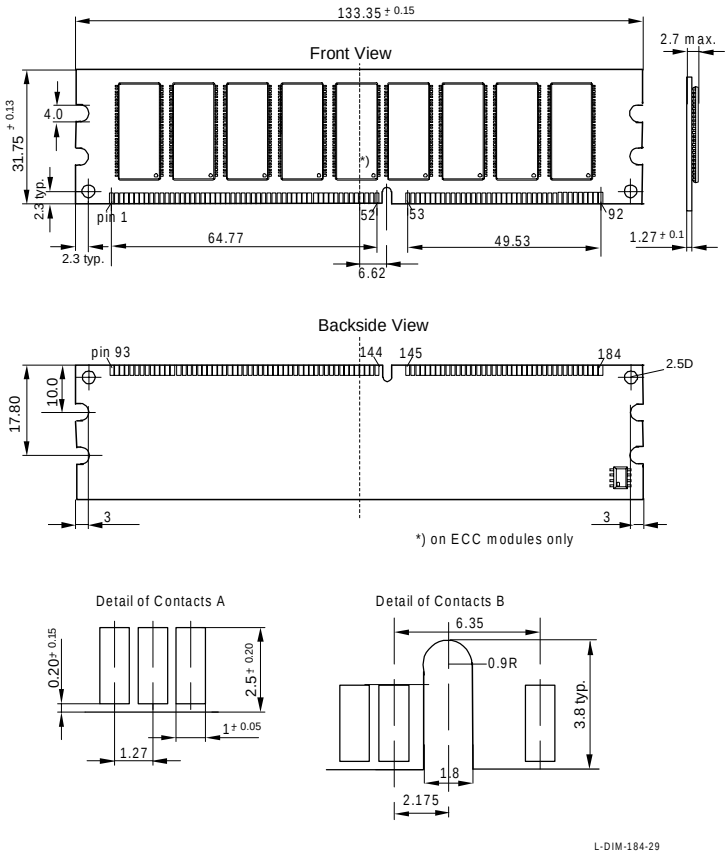
Package Outlines - Raw Card C (One Bank Modules)

DDR-SDRAM DIMM Module Package



Package Outlines -Raw Card A (One Bank Modules)

DDR-SDRAM DIMM Module Package



Package Outlines - Raw Card B (Two Bank Modules)

DDR-SDRAM DIMM Module Package

two bank modules