6A DC/DC µModule Regulator with Tracking and Frequency Synchronization

FEATURES

- **Complete Standalone Power Supply**
- **Wide Input Voltage Range: 4.5V to 26.5V**
- **6A DC Typical, 8A Peak Output Current**
- **0.8V to 5V Output**
- **Output Voltage Tracking**
- **±1.75% Maximum Total DC Error**
- **Current Mode Control/Fast Transient Response**
- **Phase-Lockable Fixed Frequency 250kHz to 780kHz**
- **On-Board Frequency Synchronization**
- **Selectable Burst Mode® Operation**
- Power Good Voltage Indicator
- Output Overvoltage Protection
- Output Current Foldback Limiting
- 9mm × 15mm × 4.32mm LGA Package

APPLICATIONS

- Telecom and Networking Equipment
- Servers
- Storage Cards
- ATCA Cards
- Industrial Equipment
- Point of Load Regulation
- Medical Systems

DESCRIPTION

The LTM®4618 is a complete 6A output switching mode DC/DC power supply in a 9mm × 15mm × 4.32mm LGA package. Included in the package are the switching controller, power FETs, inductor and all support components. Operating over an input voltage range of 4.5V to 26.5V, the LTM4618 supports an output voltage range of 0.8V to 5V set by a single external resistor. Its high efficiency design delivers 6A continuous current (8A peak). Only a few input and output capacitors are needed.

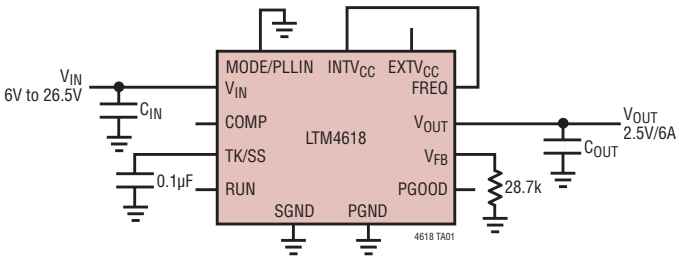
High switching frequency and a current mode architecture enable a very fast transient response to line and load changes without sacrificing stability. The device supports frequency synchronization and output voltage tracking for supply rail sequencing. Burst Mode operation or pulse-skipping mode can be selected for light load operations.

Fault protection features include overvoltage protection, overcurrent protection and foldback current limit for short-circuit protection.

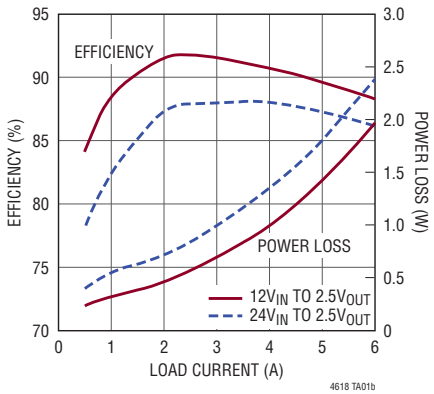
The LTM4618 is Pb-free and RoHS compliant.

TYPICAL APPLICATION

2.5V/6A DC/DC Power µModule® with 6V to 26.5V Input



Efficiency and Power Loss vs Load Current

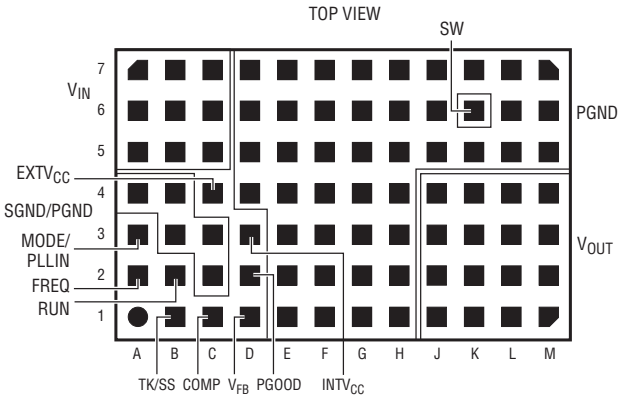


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, SW ..... –0.3V to 28V
$INTV_{CC}$, RUN, $EXTV_{CC}$, PGOOD ..... –0.3V to 6V
COMP, V_{FB} ..... –0.3V to 2.7V
MODE/PLLIN, TK/SS, FREQ ..... –0.3V to $INTV_{CC}$
V_{OUT} ..... 0.8V to 5V
Operating Junction Temperature Range (Note 2) ..... –40°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Peak Package Body Temperature ..... 250°C

PIN CONFIGURATION



LGA PACKAGE
84-LEAD (15mm × 9mm × 4.32mm)
Θ_{JA} = 16°C/W, Θ_{JCtop} = 15°C/W, $\Theta_{JCbottom}$ = 4°C/W, WEIGHT = 2.3g,
$\theta_{JB} + \theta_{BA}$ = 16°C/W, θ_{BA} = BOARD-TO-AMBIENT RESISTANCE,
θ VALUES DEFINED PER JESD51-12

ORDER INFORMATION

LEAD FREE FINISH	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTM4618EV#PBF	LTM4618V	84-Lead (15mm × 9mm × 4.32mm) LGA	–40°C to 125°C
LTM4618IV#PBF	LTM4618V	84-Lead (15mm × 9mm × 4.32mm) LGA	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{IN} = 12V, per typical application in Figure 21.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN(DC)}$	Input DC Voltage	(Note 5)	●	4.5		26.5	V
$V_{OUT(DC)}$	Output Voltage Total Variation with Line and Load	C_{IN} = 10µF ×2, R_{FB} = 28.0kΩ C_{OUT} = 100µF ×3 X7R Ceramic MODE/PLLIN = 0V, V_{FREQ} = 2.4V V_{IN} = 6V to 26.5V, I_{OUT} = 0A to 6A (Note 4)	●	2.476	2.52	2.557	V
Input Specifications							
$V_{IN(UVLO)}$	Undervoltage Lockout Thresholds	V_{INTVCC} Rising V_{INTVCC} Falling		2.00 1.85	2.20 2.00	2.35 2.15	V V
$I_{INRUSH(VIN)}$	Input Inrush Current at Start-Up	I_{OUT} = 0A, C_{IN} = 10µF ×2, C_{OUT} = 100µF ×3 V_{OUT} = 2.5V V_{IN} = 12V V_{IN} = 26.5V			 0.3 0.2		 A A

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{IN} = 12V, per typical application in Figure 21.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{Q(VIN)}$	Input Supply Bias Current	V_{IN} = 12V, V_{OUT} = 2.5V, I_{OUT} = 0A V_{IN} = 26.5V, V_{OUT} = 2.5V, I_{OUT} = 0A Shutdown, RUN = 0, V_{IN} = 26.5V			26 20 80		mA mA µA
$I_{S(VIN)}$	Input Supply Current	V_{IN} = 12V, V_{OUT} = 2.5V, I_{OUT} = 6A V_{IN} = 26.5V, V_{OUT} = 2.5V, I_{OUT} = 6A			1.430 0.675		A A
$INTV_{CC}$	Internal V_{CC} Voltage	V_{IN} = 12V, V_{RUN} > 2V, No Load		4.8	5	5.2	V
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	$EXTV_{CC}$ Ramping Positive	●	4.5	4.7		V
VLDO External	$EXTV_{CC}$ Voltage Drop	$INTV_{CC}$ = 20mA, V_{EXTVCC} = 5V			50	100	mV
V_{EXTVCC} Hysteresis	$EXTV_{CC}$ Hysteresis				200		mV
Output Specifications							
$I_{OUT(DC)}$	Output Continuous Current Range	V_{IN} = 12V, V_{OUT} = 2.5V (Note 4)		0		6	A
$\frac{\Delta V_{OUT(LINE)}}{V_{OUT}}$	Line Regulation Accuracy	V_{OUT} = 2.5V, V_{IN} from 6V to 26.5V I_{OUT} = 0A	●		0.02	0.04	%/V
$\frac{\Delta V_{OUT(LOAD)}}{V_{OUT}}$	Load Regulation Accuracy	V_{IN} = 12V, V_{OUT} = 2.5V, 0 to 6A (Note 4)	●		0.3	0.6	%
$V_{OUT(AC)}$	Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 100µF ×3 X5R Ceramic V_{IN} = 12V, V_{OUT} = 2.5V V_{IN} = 26.5V, V_{OUT} = 2.5V			 10 12		 mV mV
f_S	Output Ripple Voltage Frequency	I_{OUT} = 2A, V_{IN} = 12V, V_{OUT} = 2.5V, V_{FREQ} = $INTV_{CC}$			780		kHz
$\Delta V_{OUT(START)}$	Turn-On Overshoot	C_{OUT} = 100µF ×3 X5R Ceramic V_{OUT} = 2.5V, I_{OUT} = 0A V_{IN} = 12V V_{IN} = 26.5V			 20 20		 mV mV
t_{START}	Turn-On Time	C_{OUT} = 100µF ×3 X5R Ceramic, V_{OUT} = 2.5V, I_{OUT} = 0A, TK/SS Capacitor = 0.01µF V_{IN} = 12V V_{IN} = 26.5V			 0.75 0.70		 ms ms
ΔV_{OUTLS}	Peak Deviation for Dynamic Load	Load: 0% to 50% of Full Load C_{OUT} = 100µF ×3 X5R Ceramic, V_{OUT} = 2.5V V_{IN} = 12V			 15		 mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 50% of Full Load C_{OUT} = 100µF ×3 X5R Ceramic, V_{OUT} = 2.5V V_{IN} = 12V			 10		 µs
$I_{OUT(PK)}$	Output Current Limit	C_{OUT} = 100µF ×3 X5R Ceramic V_{IN} = 6V, V_{OUT} = 2.5V V_{IN} = 26.5V, V_{OUT} = 2.5V			 11 11		 A A
Control Section							
V_{FB}	Error Amplifier Feedback Voltage	I_{OUT} = 0A, V_{OUT} = 2.5V	 ●	0.792 0.788	0.8 0.8	0.808 0.808	V V
I_{FB}	Error Amplifier Feedback Current	(Note 3)			–10	–50	nA
V_{OVL}	Feedback Voltage Lockout	Measured at V_{FB}		0.84	0.86	0.88	V
$I_{TK/SS}$	Soft-Start Charge Current	$V_{TK/SS}$ = 0V		0.9	1.3	1.7	µA
DF_{MAX}	Maximum Duty Factor	In Dropout (Note 3)			97		%
$t_{ON(MIN)}$	Minimum On-Time	(Note 3)			90		ns
f_{NOM}	Nominal Frequency	V_{FREQ} = 1.2V		450	500	550	kHz
f_{LOW}	Lowest Frequency	V_{FREQ} = 0V		210	250	290	kHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{IN} = 12V, per typical application in Figure 21.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{HIGH}	Highest Frequency	$V_{FREQ} \geq$ 2.4V, $INTV_{CC}$		700	780	860	kHz
$V_{IH(MODE/PLLIN)}$	Synchronous Clock High Level			2.0			V
$V_{IL(MODE/PLLIN)}$	Synchronous Clock Low Level					0.8	V
$R_{MODE/PLLIN}$	MODE/PLLIN Input Resistance				250		kΩ
I_{FREQ}	FREQ Pin Sinking Current Sourcing Current	 $f_{MODE/PLLIN} > f_{OSC}$ $f_{MODE/PLLIN} < f_{OSC}$			 –13 13		 µA µA
V_{RUN}	RUN Pin On Threshold	RUN Rising		1.1	1.22	1.35	V
V_{RUN} Hysteresis	RUN Pin Hysteresis				120		mV
R_{FBHI}	Resistor Between V_{OUT} and V_{FB} Pins			60.1	60.4	60.7	kΩ
PGOOD Output							
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.1	0.3	V
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 5V				±2	µA
V_{PG}	PGOOD Trip Level	V_{FB} with Respect to Set Regulated Voltage V_{FB} Ramping Negative V_{FB} Ramping Positive		 –5 5	 –7.5 7.5	 –10 10	 % %

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4618 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4618E is guaranteed to meet performance specifications over the 0°C to 125°C operating junction temperature range. Specifications over the full –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4618I is guaranteed to meet specifications over the full operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

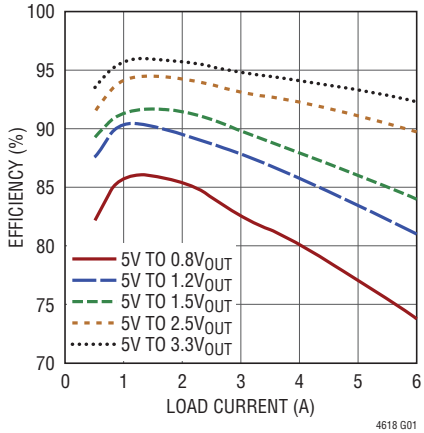
Note 3: 100% tested at wafer level only.

Note 4: See Output Current Derating curves for different V_{IN}, V_{OUT} and T_A.

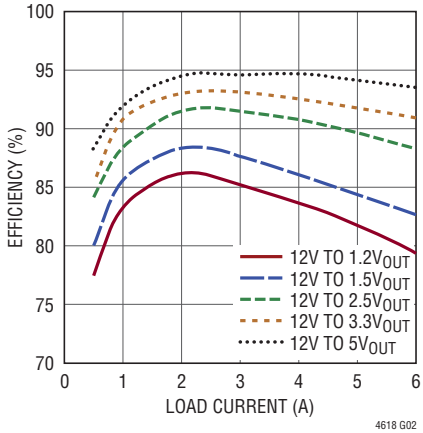
Note 5: For input voltages less than 6V, tie the V_{IN}, $INTV_{CC}$ and $EXTV_{CC}$ together. The LTM4618 will operate from 5V inputs, but V_{IN}, $INTV_{CC}$ and $EXTV_{CC}$ need to be tied together.

TYPICAL PERFORMANCE CHARACTERISTICS

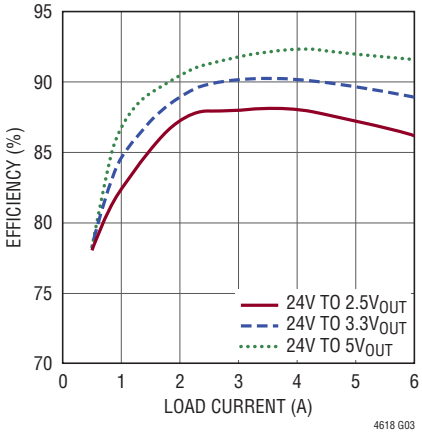
Efficiency vs Load Current with $5V_{IN}$ (CCM)



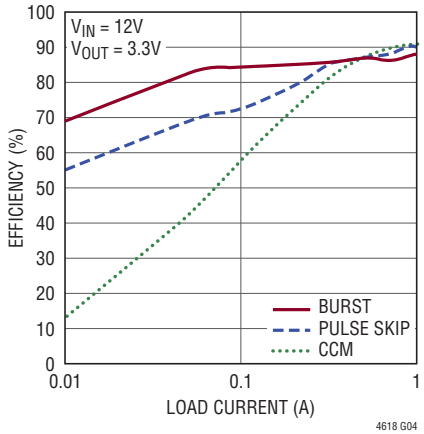
Efficiency vs Load Current with $12V_{IN}$ (CCM)



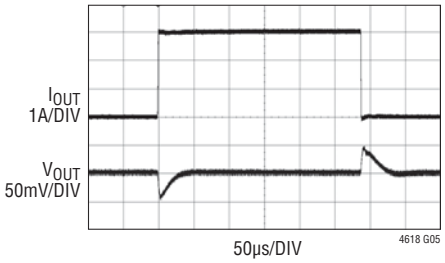
Efficiency vs Load Current with $24V_{IN}$ (CCM)



Efficiency vs Load Current with Different Mode Settings (12V to 3.3V)

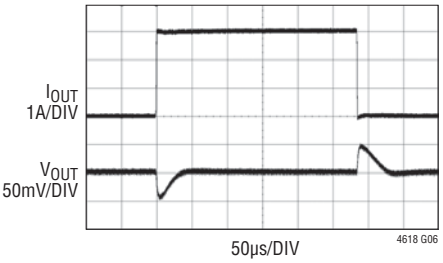


1.2V Transient Response



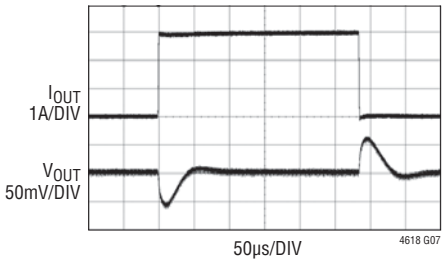
V_{IN} = 12V AND V_{OUT} = 1.2V AT 3A/µs LOAD STEP
C_{OUT} = 2× 22µF 6.3V CERAMIC CAPACITOR
1× 100µF 6.3V CERAMIC CAPACITOR
1× 220µF SANYO POSCAP

1.5V Transient Response



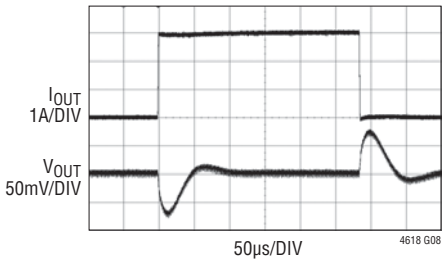
V_{IN} = 12V AND V_{OUT} = 1.5V AT 3A/µs LOAD STEP
C_{OUT} = 2× 22µF 6.3V CERAMIC CAPACITOR
1× 100µF 6.3V CERAMIC CAPACITOR
1× 220µF SANYO POSCAP

2.5V Transient Response



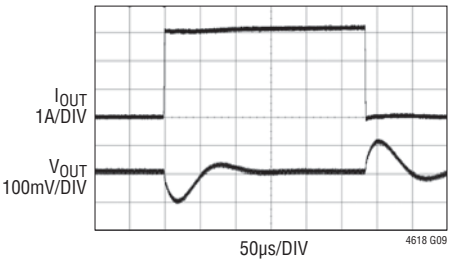
V_{IN} = 12V AND V_{OUT} = 2.5V AT 3A/µs LOAD STEP
C_{OUT} = 2× 22µF 6.3V CERAMIC CAPACITOR
1× 100µF 6.3V CERAMIC CAPACITOR
1× 220µF SANYO POSCAP

3.3V Transient Response



V_{IN} = 12V AND V_{OUT} = 3.3V AT 3A/µs LOAD STEP
C_{OUT} = 2× 22µF 6.3V CERAMIC CAPACITOR
1× 100µF 6.3V CERAMIC CAPACITOR
1× 220µF SANYO POSCAP

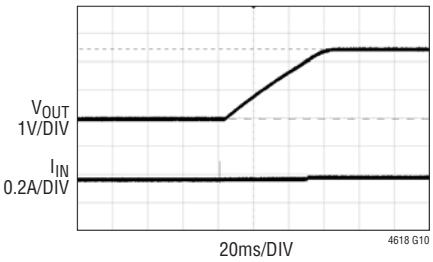
5V Transient Response



V_{IN} = 12V AND V_{OUT} = 5V AT 3A/µs LOAD STEP
C_{OUT} = 2× 22µF 6.3V CERAMIC CAPACITOR
1× 100µF 6.3V CERAMIC CAPACITOR
1× 220µF SANYO POSCAP

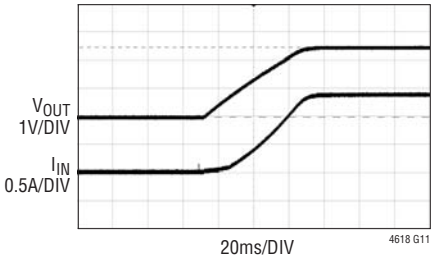
TYPICAL PERFORMANCE CHARACTERISTICS

Start-Up, I_{OUT} = 0A



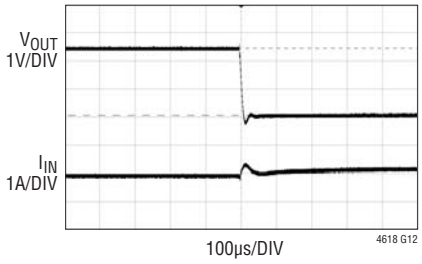
V_{IN} = 12V AND V_{OUT} = 2.5V
C_{OUT} = 2× 22µF 6.3V CERAMIC,
1× 100µF 6.3V CERAMIC AND
1× 220µF SANYO POSCAP
$C_{SOFT-START}$ = 0.1µF

Start-Up, I_{OUT} = 6A



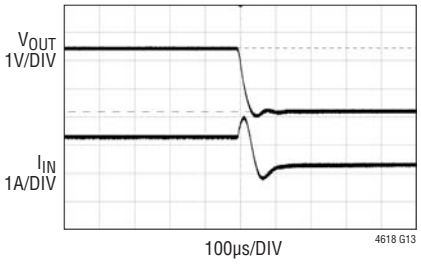
V_{IN} = 12V AND V_{OUT} = 2.5V
C_{OUT} = 2× 22µF 6.3V CERAMIC,
1× 100µF 6.3V CERAMIC AND
1× 220µF SANYO POSCAP
$C_{SOFT-START}$ = 0.1µF

Short-Circuit Protection, I_{OUT} = 0A



V_{IN} = 12V AND V_{OUT} = 2.5V
C_{OUT} = 2× 22µF 6.3V CERAMIC,
1× 100µF 6.3V CERAMIC AND
1× 220µF SANYO POSCAP

Short-Circuit Protection, I_{OUT} = 6A



V_{IN} = 12V AND V_{OUT} = 2.5V
C_{OUT} = 2× 22µF 6.3V CERAMIC,
1× 100µF 6.3V CERAMIC AND
1× 220µF SANYO POSCAP

PIN FUNCTIONS

NC (A1): No Connect. Leave floating.

FREQ (A2): Frequency Selection Pin. An internal low pass filter is tied to this pin. The frequency can be selected from 250kHz to 780kHz by setting a voltage from this pin to SGND. A programming resistor divider can be used to set the operating frequency. See the Applications Information section.

MODE/PLLIN (A3): Mode Selection or External Synchronization Pin. Tying this pin to $INTV_{CC}$ enables pulse-skipping operation. Tying this pin low enables forced continuous mode operation. Burst Mode operation is enabled by floating the pin. A clock on the pin will force the controller into forced continuous mode of operation and synchronize to the internal oscillator. The programming DC voltage has to be removed for clock synchronization.

PGND (BANK 2: A4, B4, D4-D7, E1-E7, F1-F7, G1-G7, H1-H7, J5-J7, K5, K7, L5-L7, M5-M7): Power ground pins for both input and output returns.

V_{IN} (BANK 1: A5-A7, B5-B7, C5-C7): Power Input Pins. Apply input voltage between these pins and PGND pins. Recommend placing input decoupling capacitance directly between V_{IN} pins and PGND pins.

TK/SS (B1): Output Voltage Tracking and Soft-Start Pin. An internal soft-start current of 1.3µA charges the soft-start capacitor. See the Applications Information section.

RUN (B2): Run Control Pin. A voltage above 1.35V on this pin turns on the module. Forcing this pin below 1.1V will shut down the output. The RUN pin has a 1µA pull-up current source that increases to 10µA as the RUN pin voltage reaches 1.5V and up to compliance. Therefore the pin can be left floating for normal operation. A maximum of 6V can be applied to the pin. A voltage divider can be used for a UVLO function. See the Applications Information section.

SGND (B3, C2 and C3): Signal Ground Pin. Return ground path for all analog and low power circuitry. Tie a single connection to PGND. See applications for details.

COMP (C1): Current control threshold and error amplifier compensation point. The module has been internally compensated for most I/O ranges.

$EXTV_{CC}$ (C4): External Voltage Input. Bypasses the internal $INTV_{CC}$ LDO and powers the internal circuitry and MOSFET drivers. If a 5V source is available, the internal LDO is disabled, and the power dissipation is lower, especially at higher input voltages. See the Applications Information section.

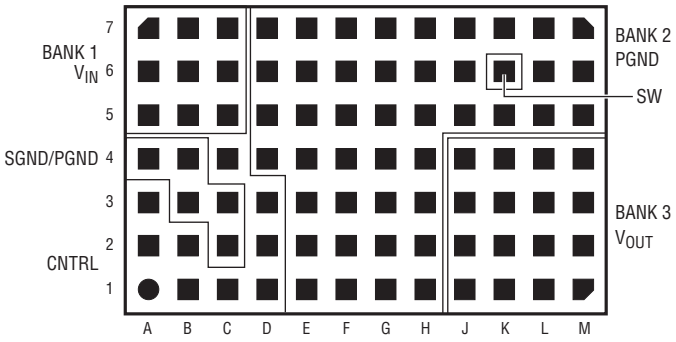
V_{FB} (D1): The negative input of the error amplifier. Internally, this pin is connected to V_{OUT} with a 60.4kΩ precision resistor. Different output voltages can be programmed with an additional resistor between V_{FB} and SGND pins. See applications for details.

PGOOD (D2): Output Voltage Power Good Indicator. Open-drain logic output that is pulled to ground when the output voltage is not within ±7.5% of the regulation point.

$INTV_{CC}$ (D3): Internal 5V Regulator Output. This pin is for additional decoupling of the 5V internal regulator.

V_{OUT} (BANK 3: J1-J4, K1-K4, L1-L4, M1-M4): Power Output Pins. Apply output load between these pins and PGND pins. Recommend placing output decoupling capacitance directly between these pins and PGND pins.

SW (K6): Switching Node of the Circuit. This pin is used to check the switching frequency. Leave pin floating. A resistor-capacitor snubber can be placed from SW to PGND to eliminate high frequency switch node ringing. See the Applications Information section.



SIMPLIFIED BLOCK DIAGRAM

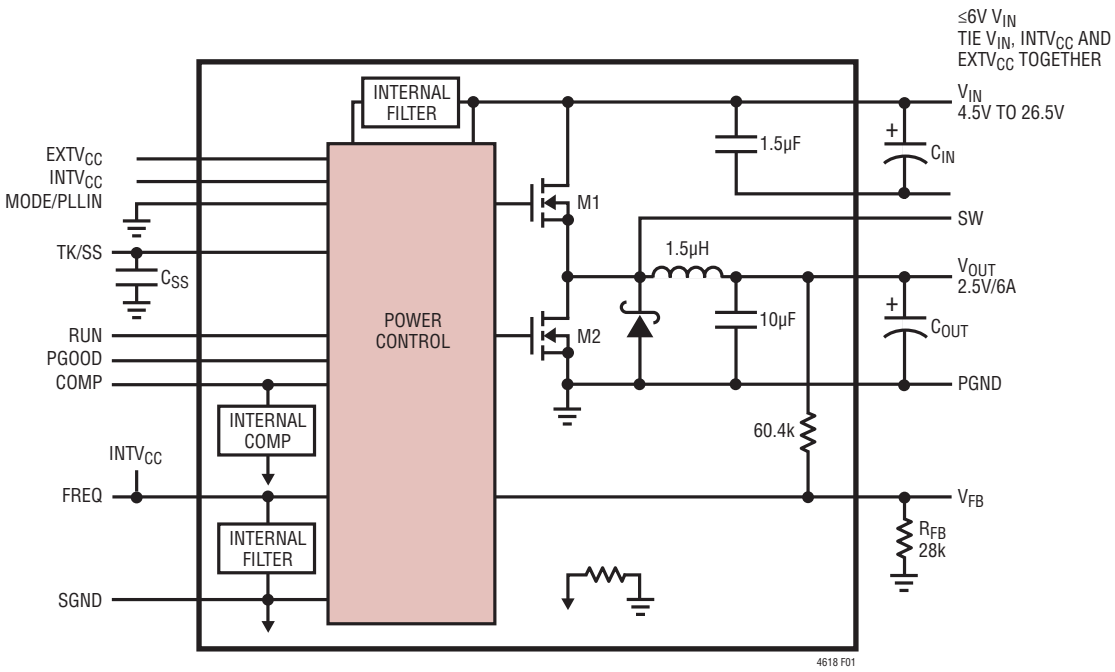


Figure 1. Simplified LTM4618 Block Diagram

DECOUPLING REQUIREMENTS

T_A = 25°C. Use Figure 1 configuration.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
C_{IN}	External Input Capacitor Requirement (V_{IN} = 4.5V to 26.5V, V_{OUT} = 2.5V)	I_{OUT} = 6A		10			µF
C_{OUT}	External Output Capacitor Requirement (V_{IN} = 4.5V to 26.5V, V_{OUT} = 2.5V)	I_{OUT} = 6A			200		µF

OPERATION

Power Module Description

The LTM4618 is a standalone non-isolated switching mode DC/DC power supply. It can deliver up to 6A (DC current) output with few external input and output capacitors. This module provides precisely regulated output voltages programmable via external resistors from 0.8VDC to 5.0VDC over 4.5V to 26.5V input voltages. The typical application schematic is shown in Figure 21. For ≤6V inputs, connect V_{IN}, $INTV_{CC}$ and $EXTV_{CC}$ together.

The LTM4618 has an integrated constant frequency current mode regulator and built-in power MOSFET devices with fast switching speed. The typical switching frequency is 750kHz.

With current mode control and internal feedback loop compensation, the LTM4618 module has sufficient stability margins and good transient performance with a wide range of output capacitors, even with all ceramic output capacitors.

Current mode control provides cycle-by-cycle fast current limit and current foldback in a short-circuit condition. Pulling the RUN pin below 1.1V forces the controller into its shutdown state, by turning off both MOSFETs. The TK/SS pin can be used for programming the output voltage ramp and voltage tracking during start-up. See the Applications Information section.

The LTM4618 is internally compensated to be stable over all operating conditions. The Linear Technology µModule Power Design Tool will be provided for transient and stability analysis. The V_{FB} pin is used to program the output voltage with a single external resistor to ground. Multiphase operation can be easily employed with the synchronization control.

High efficiency at light loads can be accomplished with selectable Burst Mode or pulse-skipping mode operations using the MODE/PLLIN pin. Efficiency graphs are provided for light load operation in the Typical Performance Characteristics section.

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The typical LTM4618 application circuit is shown in Figure 21. External component selection is primarily determined by the maximum load current and output voltage.

V_{IN} to V_{OUT} Step-Down Ratios

There are restrictions in the maximum V_{IN} to V_{OUT} step-down ratio that can be achieved for a given input voltage. One of the restrictions is the minimum on-time $t_{ON(MIN)}$, which is the smallest time duration that the LTM4618 can operate. Make sure that the operating on-time is larger than the minimum on-time as shown in the equation below. See the Thermal Considerations and Output Current Derating sections in this data sheet for the current restrictions. $t_{ON(MIN)}$ is approximately 90ns, guardband to 110ns.

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN} \bullet f}$$

Output Voltage Programming

The PWM controller has an internal 0.8V reference voltage. As shown in the Block Diagram, a 60.4k internal feedback resistor connects V_{OUT} to the V_{FB} pin. Adding a resistor R_{FB} from the V_{FB} pin to SGND programs the output voltage:

$$V_{OUT} = 0.8V \bullet \frac{60.4k + R_{FB}}{R_{FB}}$$

Table 1. V_{FB} Resistor Table vs Various Output Voltages

V_{OUT} (V)	0.8	1	1.2	1.5	1.8	2.5	3.3	5
R_{FB} (kΩ)	Open	243	121	69.8	48.7	28.7	19.1	11.5

Input Capacitors

The LTM4618 module should be connected to a low AC-impedance DC source. One 1.5µF input ceramic capacitor is included inside the module. Additional input capacitors are only needed if a large load step is required up to the 6A level. A 47µF to 100µF surface mount aluminum electrolytic bulk capacitor can be used for more input bulk capacitance. This bulk input capacitor is only needed if the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. If low impedance power planes are used, then this 47µF capacitor is not needed.

For a buck converter, the switching duty-cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Without considering the inductor current ripple, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta} \bullet \sqrt{D \bullet (1-D)}$$

In the above equation, η is the estimated efficiency of the power module. One 10µF ceramic input capacitor is typically rated for 2A of RMS ripple current, so the RMS input current at the worst case 6A maximum current is about 3A. If a low inductance plane is used to power the device, then two 10µF ceramic capacitors are enough for the output at 6A load and no external input bulk capacitor is required. The input RMS ripple current can be cancelled by paralleling multiple LTM4618 power modules out of phase, allowing the use of fewer input capacitors. Application Note 77 explains the details.

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Output Capacitors

The LTM4618 is designed for low output voltage ripple noise. The bulk output capacitors defined as C_{OUT} are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be a low ESR tantalum capacitor, a low ESR polymer capacitor or ceramic capacitor. The typical output capacitance range is from 100µF to 300µF. Additional output filtering may be required by the system designer if further reduction of output ripple or dynamic transient spikes is required. Table 4 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 3A/µs transient. The table optimizes the total equivalent ESR and total bulk capacitance to optimize the transient performance. Stability criteria are considered in the Table 4 matrix, and the Linear Technology µModule Power Design Tool is available for stability analysis. Multiphase operation will reduce effective output ripple as a function of the number of phases. Application Note 77 discusses this noise reduction versus output ripple current cancellation, but the output capacitance should be considered carefully as a function of stability and transient response. The Linear Technology µModule Power Design Tool can calculate the output ripple reduction as the number of implemented phases increases by N times.

Mode Selections and Phase-Locked Loop

The LTM4618 can be enabled to enter high efficiency Burst Mode operation, constant-frequency, pulse-skipping mode, or forced continuous conduction mode. To select the forced continuous operation, tie the MODE/PLLIN pin to ground. To select pulse-skipping mode of operation, tie the MODE/PLLIN pin to $INTV_{CC}$. To select Burst Mode operation, float the pin.

A phase-locked loop (PLL) is available on the LTM4618 to synchronize the internal oscillator to an external clock source that is connected to the MODE/PLLIN pin. The incoming clock should be applied before the regulator's RUN pin is enabled.

Frequency Selection

The switching frequency of the LTM4618's controller can be selected using a DC voltage. If the MODE/PLLIN pin is not being driven by an external clock source, the FREQ pin can program the controller's operating frequency from 250kHz to 780kHz by connecting a resistor divider as shown in Figure 21. The typical frequency is 750kHz. But if the minimum on-time is reached, a lower frequency needs to be set to increase the turn-on time. Otherwise, a significant amount of cycle skipping can occur with correspondingly larger ripple current and voltage ripple.

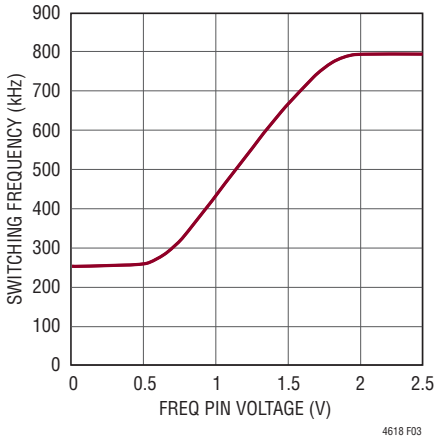

Figure 3. Relationship Between Switching Frequency and Voltage at the FREQ Pin

Frequency Synchronization

The MODE/PLLIN pin allows the LTM4618 to be synchronized to an external clock (between 400kHz to 780kHz) and the internal phase-locked loop allows the LTM4618 to lock onto input clock phase as well. The FREQ pin has the onboard loop filter for the PLL. The incoming clock must be applied before the RUN pin is enabled. For applications powering the clock source from the LTM4618's $INTV_{CC}$, the RUN pin has to be enabled in order to activate $INTV_{CC}$ for the clock source. In this situation (see Figure 22) the TK/SS pin can be used to soft-start the regulator for 100ms using a ≈ 0.22µF capacitor. This will allow the regulator to synchronize to the right frequency before the regulator's inductor ripple current peaks.

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The LTM4618 can be synchronized from 400kHz to 780kHz with an input clock that has a high level above 2.0V and a low level below 0.8V. The 400kHz low end operation limit is put in place to limit inductor ripple current. See the Typical Applications section for synchronization examples. The LTM4618 minimum on-time is limited to about 90ns. Guardband the on-time to 110ns. The on-time can be calculated as:

$$t_{ON(MIN)} = \frac{1}{FREQ} \bullet \left(\frac{V_{OUT}}{V_{IN}} \right)$$

Soft-Start and Tracking

LTM4618 has the ability to either soft-start by itself with a capacitor or track the output of an external supply. When the module is configured to soft-start by itself, a capacitor should be connected to its TK/SS pin. When the module is in the shutdown state, the TK/SS pin is actively pulled to ground.

Once the RUN pin voltage is above 1.22V, the module powers up. Then a soft-start current of 1.3µA starts to charge its soft-start capacitor. Note that soft-start or tracking is achieved not by limiting the maximum output current of the controller but by controlling the output ramp voltage according to the ramp rate on the TK/SS pin. Current foldback is disabled during this phase to ensure smooth soft-start or tracking. The soft-start or tracking range is defined as the voltage range from 0V to 0.8V on the TK/SS pin. The total soft-start time can be calculated as:

$$t_{SOFT\text{-}START} = \frac{0.8V \bullet C_{SS}}{1.3\mu A}$$

Output voltage tracking can be programmed externally using the TK/SS pin. The master voltage is divided down with an external resistor divider that is the same as the slave's feedback divider to implement coincident tracking. The LTM4618 uses an accurate 60.4k resistor internally for the top feedback resistor. Figure 4 shows an example of coincident tracking.

$$V_{OUT(SLAVE)} = \left(1 + \frac{R1}{R2}\right) \bullet V_{TRACK}$$

V_{TRACK} is the track ramp applied to the slave's TK/SS pin. V_{TRACK} has a control range of 0V to 0.8V. When the master's output is divided down with the same resistor values used to set the slave's output, then the slave will coincident track with the master until it reaches its final value. The master will continue to its final value from the slave's regulation point.

Ratiometric modes of tracking can be achieved by selecting different divider resistor values to change the output tracking ratio. The master output must be greater than the slave output for the tracking to work. Master and slave data inputs can be used to implement the correct resistor values for coincident or ratio tracking.

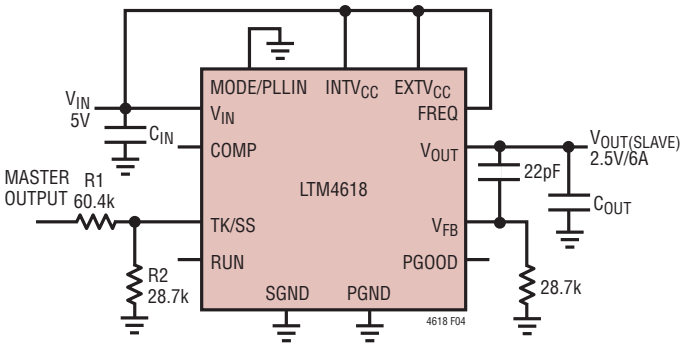

Figure 4. Output Voltage Coincident Tracking

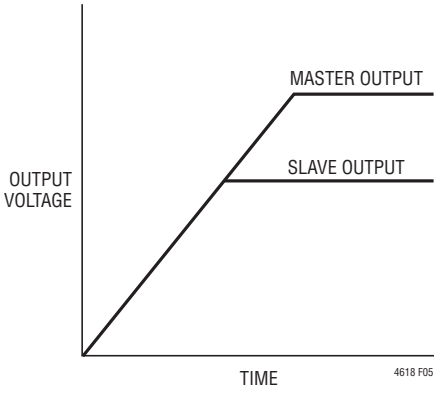

Figure 5. Coincident Tracking Characteristics

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Slope Compensation

The module has already been internally compensated for all output voltages. The Linear Technology µModule Power Design Tool will be provided for other control loop optimization.

RUN Pin

The RUN pin has a 1µA pull-up current source that will enable the device in a float condition. A voltage divider can be used to enable a UVLO function using the RUN pin. See Figure 21.

Fault Conditions: Current Limit and Overcurrent Foldback

The LTM4618 has a current mode controller, which inherently limits the cycle-by-cycle inductor current not only in steady-state operation, but also in transient.

To further limit current in the event of an overload condition, the LTM4618 provides foldback current limiting. If the output voltage falls by more than 40%, then the maximum output current is progressively lowered to about 25% of its full current limit value.

Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD51-9 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board—also defined by JESD51-9 ("Test Boards for Area Array Surface Mount Package Thermal Measurements"). The motivation for providing these thermal coefficients in found in JESD 51-12 ("Guidelines for Reporting and Using Electronic Package Thermal Information").

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to anticipate the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are in-and-of themselves not relevant to providing guidance of thermal performance; instead, the derating curves provided in the data sheet can be used in a manner that yields insight and guidance pertaining to one's application-usage, and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section shows four thermal coefficients explicitly defined in JESD 51-12; these coefficients are quoted or paraphrased below:

- θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.
- $\theta_{JCbottom}$, the thermal resistance from junction to the bottom of the product case, is the junction-to-board thermal resistance with all of the component power dissipation flowing through the bottom of the package. In the typical µModule, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.
- θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.
- θ_{JB}, the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule and into the board, and

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is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured at specified distance from the package, using a two sided, two layer board. This board is described in JESD 51-9.

A graphical representation of the forementioned thermal resistances is given in Figure 6; blue resistances are contained within the µModule, whereas green resistances are external to the µModule.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD 51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule. For example, in actual board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within a SIP (System-In-Package) module, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the µModule and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JSED51-9 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the µModule with heat sinks and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same power loss as that which was simulated. An outcome of this process and due-diligence yields a set of derating curves provided in other sections of this data sheet. After these laboratory tests have been performed and correlated to the µModule model, then the θ_{JB} and θ_{BA} are summed together to correlate quite well with the µModule model with no air flow or heat sinking in a properly define chamber. This θ_{JB}+ θ_{BA} value is shown in the Pin Configuration section and should accurately equal the θ_{JA} value because approximately 100% of power loss flows from the junction through the board into ambient with no airflow or top mounted heat sink.

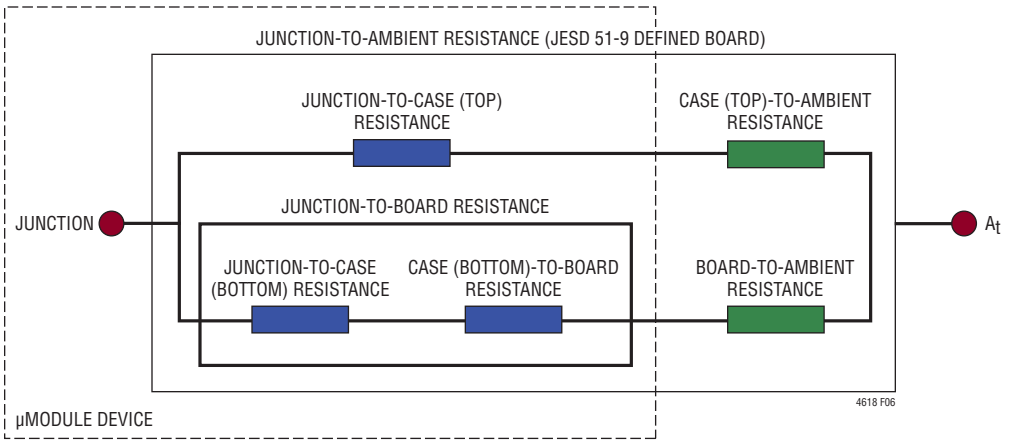

Figure 6. Graphical Representation of JESD51-12 Thermal Coefficients

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The 1.5V and 3.3V power loss curves in Figures 7 and 8 can be used in coordination with the load current derating curves in Figures 9 to 16 for calculating an approximate θ_{JA} thermal resistance for the LTM4618 with various heat sinking and air flow conditions. The power loss curves are taken at room temperature, and are increased with multiplicative factors according to the ambient temperature. These approximate factors are: 1 for 40°C; 1.05 for 50°C; 1.1 for 60°C; 1.15 for 70°C; 1.2 for 80°C; 1.25 for 90°C; 1.3 for 100°C; 1.35 for 110°C and 1.4 for 125°C. The derating curves are plotted with the output current starting at 6A and the ambient temperature at 40°C. The output voltages are 1.5V, and 3.3V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without air flow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 120°C maximum while lowering output current or power with increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example, in Figure 11 the load current is derated to ~5A at ~85°C with no air flow or heat sink and the power loss for the 12V to 1.5V at 5A output is about 1.7W. The 1.7W loss is calculated with the ~1.4W room temperature loss from the 12V to 1.5V power loss curve at 5A, and the 1.2 multiplying factor at 85°C ambient. If the 85°C ambient temperature is subtracted from the 115°C junction temperature, then the difference of 30°C divided 1.7W equals a 17°C/W θ_{JA} thermal resistance. Table 2 specifies a 16°C/W value which is very close. Table 2 and Table 3 provide equivalent thermal resistances for 1.5V and 3.3V outputs with and without air flow and heat sinking. The derived thermal resistances in Tables 2 and 3 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with the above ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick four layer board with two ounce copper for the two outer layers and one ounce copper for the two inner layers. The PCB dimensions are 95mm × 76mm. The BGA heat sink is listed in Table 3.

Safety Considerations

The LTM4618 modules do not provide isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure.

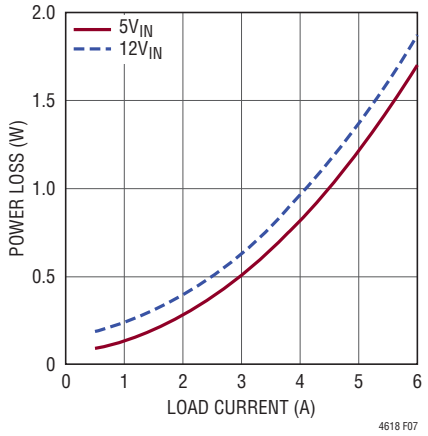

Figure 7. Power Loss at $1.5V_{OUT}$

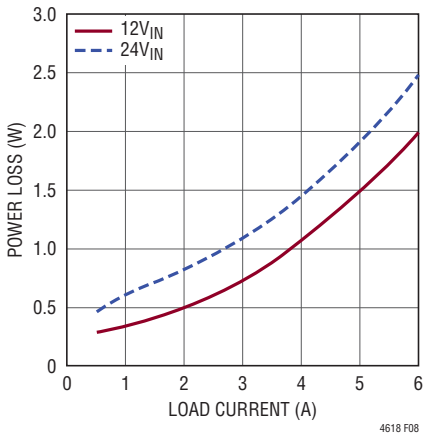

Figure 8. Power Loss at $3.3V_{OUT}$

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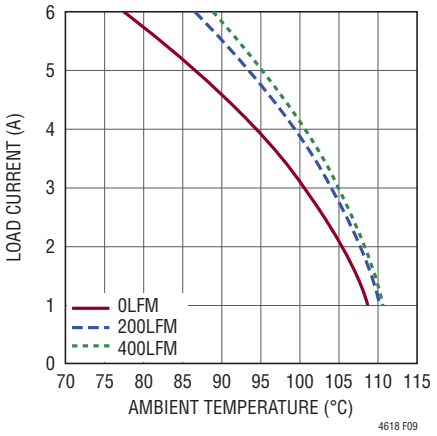

Figure 9. $5V_{IN}$ to $1.5V_{OUT}$ without Heat Sink

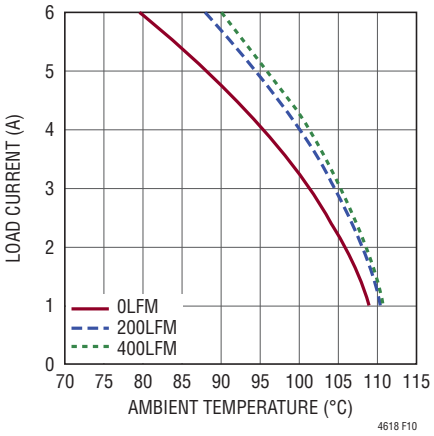

Figure 10. $5V_{IN}$ to $1.5V_{OUT}$ with Heat Sink

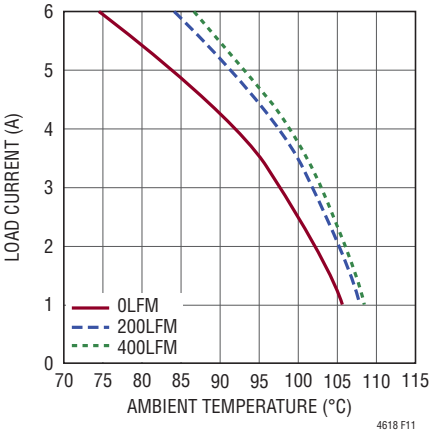

Figure 11. $12V_{IN}$ to $1.5V_{OUT}$ without Heat Sink

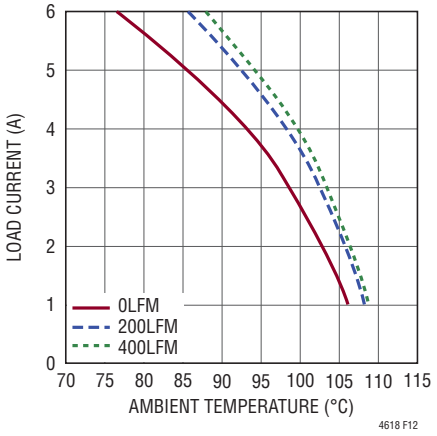

Figure 12. $12V_{IN}$ to $1.5V_{OUT}$ with Heat Sink

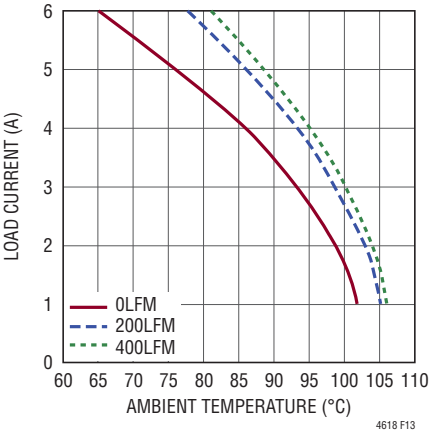

Figure 13. $12V_{IN}$ to $3.3V_{OUT}$ without Heat Sink

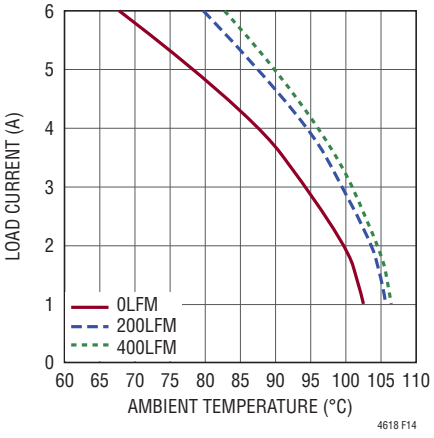

Figure 14. $12V_{IN}$ to $3.3V_{OUT}$ with Heat Sink

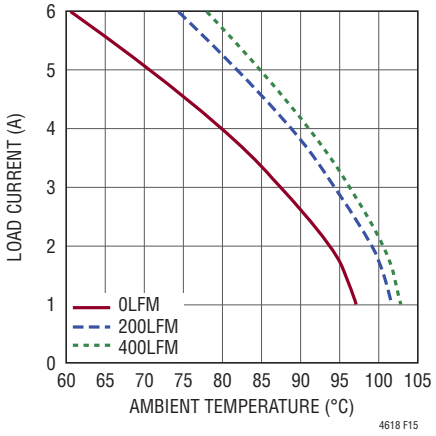

Figure 15. $24V_{IN}$ to $3.3V_{OUT}$ without Heat Sink

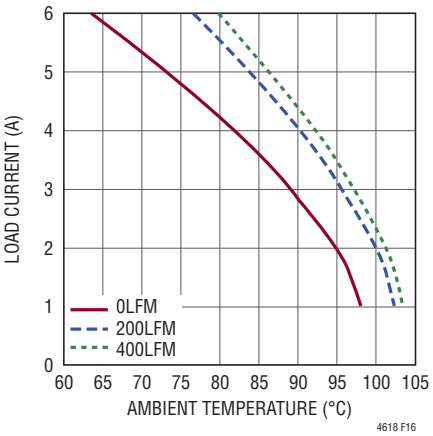

Figure 16. $24V_{IN}$ to $3.3V_{OUT}$ with Heat Sink

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Table 2. 1.5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	Θ_{JA} (°C/W)
Figures 9, 11	5, 12	Figure 7	0	None	16
Figures 9, 11	5, 12	Figure 7	200	None	12.2
Figures 9, 11	5, 12	Figure 7	400	None	11.2
Figures 10, 12	5, 12	Figure 7	0	BGA Heat Sink	15.2
Figures 10, 12	5, 12	Figure 7	200	BGA Heat Sink	11.6
Figures 10, 12	5, 12	Figure 7	400	BGA Heat Sink	10.7

Table 3. 3.3V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	Θ_{JA} (°C/W)
Figures 13, 15	12, 24	Figure 8	0	None	15
Figures 13, 15	12, 24	Figure 8	200	None	11.2
Figures 13, 15	12, 24	Figure 8	400	None	10.2
Figures 14, 16	12, 24	Figure 8	0	BGA Heat Sink	14.2
Figures 14, 16	12, 24	Figure 8	200	BGA Heat Sink	10.6
Figures 14, 16	12, 24	Figure 8	400	BGA Heat Sink	9.7

Heat Sink Used: 15 × 9 Version of Aavid #375424B000346

Table 4. Output Voltage Response vs Component Matrix (Refer to Figure 21) 0A to 3A Load Step

V_{OUT} (V)	C_{IN} (CERAMIC)	C_{IN} (BULK)	C_{OUT1} (CERAMIC)	C_{OUT2} (BULK)	COMP	C2 (pF)	FREQ (kHz)	DROOP (mV)	P-P DEVIATION (mV)	RECOVERY TIME (µs)	LOAD STEP (A/µs)	R_{FB} (kΩ)
1	22µF × 2	68µF	100µF × 4	None	None	100	400	38	76	35	3	242
1	22µF × 2	68µF	100µF × 2	220µF	None	None	400	35	70	35	3	242
1	22µF × 2	68µF	100µF	470µF	None	None	400	30	60	35	3	242
1.2	22µF × 2	68µF	100µF × 4	None	None	47	400	40	80	30	3	121
1.2	22µF × 2	68µF	100µF × 2	220µF	None	None	400	37	74	35	3	121
1.2	22µF × 2	68µF	100µF	470µF	None	None	400	27	54	35	3	121
1.5	22µF × 2	68µF	100µF × 3	None	None	47	500	48	96	36	3	68.1
1.5	22µF × 2	68µF	100µF	220µF	None	None	500	40	80	36	3	68.1
1.5	22µF × 2	68µF	100µF	470µF	None	None	500	30	60	40	3	68.1
1.8	22µF × 2	68µF	100µF × 3	None	None	47	500	52	104	36	3	48.7
1.8	22µF × 2	68µF	100µF	220µF	None	None	500	45	90	35	3	48.7
1.8	22µF × 2	68µF	100µF × 4	None	None	47	500	50	100	35	3	48.7
2.5	22µF × 2	68µF	100µF × 3	None	None	47	500	65	130	38	3	28
2.5	22µF × 2	68µF	100µF × 4	None	None	None	600	75	150	35	3	28
2.5	22µF × 2	68µF	100µF	220µF	None	None	600	60	120	45	3	28
3.3	22µF × 2	68µF	100µF × 2	None	None	22	600	90	180	36	3	19.1
3.3	22µF × 2	68µF	100µF × 2	None	None	47	600	80	160	40	3	19.1
5	22µF × 2	68µF	100µF	None	None	47	600	150	300	40	3	11.5

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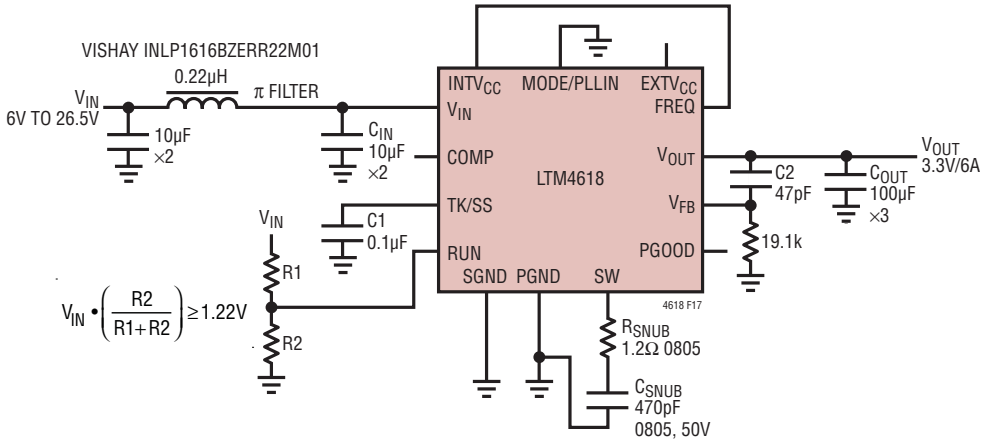


Figure 17. 6V to 26.5V Input, 3.3V at 6A Design, Meeting CISPR25 Conducted and CISPR22 Radiated EMI Solution

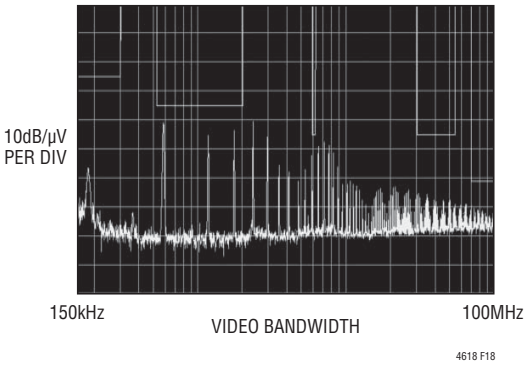


Figure 18. V_{IN} 26.5V, V_{OUT} 3.3V, I_{OUT} 5A, π Filter 20µF to 0.22µH Vishay (1616BZ) to 20µF CISPR25 Conducted Emissions

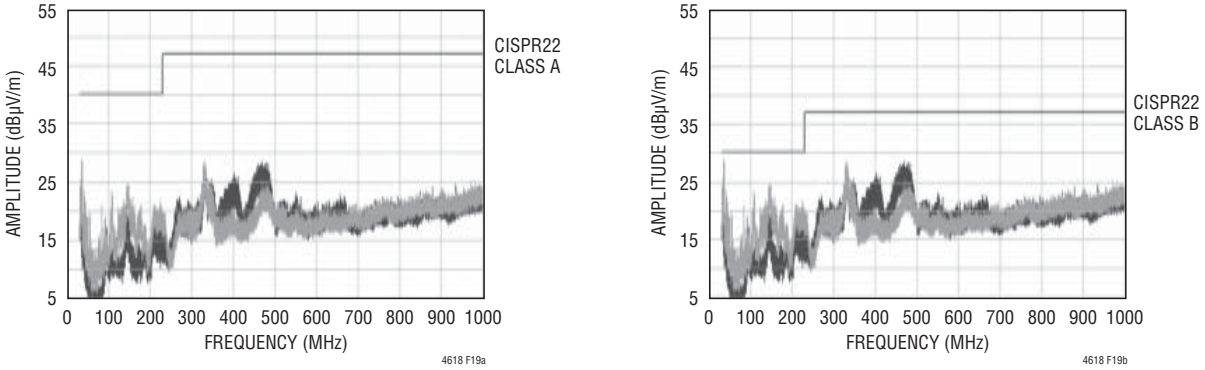


Figure 19. V_{IN} 26.5V, V_{OUT} 3.3V, I_{OUT} 5A, π Filter 20µF to 0.22µH Vishay (1616BZ) to 20µF CISPR22 Radiated EMI Plots

APPLICATIONS INFORMATION

EMI Section

The LTM4618 has been evaluated for CISPR22 A and B Radiated EMI and CISPR25 Conducted EMI. The CISPR25 Conducted EMI test was performed with an input π filter as shown in Figure 17. An RC snubber circuit is optionally used from the SW pin to the PGND pin to improve the higher frequency attenuation and EMI limit guard band. Figure 18 shows the CISPR25 conducted emissions plot for 26.5V input to 3.3V output at 5A load. Several conditions were evaluated, and Figure 18 results are from the worst-case condition. The input π filter is used to attenuate the reflected noise from the regulator input, and is primarily utilized when the power regulators are closed to the input power feed to a board, like the input power connectors. If the regulator design is placed out on the center of the system board, then the input π filter may not be needed because all of the extra board capacitance and the inductive planes will provide filtering for reflected emissions. If the system board has noise sensitive circuitry that is powered from the same voltage rail as the regulators are, then an input π filter is a good idea to keep regulator noise from corrupting the noise sensitive circuitry on the system board. Figure 19 shows the CISPR22 B Radiated EMI plots. The input π filter is used to attenuate the reflected noise from propagating out onto the input power cables, thus possibly causing radiated EMI issues. An RC snubber circuit is optionally used from the SW pin to the PGND pin to improve the higher frequency attenuation and EMI limit guard band. A placeholder can accommodate the R_{SNUB} and C_{SNUB} components with 1.2Ω and 470pF. These components are probably not necessary, but can be used or adjusted to improve the radiated limit guard bands at the higher frequencies by attenuating any switch node ringing due to parasitic values in the high speed switching paths. It is important to follow the recommended layout guidelines and use good X5R or X7R ceramic capacitors to get good results.

Layout Checklist/Example

The high integration of LTM4618 makes the PC board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current path, including V_{IN}, PGND and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Test points can be placed on signal pin for monitoring during testing.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, PGND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on the pad, unless they are capped.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to PGND underneath the unit.

Figure 20 gives a good example of the recommended layout.

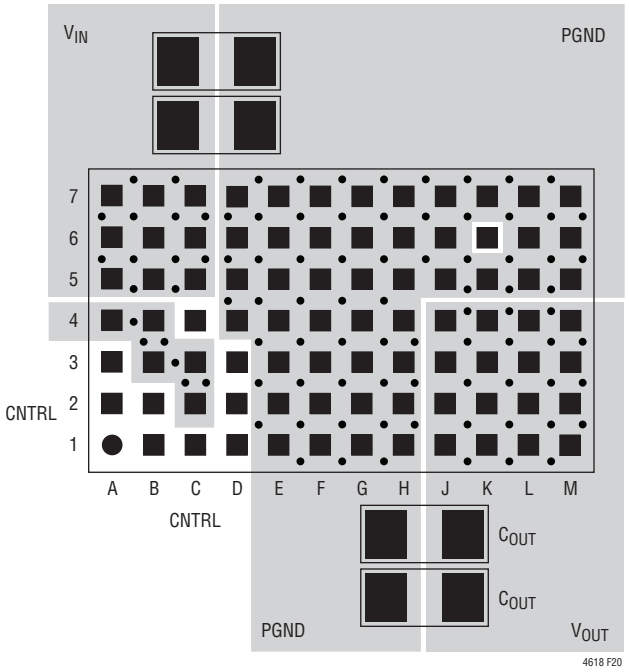


Figure 20. Recommended PCB Layout Example

TYPICAL APPLICATIONS

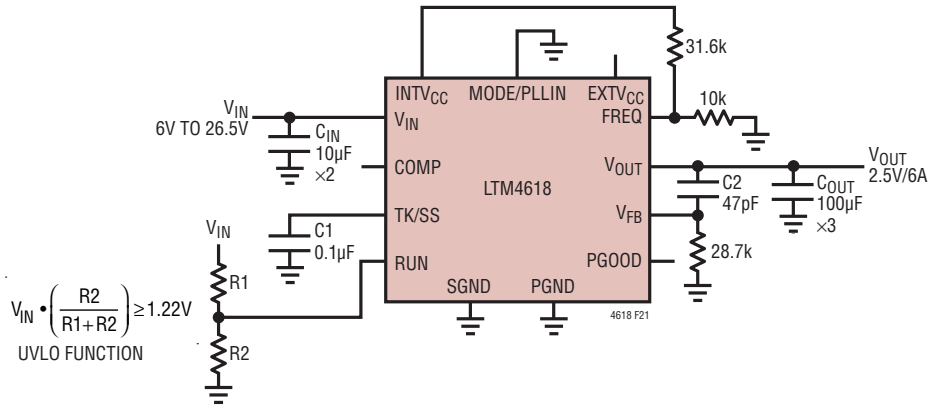


Figure 21. Typical 6V to 26.5V Input, 2.5V at 6A Design, 500kHz Operation

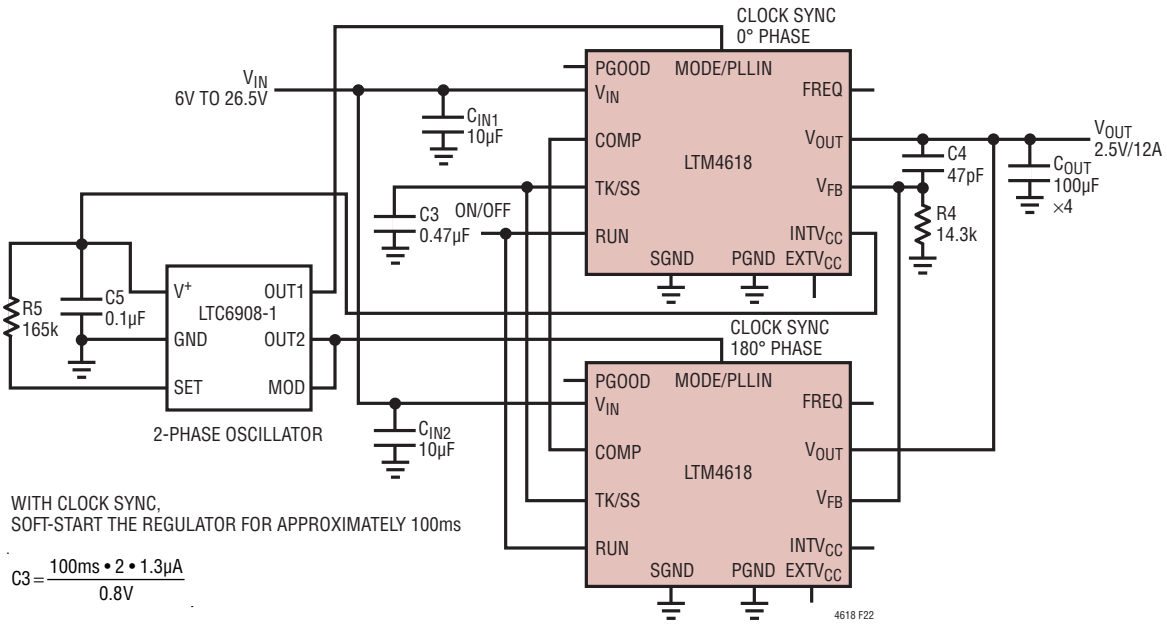


Figure 22. Two LTM4618 Parallel, 2.5V at 12A Design

TYPICAL APPLICATIONS

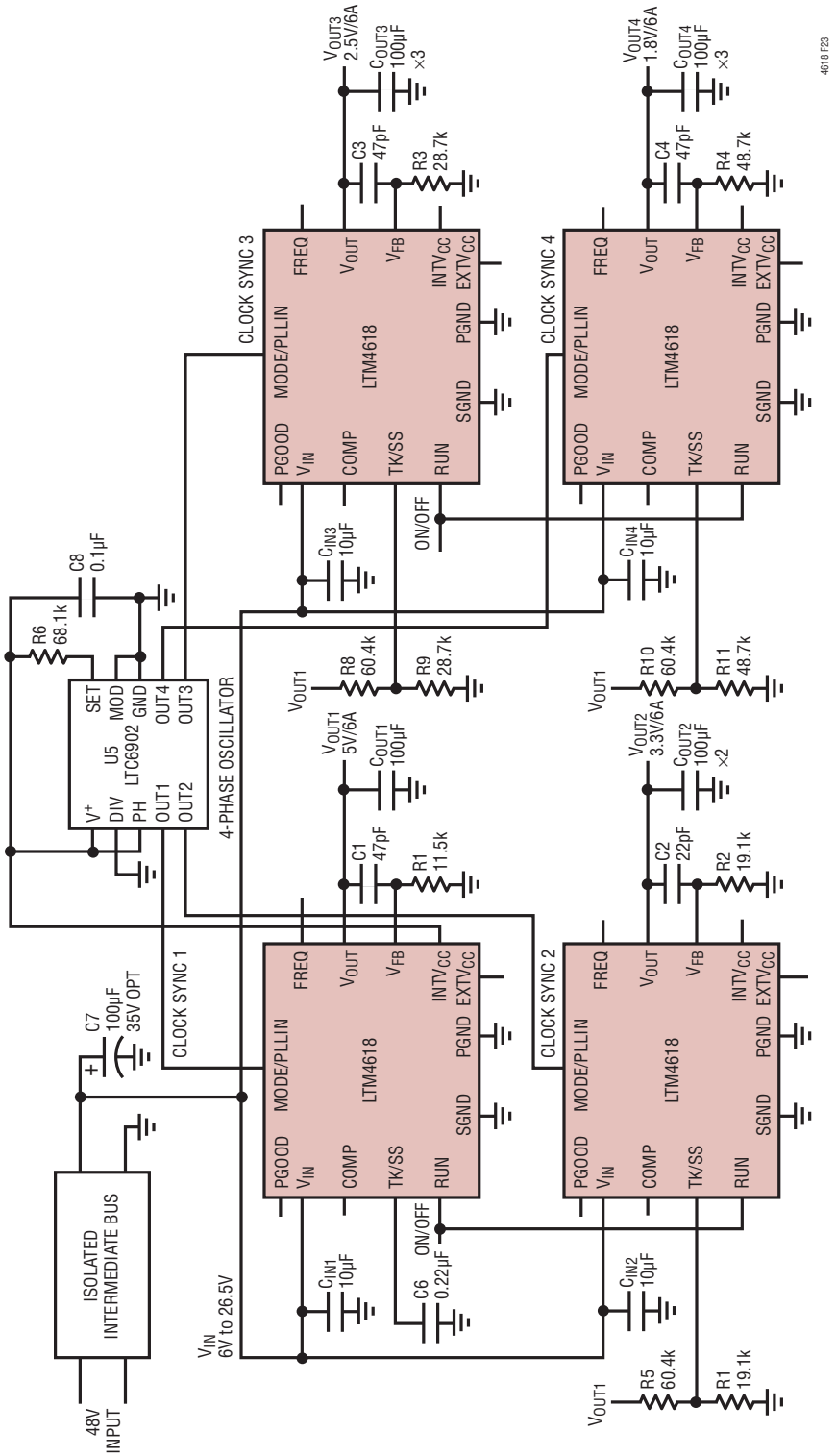
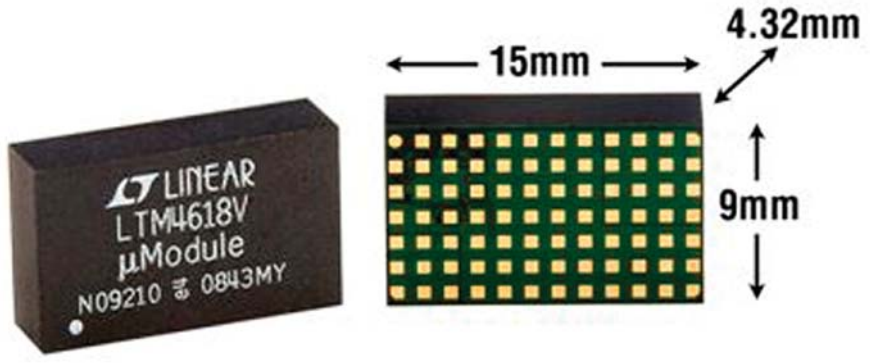


Figure 23. 4-Phase, Four Outputs (5V, 3.3V, 2.5V and 1.8V) with Tracking

PACKAGE PHOTOGRAPH



PACKAGE DESCRIPTION

Pin Assignment Tables
(Arranged by Pin Function)

PIN NAME	
A1	N/C
A2	FREQ
A3	MODE/PLLIN
A4	PGND
A5	V_{IN}
A6	V_{IN}
A7	V_{IN}
B1	TK/SS
B2	RUN
B3	SGND
B4	PGND
B5	V_{IN}
B6	V_{IN}
B7	V_{IN}
C1	COMP
C2	SGND
C3	SGND
C4	$EXTV_{CC}$
C5	V_{IN}
C6	V_{IN}
C7	V_{IN}

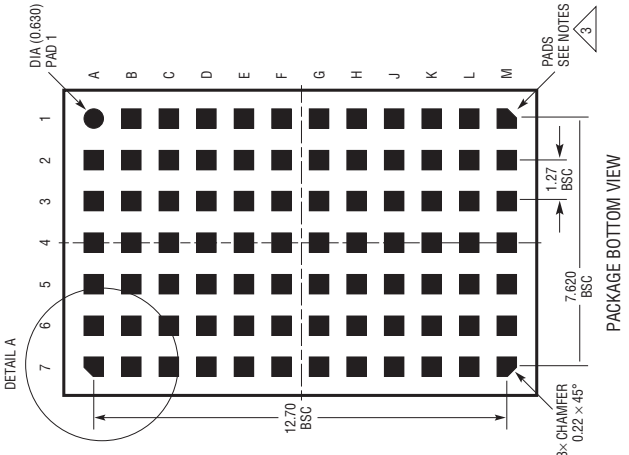
PIN NAME	
D1	V_{FB}
D2	PGOOD
D3	$INTV_{CC}$
D4	PGND
D5	PGND
D6	PGND
D7	PGND
E1	PGND
E2	PGND
E3	PGND
E4	PGND
E5	PGND
E6	PGND
E7	PGND
F1	PGND
F2	PGND
F3	PGND
F4	PGND
F5	PGND
F6	PGND
F7	PGND

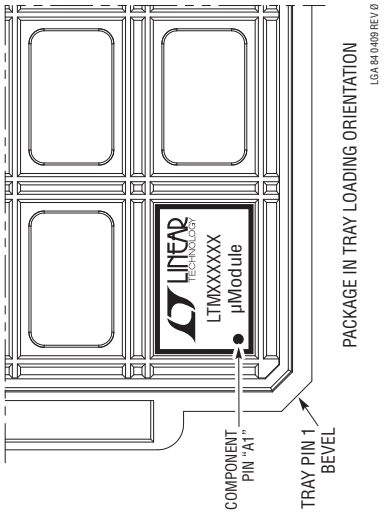
PIN NAME	
G1	PGND
G2	PGND
G3	PGND
G4	PGND
G5	PGND
G6	PGND
G7	PGND
H1	PGND
H2	PGND
H3	PGND
H4	PGND
H5	PGND
H6	PGND
H7	PGND
J1	V_{OUT}
J2	V_{OUT}
J3	V_{OUT}
J4	V_{OUT}
J5	PGND
J6	PGND
J7	PGND

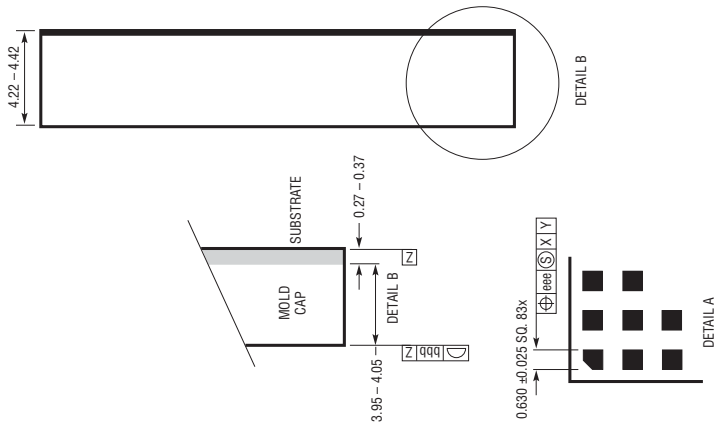
PIN NAME	
K1	V_{OUT}
K2	V_{OUT}
K3	V_{OUT}
K4	V_{OUT}
K5	PGND
K6	SW
K7	PGND
L1	V_{OUT}
L2	V_{OUT}
L3	V_{OUT}
L4	V_{OUT}
L5	PGND
L6	PGND
L7	PGND
M1	V_{OUT}
M2	V_{OUT}
M3	V_{OUT}
M4	V_{OUT}
M5	PGND
M6	PGND
M7	PGND

PACKAGE DESCRIPTION

LGA Package
84-Lead (15mm × 9mm × 4.32mm)
(Reference LTC DWG # 05-08-1842 Rev Ø)

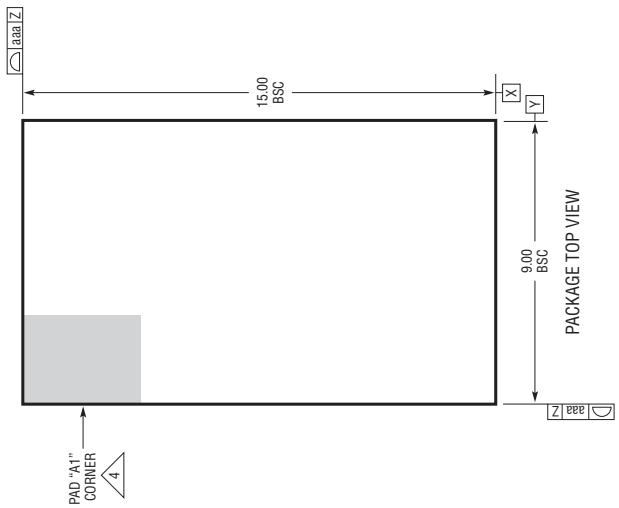


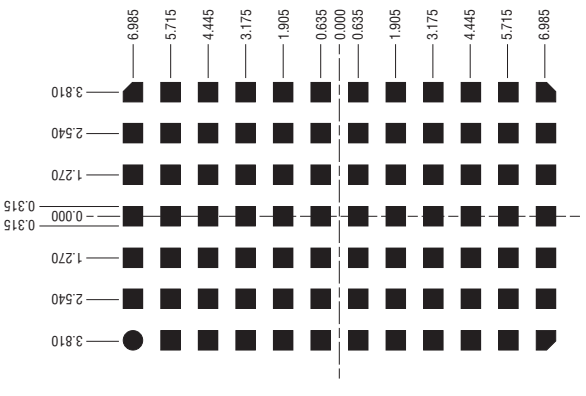




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. LAND DESIGNATION PER JESD MO-222
4. DETAILS OF PAD #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PAD #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. THE TOTAL NUMBER OF PADS: 84

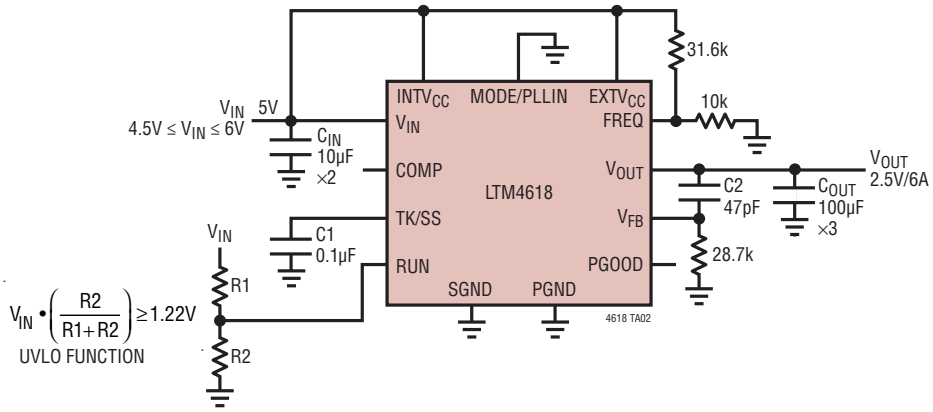
SYMBOL	TOLERANCE
aaa	0.15
bbb	0.10
eee	0.05





TYPICAL APPLICATION

5V Input, 2.5V at 6A Design, 500kHz Operation



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4603	6A DC/DC µModule Regulator with PLL and Output Tracking/Margining	4.5V to 20V Input, 0.6V to 5V Output, 15mm × 15mm × 2.8mm LGA Package
LTM4604A	4A DC/DC µModule Regulator	2.375V to 5.5V Input, 0.8V to 5V Output, Tracking
LTM4608A	8A DC/DC µModule Regulator	2.7V to 5.5V Input, 0.6V to 5V Output, PLL, Tracking
LTM4612	36V_{IN} DC/DC µModule Regulator	4.5V to 36V Input, 3.3V to 15V Output, PLL, Tracking, Margining
LTM4619	Dual 4A DC/DC µModule Regulator	4.5V to 26.5V Input, Dual 0.8V to 5V Output, PLL, Tracking
LTM8025	36V_{IN}, 3A DC/DC µModule Regulator	3.6V ≤ V_{IN} ≤ 36V; 0.8V ≤ V_{OUT} ≤ 24V; 9mm × 15mm × 4.32mm LGA Package

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