MX88L284AEC
Data Sheet

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General Description

The MX88L284AEC is a highly integration chip for Flat Panel Display application. It's fully compatible with MX88L284. With Macronix's Smartscaling™ -2 filter, it provides high quality scaled video image and format conversion capability.

Applications

- LCD monitor
- LCD projector
- Other Flat Panel Display Application (DMD, PDP, PALC ..).

Features

General Features

- Converts NTSC/PAL and PC video signal into flat panel display device timing and resolution
- Provide Full frame buffer, reduce frame buffer (w/ compression) and frame buffer less optional architecture.
- Built-in memory and output clock generator
- Built-in OSD generator with 64 ROM font, and 64 programmable RAM fonts
- Provide 90 degree rotation for internal OSD to support portrait direction display
- Arbitrary scaling from 1/32 to 32 times with filters (SmartScaling™ – 2^+ Technology)
- Support Auto-tracking and Auto-position capabilities (SmartTracking™ Technology)
- Support Auto-gain capability for input image
- Support Flip and Mirror capabilities
- On-chip brightness and contrast adjustments
- On-chip γ correction for panel compensation
- Support dynamic dithering capability to make 18 bit video as good as 24 bit quality
- Support H/V Sync. Polarity and pulse width information for mode detection
- Support two types of CPU interface (direct and serial bus)

- Provide 1 pixel/clock and 2 pixel/clock output to connect TFT LCD panel directly
- Built-in Color space converter for video decoder input
- Support configurable SDRAM/SGRAM (x0 x1 and x2) for different resolution to minimize the system cost
- Support Composite Sync. input
- Support DPMS and H/V sync. Interrupt

Input

- PC video up to 1024 x 768 @ 85Hz
- Support YCrCb422, RGB888 mode (Interlaced and Non-interlaced)
- Support Philips, Samsung, and Techwell NTSC/PAL video decoder in 16 bit interface
- Support TTL clock input
- Support input H/V sync. polarity and odd/even field detection
- Support digital input capability

Output

- Support TFT LCD panel in following resolution and frequency

Resolution	800x600	1024x768
Horizontal frequency (KHz)	20 ~ 55	20 ~ 70
Vertical frequency (Hz)	50 ~ 75	50 ~ 75
Dot clock (MHz)	32.5 ~ 60	25 ~ 80

Remark:

The Max. output resolution and frequency is depend on memory bus bandwidth, input resolution/frequency and image size.

- Single (18/24) and Dual (36/48) bit RGB data output
- Support Inverse, delay adjustment and frequency adjustment for LCD panel clock (LCKA and LCKB)
- Support programmable H/V sync. and LDTG timing for LCD panel
- Support OSD MUX capability for On-Screen-Display chip input
- Built-in OSD generator
- Built-in YCrCb to RGB color space converter
- Built-in programmable Brightness and Contrast control

- Built-in programmable gamma correction table
- Support Horizontal and Vertical position adjustment
- Support SmartScaling™ -2+ or double scan capability for Interlaced input
- Support Edge Filter control

CPU Interface

- Support direct 8 bit uP interface and serial bus (high-speed) interface
- Support CPU line write/read and flush screen capability

Memory Interface

- Optimized single buffer design
- Support Memory clock fine-tune and frequency programmable capabilities
- Support 32/16 bit bus width
- Support SDRAM/SGRAM x0 x1 and x2 configuration
- Support power down mode
- Support DRAM self test

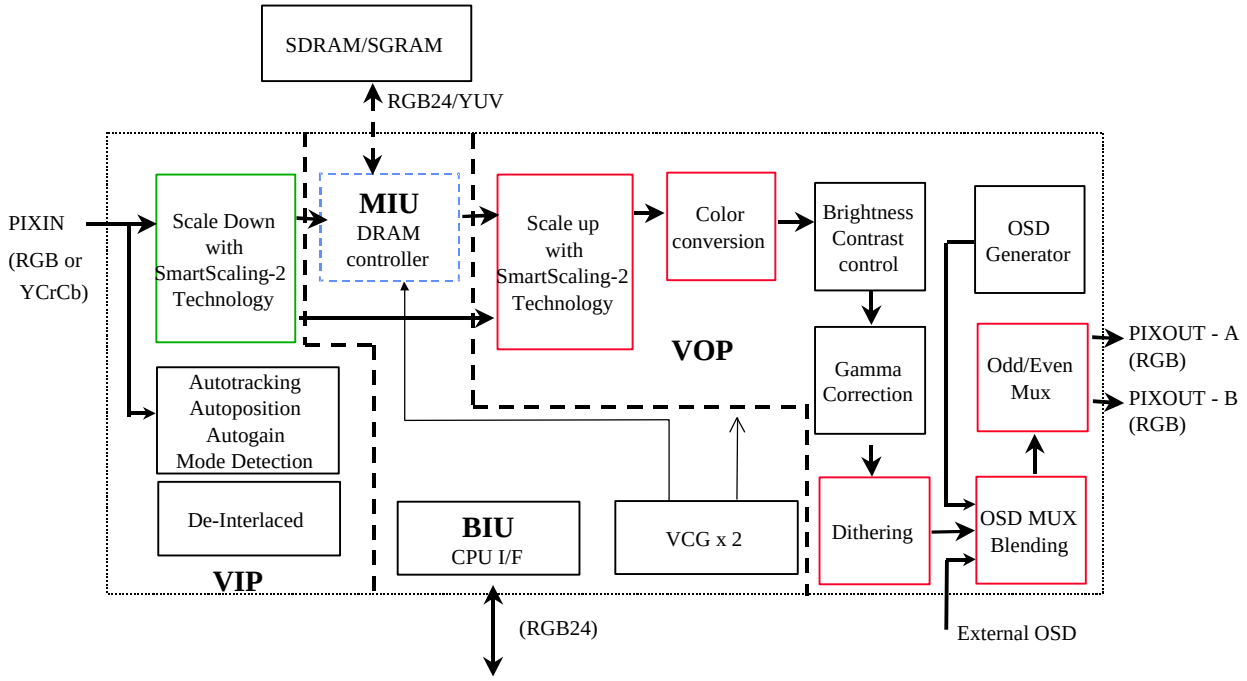
Power

- Power supplier: 3.3 volt power supplier
- Power Consumption: less than 1.5W

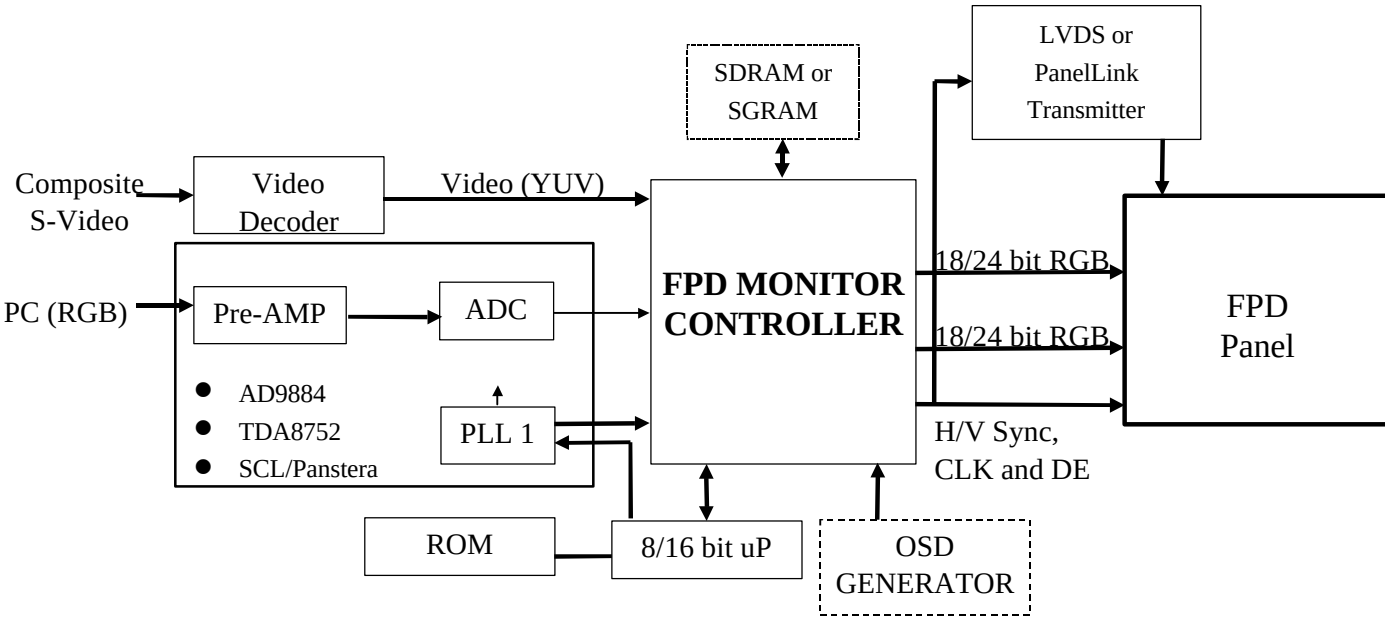
Others

- Support power down mode
- Power on strapped input for system configuration
- Support GPIO pins to minimized the system cost.

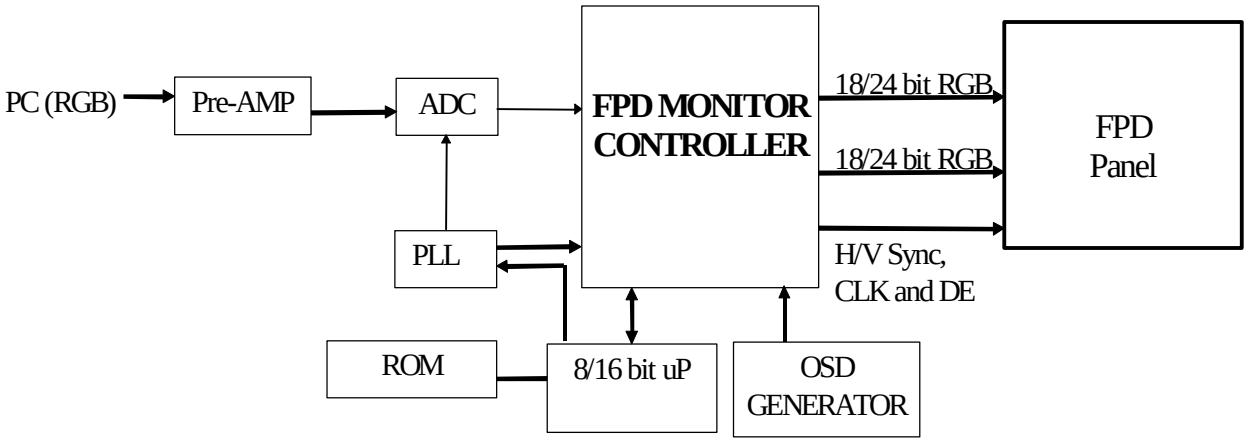
Chip Block Diagram



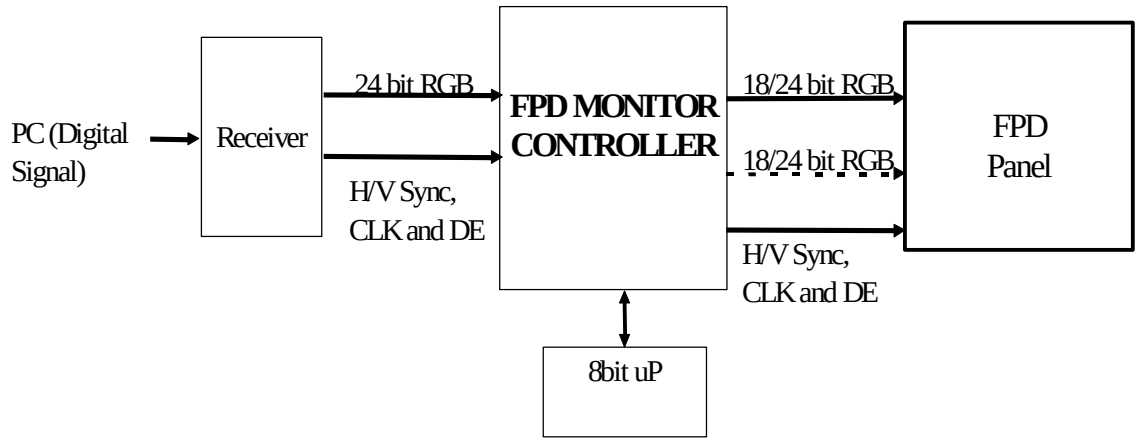
System Block Diagram for LCD monitor (TTL and PanelLink/LVDS Interfaced)



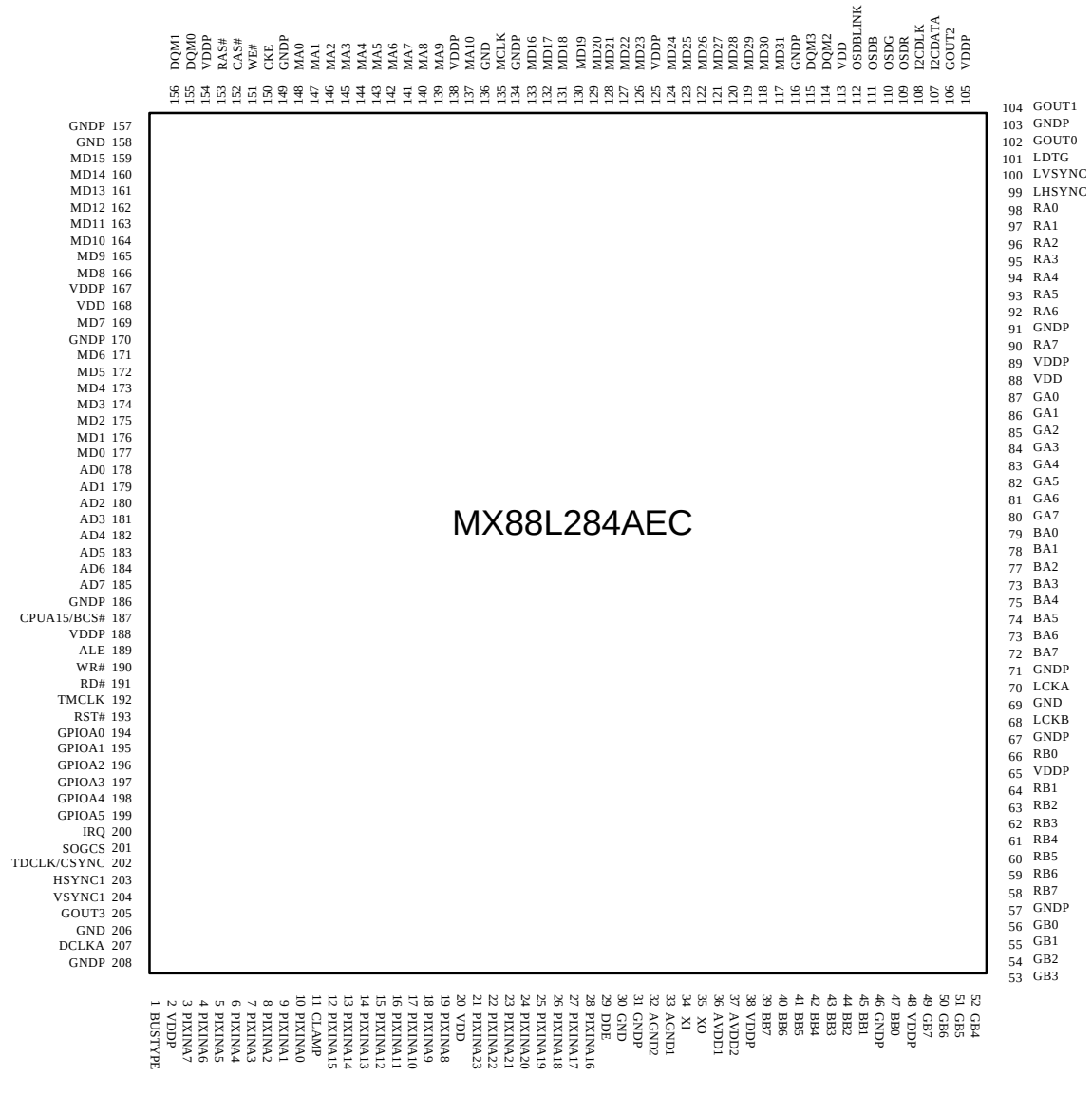
System Diagram W/O Frame Buffer



System Diagram for Digital input Interface



Pin Configurations



General Description

There are four major parts in this chip which include VIP (Video Input Processor), MIU (Memory Interface Unit), VOP (Video Output Processor) and BIU (CPU Bus Interface Unit). Following is the block and description of these parts.

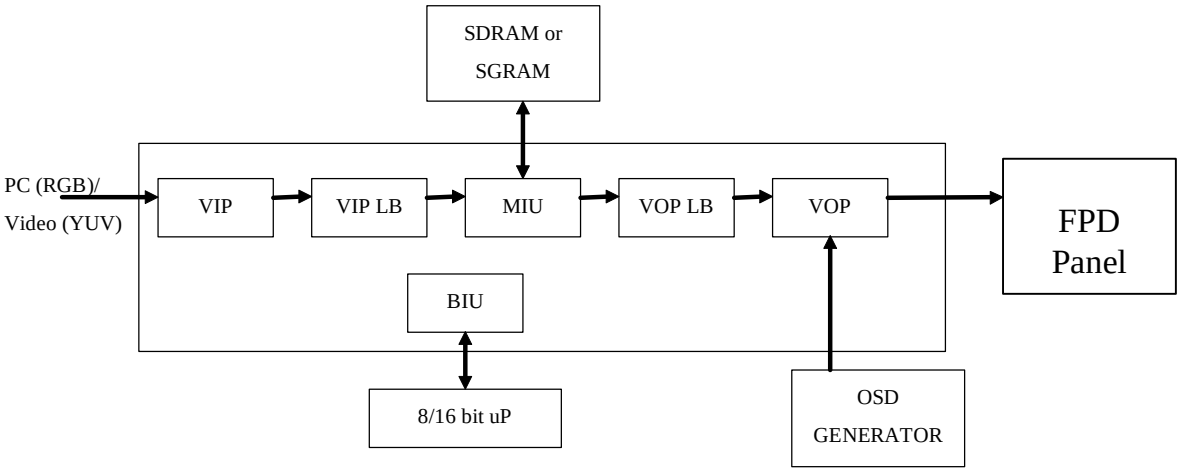


Fig. 1 Chip Level Block Diagram

VIP (Video Input Processor) Function Description

VIP is a Video Input Process unit which processes incoming data either from Graphic card or Video Decoder.

With Line Buffers and Decimation logic based on proprietary Smartscaling^{TM} –2 algorithm , it can process input data and then write to frame buffer . Furthermore, it can detect the polarity of input H/V SYNC and then do the normalization of them and also detect the ODD/EVEN field of the input interlaced data. It can also measure the pulse width and period of input H/V SYNC for system application purposes.

Video encoder interface is supported for video image input.

MIU (Memory Interface Unit) Functional Description

MIU is a interface unit between external DRAM and this chip. We support 6 kinds of configurations for SDRAM and SGRAM through POWER_ON Strapped_Input or register defined value.

DRAM Configuration (Support 8M SGRAM and 16M SDRAM)

DRAM Type	DRAM Number	Bus Width
SGRAM	1	32 bits
SGRAM	2	32 bits
SDRAM	1	16 bits
SDRAM	2	32 bits

Memory Configuration Table

Input Resolution	NO. of SGRAM	NO. of SDRAM
YCrCb	1	1
640X480	1/2	1
800X600	1	2
1024X768	1 or 2	2
1280X1024	2	2

VOP (Video Output Processor) Function Description

VOP is a Video Output Process unit which reads data from Frame buffer and then process it to display Flat panel Display.

With Line Buffers and Scale- up logic based on proprietary Smartscaling™ –2 algorithm, it can enlarge image smoothly. Furthermore, it provides many adjusting functions like programmable Brightness and Contrast control, programmable GAMMA table, programmable Dithering control, and OSD MUX to adjust the output quality. It also provides Single/Dual output to cope with different flat panels display device.

BIU (Bus Interface Unit) Function Description

BIU is a bus interface unit between the host CPU and MX88281/MX88282, which supports two bus types : direct and Serial Bus through POWER_ON Strapped_Input value.

It also supports 3 functions to access frame buffer:

1. Line Write Allow WRITE data from CPU to frame buffer line by line.

2. Flush Write Allow WRITE assigned color data defined in the register to frame buffer to clean screen.

3. Line Read Allow READ data from frame buffer to CPU line by line.

Pin Description

CPU Interface Pins: (15 pins)

Pin Name	Drive	I/O	No.	DESCRIPTION
RSTZ#		I	193	System reset.
AD[7:0]	4 mA	IO	185-178	Multiplexed low_order address and data bus.
AD7/SBCLK			185	Serial Bus Clock
AD6/SBDATA			184	Serial Bus Data
AD5/SBCS#			183	Serial Bus CS# Low Active
CPUA15/BCS		I	187	high_order a15 address input, or BIU Valid cycle.(for ISA bus debug)
ALE		I	189	Address Latch Enable for 8051 Bus.
WR#		I	190	Memory Write Strobe.
RD#		I	191	Memory Read Strobe
BUSTYPE		I	1	Bus type select
IRQ		O	200	Interrupt request

DRAM Interface Pins: (52 pins) ** 3.3 Volt Interface ***

Pin Name	Drive	I/O	No.	DESCRIPTION
MCLK	20 mA	O	135	Memory clock
CKE	4 mA	O	150	Memory clock enable
RAS#	8 mA	O	153	Row address strobe
CAS#	8 mA	O	152	Column address strobe
WE#	8 mA	O	151	Write Enable
DQM[3:0]	8 mA	O	115,114, 156,155	data mask byte enable (For SGRAM)
MA[10:0]	8 mA	O	137,139-148	Memory address
MD[31:0]	4 mA	IO	117-124, 126-133, 159-166, 169, 171-177,	Memory data input/output

Input Interface Pins: (30 pins)

Pin Name	Drive	I/O	No.	DESCRIPTION
DCLKA		I	207	Input dot clock
VSYNC1		I	204	Input VSYNC
HSYNC1		I	203	Input HSYNC
SOGCS		I	201	Input Sync on Green composite Sync
PIXINA[7:0]		I	3-10	Pixel input A RED[7:0] from ADC. Y[7:0]: Luminance data from Video Decoder.
PIXINA[15:8]		I	12-19	Pixel input A GREEN[7:0] from ADC. CbCr[7:0]: Color data from Video Decoder.
PIXINA[23:16]		I	21-28	Pixel Input A BLUE[7:0] from ADC. D23: MPLLC2, (Video input clk signal)/2. D22: MPHS, Video input Hsync signal. D21: MPVS, Video input Vsync signal. D20: MPODD, Video input Odd/Even field signal. D19: MPHREF, Video input horizontal reference signal. D18: MPLLC, Video input clk signal. D17: MPCREF, Video input clk reference ignal D16: MPVREF, Video input vertical reference signal.
DDE	16 mA	I	29	Digital display enable input pin
CLAMP	2 mA	O	11	Clamp signal

LCD Interface Pins: (53 pins)

Pin Name	Drive	I/O	No.	DESCRIPTION
RA[7:0]	4 mA	O	90, 92-98	RED DATA (Odd),
GA[7:0]	4 mA	O	80-87	GREEN DATA (Odd),
BA[7:0]	4 mA	O	72-79	BLUE DATA (Odd),
RB[7:0]	4 mA	O	58-64, 66	RED DATA (Even).
GB[7:0]	4 mA	O	49-56	GREEN DATA (Even).
BB[7:0]	4 mA	O	39-45, 47	BLUE DATA (Even),
LVSYNC	8 mA	O	100	VSYNC output for LCD display.

Pin Name	Drive	I/O	No.	DESCRIPTION
LHSYNC	8 mA	O	99	HSYNC output for LCD display.
LDTG	8 mA	O	101	Data Enable output for LCD display.
LCKA	16 mA	O	70	Odd data clock output for LCD display.
LCKB	16 mA	O	68	Even data clock output for LCD display.

OSD interface Pins: (6 pins)

Pin Name	Drive	I/O	No.	DESCRIPTION
OSDR		I	109	OSD RED input
OSDG		I	110	OSD GREEN input
OSDB		I	111	OSD BLUE input
OSDBLNK		I	112	OSD select.
OSDR0 /OSDINT/GOUT2	4mA	I/O	106	Extended OSD RED input or use as Motorola OSD intensity input (Output Share With GOUT4)
OSDG0/GOUT1	2mA	I/O	104	Extended OSD GREEN input (Support in 6-bit format) Output Share with GOUT1
OSDB0/GOUT0	2mA	I/O	102	Extended OSD BLUE input (Support in 6 -bit format) Output Share with GOUT0
I2CCLK	4 mA	IO	108	I2C CLK. Pull up by internal 20K Ohm resistor
I2CDATA	4 mA	IO	107	I2C DATA. Pull up by internal 20K Ohm resistor

Internal VCG Interface Pins: (2 pins)

Pin Name	I/O	No.	DESCRIPTION
XI	I	34	Analog pad for Reference Frequency Input for internal oscillator.
XO	O	35	Analog pad for Reference Frequency Output for internal oscillator.

Other Interface Pins: (9 pins)

Pin Name	Drive	I/O	No.	DESCRIPTION
GOUT3	4 mA	O	205	General Output 3
GOUT2	4 mA	O	106	General Output 2

Pin Name	Drive	I/O	No.	DESCRIPTION
GOUT1	2 mA	O	104	General Output1
GOUT0	2 mA	O	102	General Output0
GPIOA[5:0]	2 mA	IO	199-194	General I/O GPIOA[5] : Input select GPIOA[4] : PDEN for External PLL GPIOA[3] : DS for External ADC GPIOA[1] : ADC-Coast source select GPIOA[0] : Hsync source select Pull down by internal 20Kohm resistors

External Clock Input Interface Pins: (2)

Pin Name	I/O	No.	DESCRIPTION
TMCLK	I	192	External MCLK input
TDCLK/CSYNC	I	202	External DCLK input/Composite Sync input

Power Pins:

All Power 3.3 Volt

Pin Name	No.	DESCRIPTION
VDD	20,88,113,168	Core Power
GND	30,69,136,158, 206	Core GND
VDDP	2,38,48,65,89,105,125,138,154,167,188	PAD Power
GNDP	31,46,57,67,71,91,103,116, 134,149,157,170,186,208	PAD GND
AVDD	36 ,37	Analog Power
AGND	32,33	Analog GND

Remark:

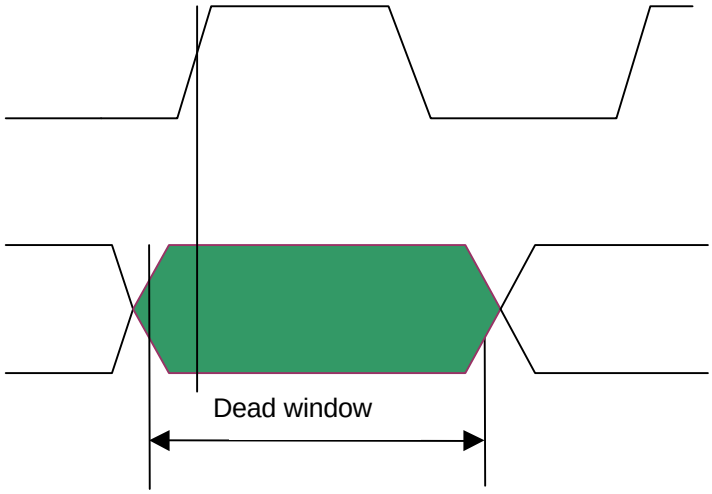
1. All the input loading is 5pf
2. Driving capability is measured under 30pf loading
3. MCLK, LCKA driving capability is measured under 50pf loading

AC Characteristics

AC timings if the load of all output pins is 5~20pF

1. Input signal

AC timing of input horizontal sync

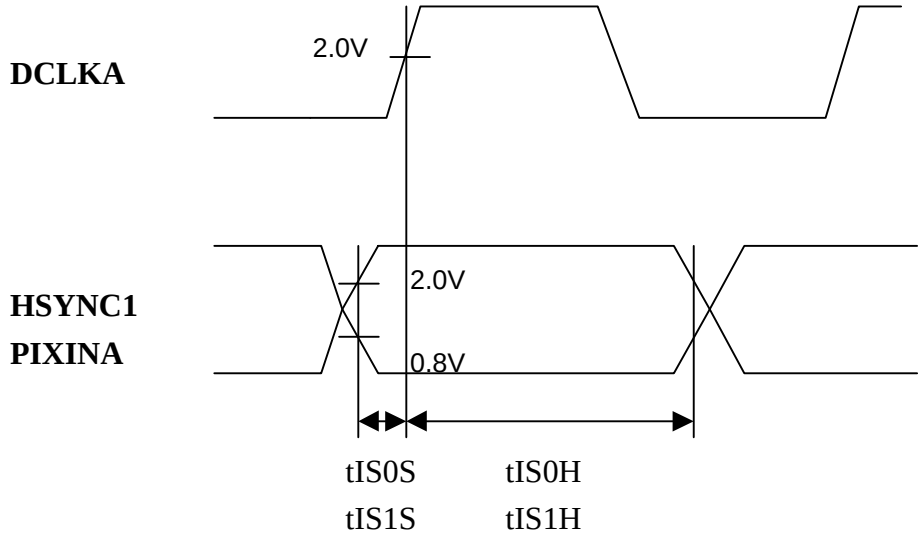


Note : in the following case, it assumes that registerE4.bit6 is 0, and registerF1 and F2 are 0x00

	Register10, bit 5	RegisterE8, bit 5:4	remark
Case	0	00,10 or 11	Low power disabled, HSYNC1 strobed

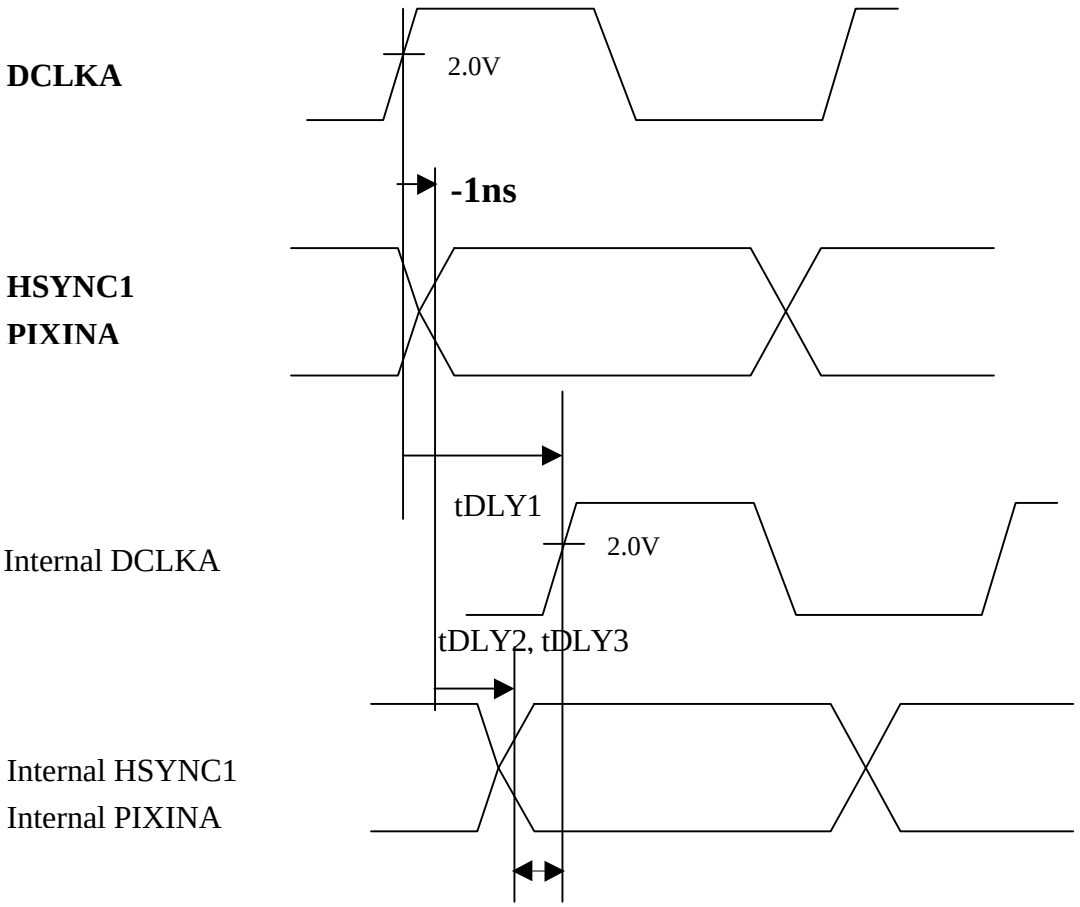
Note : it assumes the DCLKA rising edge is at 0 ns

	Case
Dead window for HSYNC1	1~6ns



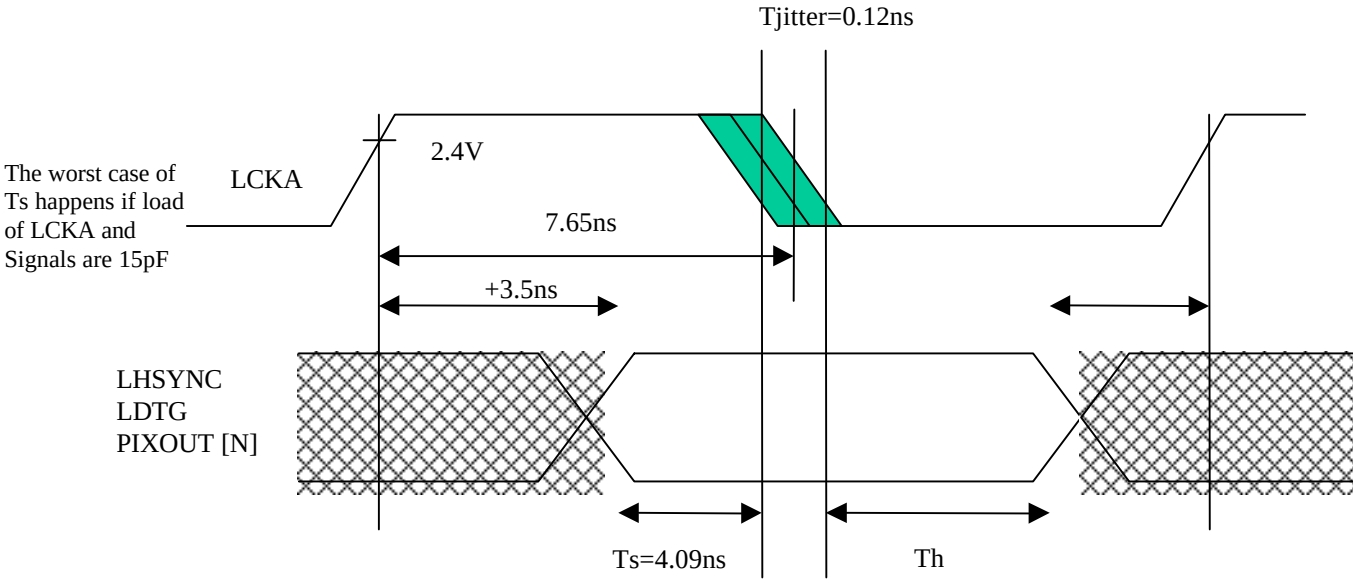
Symbol	Parameter	Min.	Max.	Unit
tIS1S tIS0S	Input image PIXINA setup time for DCLKA Input image HSYNC1 setup time for DCLKA	-1		ns
tIS1H	Input image PIXINA hold time for DCLKA	7		ns
tIS0H	Input image HSYNC1 hold time for DCLKA	6		ns

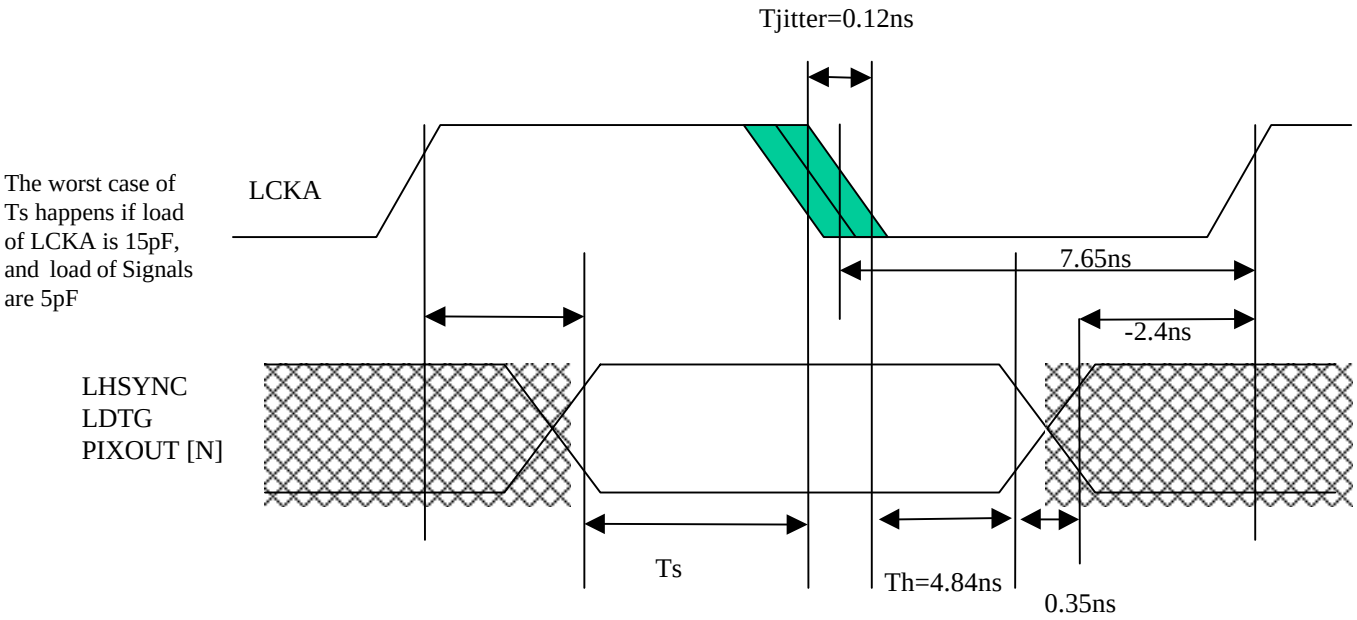
(note2 : MX88L284 does not need tIS0S/tIS0H for VSYNC1 to properly operate if regE8[6:4]=111)
(note3 : -1ns means that PIXINA and HSYNC1 can be earlier than, or **late than DCLKA by less than 1ns**, without sampling problem. These -1ns and 7/6ns might look non-straightforward, it's because there is added internal delay for DCLKA to gain more safety margin and prevent any sampling problem caused by skew between PIXINA/HSYNC1 and DCLKA on the PCB board)



2. Output signal

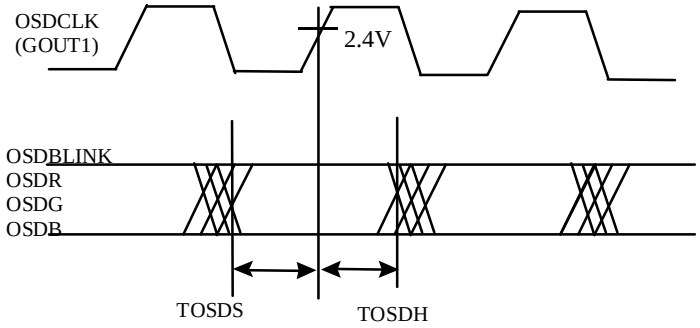
1. the setup/hold time of pixel data, LHSYNC and LDTG with respect to LCKA
   (5pF <= load of signal data <= load of LCKA <= 15pF)





Symbol	Parameter	Min.	Max.	Unit
TOS1DL	Output LHSYNC, LDTG, Pixel Signal output delay	-2.4	3.5	ns

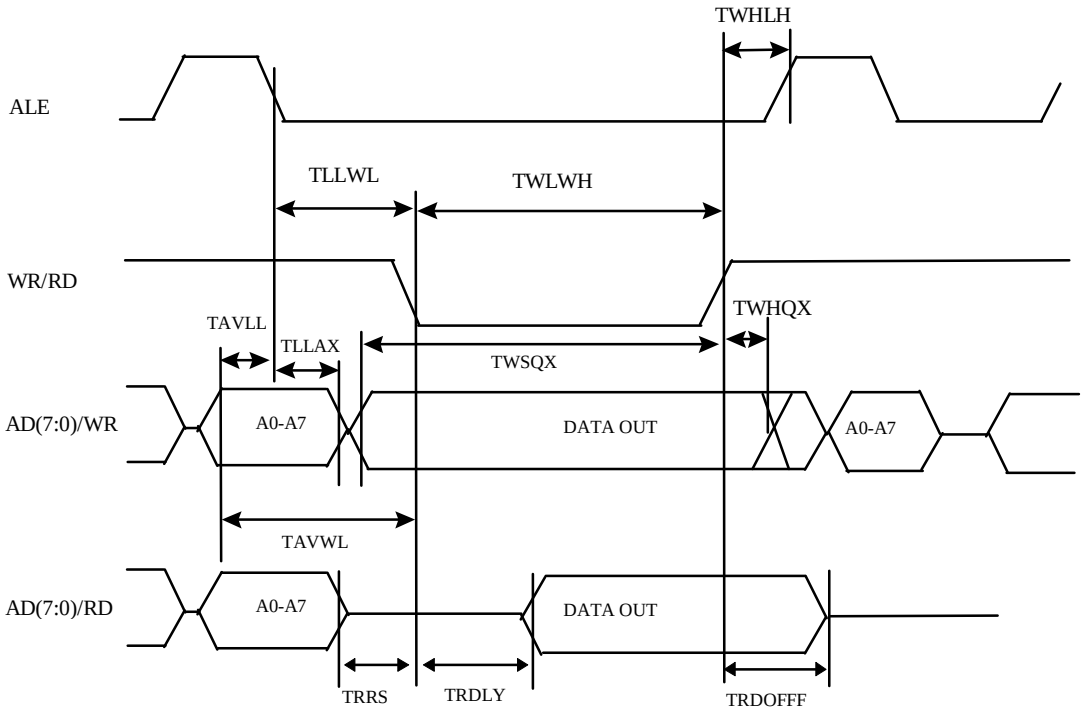
External OSD signal



Symbol	Parameter	Min.	Max.	Unit
tOSDS	OSD input setup time	3		ns
tOSDH	OSD input hold time	2		ns

(note : this data value is measured at the condition of regA5[7:0]=0000_0000, regA6[7:0]=0000_0100)

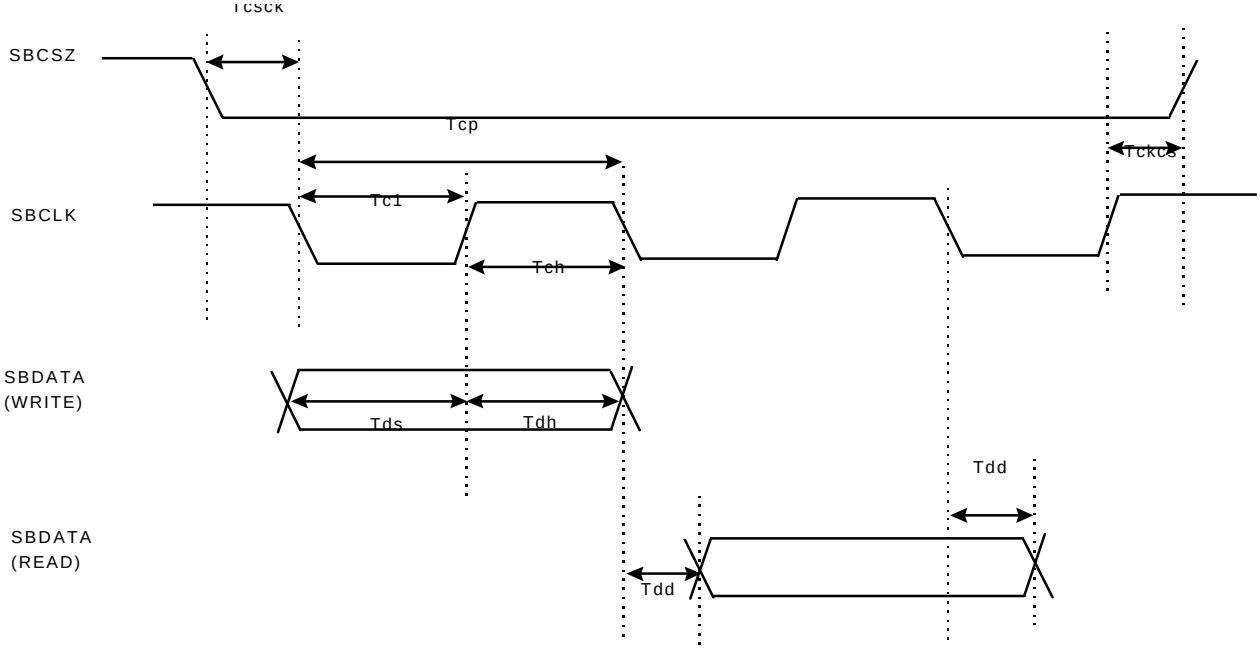
3. Direct CPU Interface



Symbol	Parameter	Min.	Max.	Unit
TAVLL	Address Valid to ALE Low	6		ns
TLLAX	Address Hold After ALE Low	6		ns
TWLWH	WR Pulse Width	40		ns
TWSQX	Data Setup Before WR	6		ns
TWHQX	Data Hold After WR	6		ns
TWHLH	---	*	*	*
TRDLY	Data delay after RD Low		35	ns
TRDOFF	Data off delay after RD High		15	ns
TALLWL	ALE falling edge to Write active Low	15		
TAVWL	Address Valid to Write Active Low	21		
TRRS	Minimum Address Release time from Address to invalid RD active Low	0		

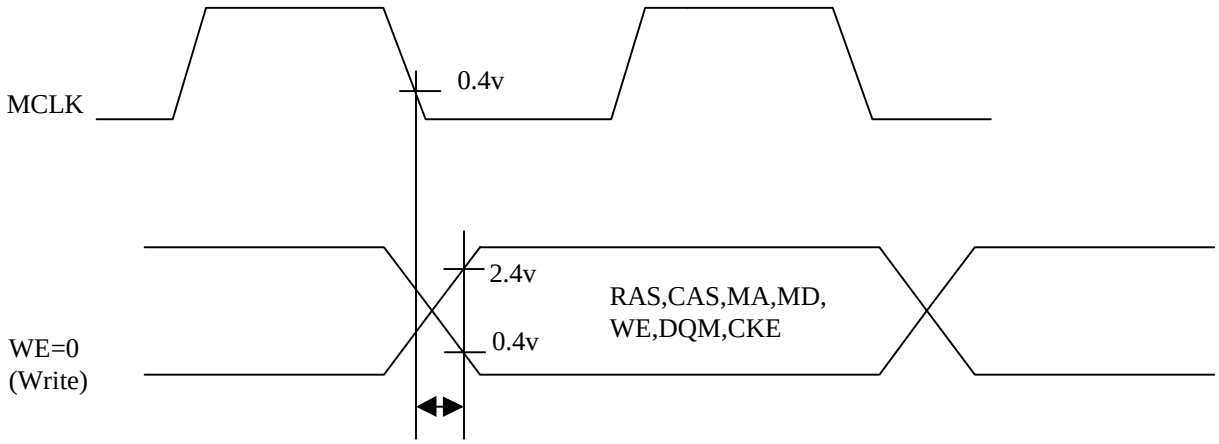
(note : there is no need of tWHLH for MX88L284AEC to operate properly)

4. Serial Bus Interface



Symbol	Parameter	Min.	Max.	Unit
Tcsck	CS to CLK Start	15		ns
Tckcs	CLK to CS high	15		ns
Tds	Data setup time versus CLK	3		ns
Tdh	Data hold time versus CLK	4		ns
Tdd	Data delay time	5	16	ns

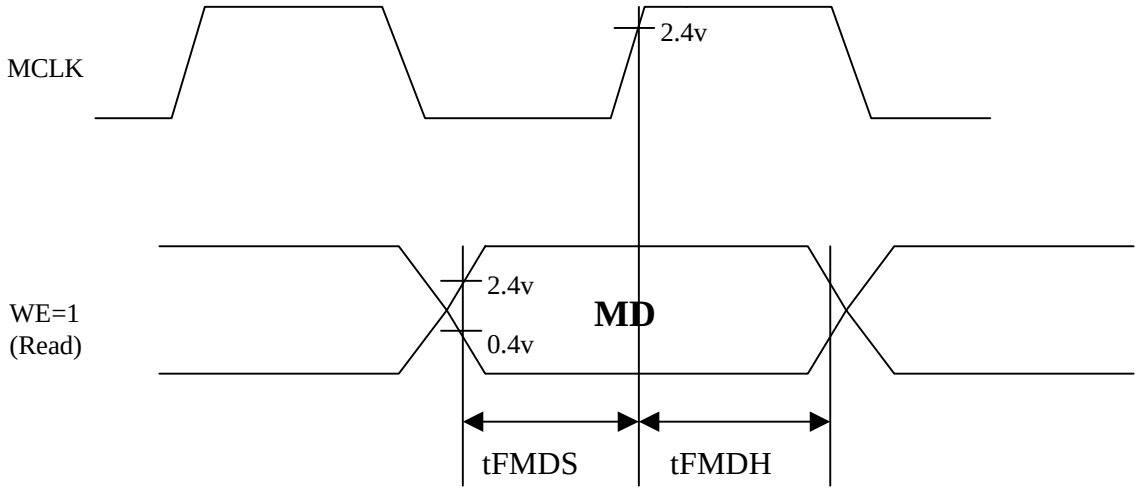
5. Frame memory (SDRAM/SGRAM) Interface



Tfmdl (MCLK falling edge to output signals)

Load of MCLK(pF)	Load of signals(pF)	Min(ns)	Max(ns)
5~20	5~20	-1.5*	2.5
5	5	0	2
20	20	-1.5	2.3

(note1 : this data value is measured at the condition of reg91[3:0]=1000. Reg91[3:0] is used to choose MCLK inversion and internal delay time
note2 : -1.5ns means that memory data and control signals may appear earlier than MCLK)



	Min(ns)	Max(ns)
tFMDS	1	
tFMDH	1.5	

(note : this data value is measured at the condition of reg92[7]=1. Reg92[7] is used to choose either internal memory clock or pad feedback MCLK as MD's sampling clock)

6. External Clock Input Interface

Symbol	Parameter	Min.	Max.	Unit
Fclk	Maximum TMCLK/TDCLK input frequency		80	MHz
Fpw	Minimum pulse width	3		ns

DC characteristics

1. Environmental specification:

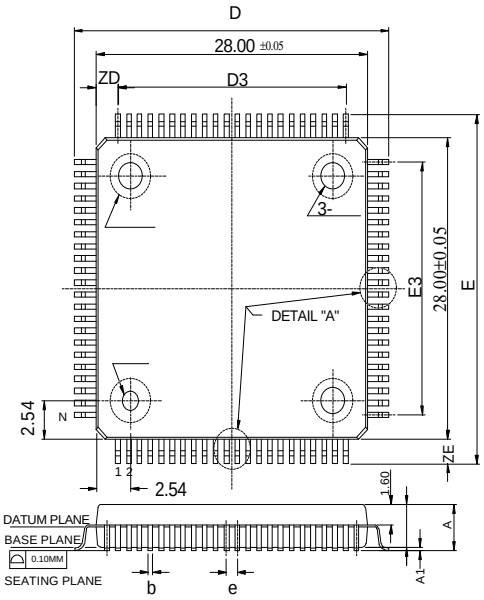
Rating	Value	Unit
Ambient Operating Temperature	0 to 70	°C
Storage Temperature	-55 to 125	°C
Maximum Junction Temperature	125	°C
Maximum Case Temperature	100	°C

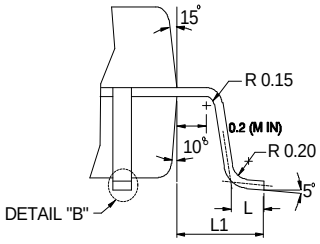
2. Standard DC Specification for 3.3 Volts Operation:

(Ta=0°C to 70°C, VCC=3V to 3.6V)

Symbol	Parameter	Min	Max	Unit	Conditions
VOH	Output High Voltage	2.4		V	
VOL	Output Low Voltage		0.5	V	
VIH	Input High Voltage	0.7VCC		V	
VIL	Input Low Voltage		0.8	V	
RPU	I/O Pull-up Resistance	15	100	KOhm	
RPD	I/O Pull-down Resistance	15	100	KOhm	
ILI	Input Leakage Current	-10	+10	*u* A	
ILO	Output Leakage Current	-20	+20	*u* A	

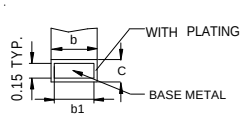
Dimensions



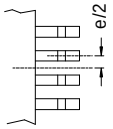


TERMINAL DETAILS

DETAIL "A"	144F2828-A	160F2828-A	208F2828-A	256F2828-A
b	0.32	0.32	0.22	0.18
C	0.10	0.10	0.10	0.10
b1	0.30	0.30	0.20	0.16
e	0.65	0.65	0.50	0.40
L1	1.60	1.60	1.30	1.30
L	0.80	0.80	0.50	0.50
ZE (REF.)	1.33	1.33	1.25	1.25
E3 (REF.)	25.35	25.35	25.50	25.50
E	31.2	31.2	30.6	30.6
ZD (REF.)	2.63	1.33	1.25	1.40
D3 (REF.)	25.35	25.35	25.50	25.20
D	31.2	31.2	30.6	30.6
A1	0.35	0.35	0.35	0.35
A (MAX.)	3.80	3.80	3.80	3.80
N	144L	160L	208L	256L
JEDEC	MO-108 DC-1	MO-108 DD-1	MO-143 FA-1	MO-143 FB1



DETAIL "B"



DETAIL "A"

Macronix International Co., Ltd.					DWG. NO. 6110-0212
TITLE OUTLINE DIMENSIONS FOR QFP2828 MM PACKAGE					TOLERANCE ANGLE °
DRAWN	APPROVED	SCALE	UNIT		REVISION
CH Lin	JW Lin		mm		2