MX23C1024

1M-BIT [64K x 16] CMOS MASK ROM

FEATURES

- 64K x 16 organization (JEDEC pin out)
- Single +5V power supply
- Fast access time: 120/150/200ns
- Totally static operation
- Completely TTL compatible
- Operating current: 60mA
- Standby current: 100uA
- Package
  - 40 pin DIP (600 mil)
  - 44 pin PLCC

GENERAL DESCRIPTION

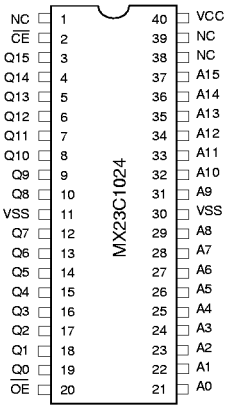
The MX23C1024 is a 5V only, 1M-bit, Read Only Memory. It is organized as 64Kx16 bit. MX23C1024 has a static standby mode, and has an access time of 120/150/200ns. It is designed to be compatible with all microprocessors and similar applications in which high performance, large bit storage and simple interfacing are important design considerations.

MX23C1024 offers automatic power-down, with power-down controlled by the chip enable ($\overline{CE}$) input. When $\overline{CE}$ is not selected, the device automatically powers down and remains in a low-power standby mode as long as $\overline{CE}$ stays in the unselected mode.

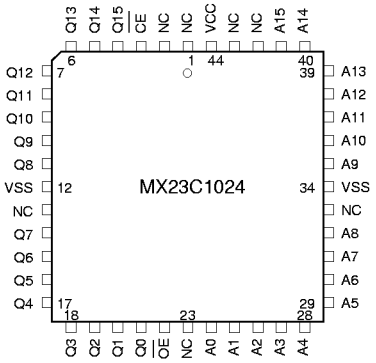
The $\overline{OE}$ input as well as $\overline{CE}$ input may be programmed active Low.

PIN CONFIGURATION

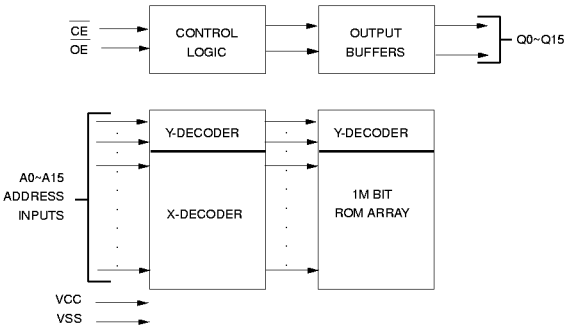
40 PDIP



44 PLCC



BLOCK DIAGRAM



PIN DESCRIPTION

Symbol	Pin Function
A0~A15	Address Input
Q0~Q15	Data Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
VCC	Power Supply Pin (+5V)
VSS	Ground Pin

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to 7.0V
VCC to Ground Potential	-0.5V to 7.0V

Note:
Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

DC CHARACTERISTICS (Ta = 0°C ~ 70°C, VCC = 5V±10%)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.4V	-	IOH = -1.0mA
Output Low Voltage	VOL	-	0.4V	IOL = 2.1mA
Input High Voltage	VIH	2.2V	VCC+0.3V	
Input Low Voltage	VIL	-0.3V	0.8V	
Input Leakage Current	ILI	-10uA	10uA	VIN=0 to 5.5V
Output Leakage Current	ILO	-10uA	10uA	VOUT=0 to 5.5V
Power-Down Supply Current	ICC3	-	100uA	$\overline{CE}$>VCC-0.2V
Standby Supply Current	ICC2	-	1.5mA	$\overline{CE}$ = VIH
Operating Supply Current	ICC1	-	60mA	Note 1

CAPACITANCE (Ta = 25°C, f=1.0MHz (Note 2))

Item	Symbol	TYP.	MAX.	UNIT	Conditions
Input Capacitance	CIN	8	12	pF	VIN=0V
Output Capacitance	COUT	8	12	pF	VOUT=0V

AC CHARACTERISTICS (Ta = 0°C ~ 70°C, VCC = 5V±10%)

Item	Symbol	23C1024-12		23C1024-15		23C1024-20		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	CONDITIONS
Cycle Time	tCYC	120ns	-	150ns	-	200ns	-	
Address Access Time	tAA	-	120ns	-	150ns	-	200ns	
Output Hold Time After Address Change	tOH	0ns	-	0ns	-	0ns	-	
Chip Enable Access Time	tACE	-	120ns	-	150ns	-	200ns	
Output Enable/Chip Select Access Time	tAOE	-	70ns	-	80ns	-	90ns	
Output Low Z Delay	tLZ	0ns	-	0ns	-	0ns	-	Note 3
Output High Z Delay	tHZ	-	70ns	-	70ns	-	70ns	Note 4

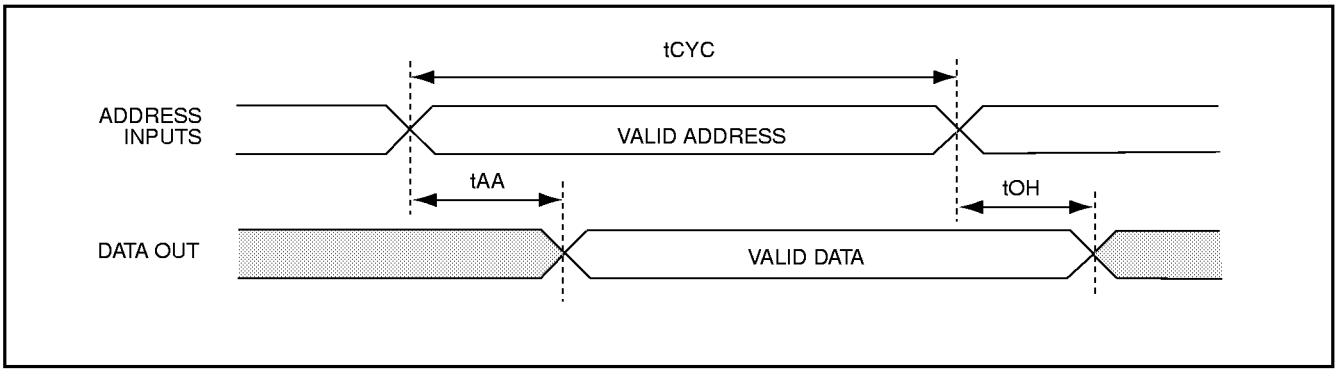
Note:
1. Measured with device selected at f=5 MHz and output unloaded.
2. This parameter is periodically sampled and is not 100% teseted.
3. Output low-impedance delay (tLA) is measured from CE going low.
4. Output high-impedance delay (tHZ) is measured from CE going high.

AC Test Conditions

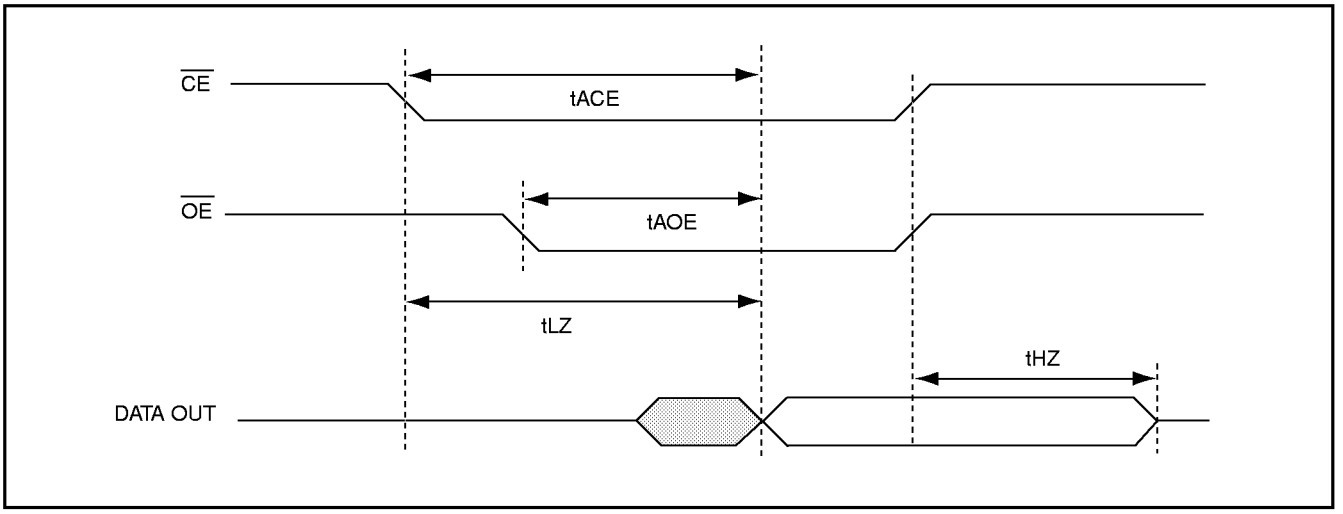
Input Pulse Levels	0.4V~ 2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.5V
Output Timing Level	0.8V and 2.0V
Output Load	1TLL+100pF

TIMING DIAGRAM

PROPAGATION DELAY FROM ADDRESS ($\overline{CE}$/$\overline{OE}$=ACTIVE)



PROPAGATION DELAY FROM CHIP ENABLE (ADDRESS VALID)



ORDER INFORMATION

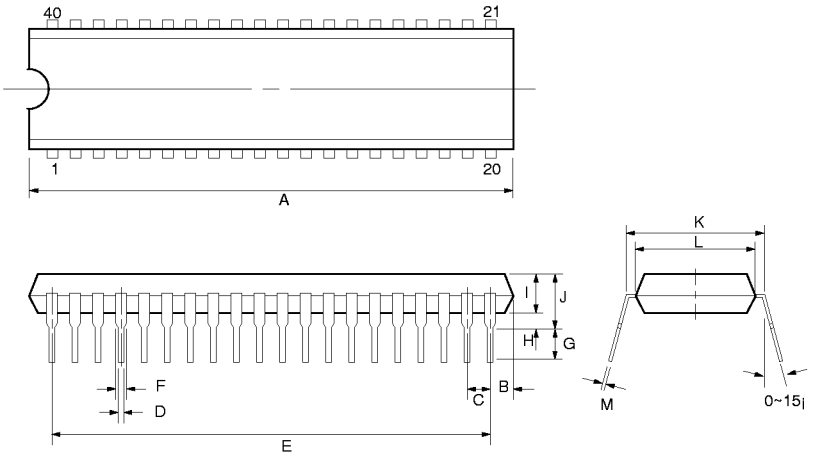
Part No.	Access Time	Operating Current MAX.	Standby Current MAX.	Package
MX23C1024PC-12	120ns	60mA	100uA	40 pin DIP
MX23C1024PC-15	150ns	60mA	100uA	40 pin DIP
MX23C1024PC-20	200ns	60mA	100uA	40 pin DIP
MX23C1024QC-12	120ns	60mA	100uA	44 pin PLCC
MX23C1024QC-15	150ns	60mA	100uA	44 pin PLCC
MX23C1024QC-20	200ns	60mA	100uA	44 pin PLCC

PACKAGE INFORMATION

40-PIN PLASTIC DIP (600 mil)

ITEM	MILLIMETERS	INCHES
A	52.54 max.	2.070 max.
B	2.03 [REF]	.080 [REF]
C	2.54 [TP]	.100 [TP]
D	.46 [Typ.]	.018 [Typ.]
E	48.22	1.900
F	1.52 [Typ.]	.060 [Typ.]
G	3.30±.25	.130±.010
H	.51 [REF]	.020 [REF]
I	3.94±.25	1.55±.010
J	5.33 max.	.210 max.
K	15.22±.25	.600±.010
L	13.97±.25	.550±.010
M	.25 [Typ.]	.010 [Typ.]

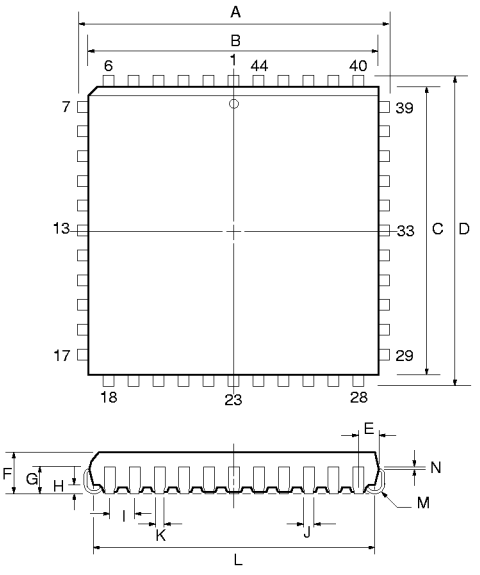
NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



44-PIN PLASTIC LEADED CHIP CARRIER (PLCC)

ITEM	MILLIMETERS	INCHES
A	17.53±.12	.690±.005
B	16.59±.12	.653±.005
C	16.59±.12	.653±.005
D	17.53±.12	.690±.005
E	1.95	.077
F	4.70 max.	.185 max.
G	2.55±.25	.100±.010
H	.51 min.	.20 min.
I	1.27 [Typ.]	.050 [Typ.]
J	.71±.10	.028±.004
K	.46±.10	.018±.004
L	15.50±.51	.610±.020
M	.63 R	.025 R
N	.25 [Typ.]	.010 [Typ.]

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



REVISION HISTORY

Revision	Descritpion	Page	Date
1.2	Provide $\overline{CE}$ & $\overline{OE}$ only.		AUG/26/1997
1.3	AC Characteristics:tOH 10ns --> 0ns	P3	JAN/29/1999