NEC

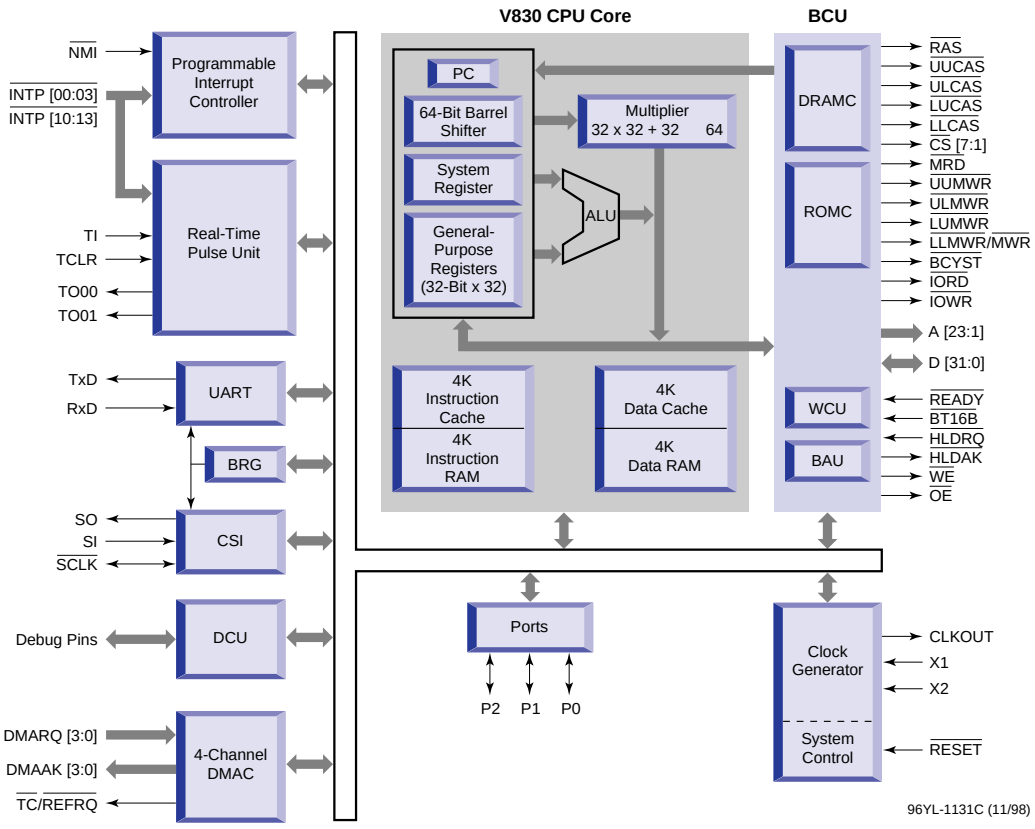
V831™ 32-BIT RISC MICROCONTROLLER

The V831 microcontroller is the second member of NEC's V830™ family of 32-bit RISC microcontrollers. This high-performance, low-power microcontroller is well suited for embedded, image processing and networking applications. The V831 device integrates the V830 microprocessor core with on-chip external memory support and standard peripherals that include a DMA controller, DRAM/EDO/page-mode ROM controllers, UART, clocked serial interface, and timers. With its on-board peripherals, the V831 microcontroller provides a cost-effective solution for consumer electronics applications.

SPECIFICATIONS

- Clock frequency: 33 to 100 MHz
- Performance
  - 118 Dhrystone MIPS at 3.3V
  - 157 MIPS/W
- 32-bit single-cycle MAC instruction (200 MOPS)
- 32-bit external data bus
- Power consumption: 750 mW at 100 MHz at 3.3V (max.)
- DRAM/EDO DRAM/page-mode ROM controllers
- Enhanced JTAG debugging (N-wire)
- UART, clocked serial interface, baud rate generator, and two timer/counters
- 20 interrupt sources with four programmable priority levels
- 16K of instruction and data cache/RAM
- Four-channel 8-/16-/32-bit DMA controller
- Three I/O ports
- 0.35-µm CMOS process technology
- 3.3V V_{DD}

BLOCK DIAGRAM



96YL-1131C (11/98)

FEATURE DESCRIPTION

CPU

200-MOPS MAC instruction

- High-performance microprocessor
  - Five-stage pipeline control
  - Thirty-two general-purpose 32-bit registers
  - 64-bit barrel shifter
  - 32-bit MAC unit
- Powerful RISC instruction set
  - 102 16- and 32-bit RISC instructions
  - Single-cycle MAC instruction (32 bits x 32 bits –> 64-bit result)
  - Saturated arithmetic operation (with a saturation detection function)
  - One- and two-cycle double-word shift (64-bit data)
  - High-speed lookahead branch
  - Block load/store instructions
- Fast instruction execution: 10 ns at 100 MHz

INTERRUPTS

- 20 maskable and prioritizable interrupts plus NMI
- Four programmable priority levels

MEMORY

- 4KB instruction RAM with 4K instruction cache (direct mapping)
- 4KB data RAM with 4K data cache (direct mapping/write through)
- 128-MB linear address memory space

EXTERNAL BUS INTERFACE

- Single and 16-byte burst transfer modes
- Separate 24-bit address and 32-bit data buses
- 32-/16-bit data bus sizing
- Bus hold/lock
- Seven chip select outputs

OTHER FUNCTIONS

- Sleep/stop modes
- Internal clocks (3x PLL)

PERIPHERALS

- DRAM controller (RAS/CAS and EDO mode)
- Page-mode ROM controller
- Two 16-bit timer/counters with five capture/compare registers
- UART and clocked serial ports with baud rate generator

DMA CONTROLLER

- Four-channel controller
- 16-MB byte count
- 128-MB address range
- Memory <-> memory and memory <-> I/O
- 32-/16-/8-bit data width
- External terminal count pin

DEVELOPMENT TOOLS

- High-performance optimized C compilers (NEC, Green Hills, MetroWerks)
- Real-time operating systems
- High-level language debugger with GUI
- ROM-ICE emulator
- N-wire ICE
- Evaluation board
- Middleware libraries
  - MH/MR/MMR
  - JBIG, JPEG, MPEG
  - SOFTMODEM
- PCI/I^2O compatibility

ORDERING INFORMATION

PART NUMBER	PACKAGE
µPD705101GM-100-8ED	160-pin plastic QFP (24 mm x 24 mm)

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For literature, call 1-800-366-9782 7 a.m. to 6 p.m. Pacific time
or fax your request to 1-800-729-9288
or visit our Web site at www.nec.com

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