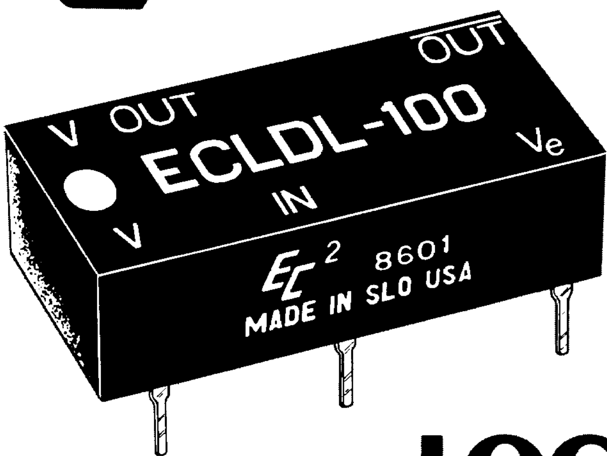
EC2

low profile

ECL COMPATIBLE LOGIC DELAY LINE



- ECL input and outputs
- Delay stable and precise
- 16-pin DIP package (.250 high)
- Available in delays from 2 to 1000ns
- Output isolated and with 70 ECL DC fan-out capacity
- Fast rise time on all outputs

design notes

The "DIP Series" Logic Delay Lines developed by Engineered Components Company have been designed to provide precise delays with required driving and pick-off circuitry contained in a single 16-pin DIP package compatible with ECL "10,000" series circuits. These Logic Delay Lines are of hybrid construction utilizing the proven technologies of active integrated circuitry and of passive networks utilizing capacitive, inductive and resistive elements. The ICs utilized in these modules are burned-in to Level B of MIL-STD-883 to ensure a high MTBF. The MTBF on these modules, when calculated per MIL-HDBK-217 for a 50°C ground fixed environment, is in excess of 3 million hours. Module design includes compensation for propagation delays and incorporates internal termination at the output; no additional external components are needed to obtain the desired delay.

The ECLDL is offered in 56 delays from 2 to 1000ns. Delay tolerances and rise times are maintained as shown in the accompanying Part Number Table, when tested under the "Test Conditions" shown. Delay time is measured at the −1.3V level on the leading edge; rise time is measured from 20% to 80% pulse amplitude. Temperature coefficient of delay is less than ±500 ppm/°C over the operating temperature range of −30 to +85°C.

These modules accept either logic "1" or logic "0" inputs and reproduce the logic at the output without inversion. The delay modules are intended primarily for use with positive going pulses and are calibrated to the tolerances shown in the table on rising edge delay; where best accuracy is desired in applications using falling edge timing, it is recommended that a special unit be calibrated for the specific application. Each module has the capability of driving up to 70 ECL DC loads.

These "DIP Series" modules are packaged in a 16-pin DIP housing, molded of flame-proof Diallyl Phthalate per MIL-M-14, type SDG-F, and are fully encapsulated in epoxy resin. Flat metal leads meet the solderability requirements of MIL-STD-202, Method 208. Leads provide positive stand off from the printed circuit board to permit solder-fillet formation and flush cleaning of solder-flux residues for improved reliability.

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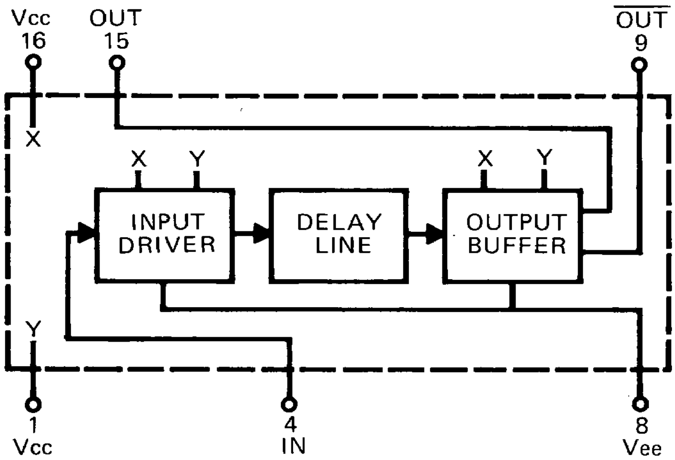
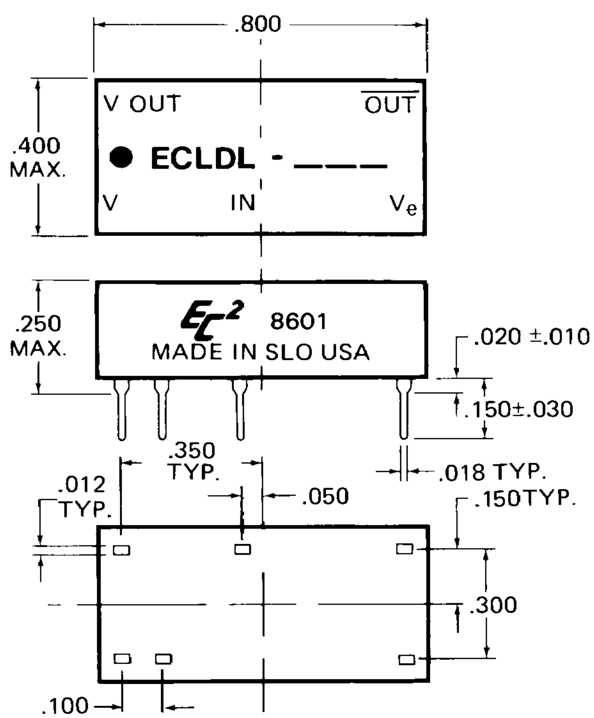
DESIGN NOTES (continued)

Marking consists of manufacturer's name, logo (EC2), part number, terminal identification and date code of manufacture. All marking is applied by silk screen process using white epoxy paint in accordance with MIL-STD-130, to meet the permanency of identification required by MIL-STD-202, Method 215.

BLOCK DIAGRAM IS SHOWN BELOW



MECHANICAL DETAIL IS SHOWN BELOW



TEST CONDITIONS

1. All measurements are made at 25°C.
2. Vee supply voltage is maintained at −5.2V DC.
3. All units are tested using a positive input pulse provided by a standard open emitter ECL 10,000 gate. The input and output utilize a 100 ohm pulldown resistor to −2V; the output is also loaded with one ECL 10,000 gate.

ϕ 4. Input pulse width used is 100% longer than delay of module under test; spacing between pulses (falling edge to rising edge) is three times the pulse width used.

OPERATING SPECIFICATIONS

* Supply voltage: . . . . −5.2V ±5% to Vee (can be operated on +5V to Vcc).

Supply current: . . . . 40ma typical

Logic 1 input at 25°C:

Voltage . . . . −.98 min.

Current . . . . 265ua max.

Logic 0 input at 25°C:

Voltage . . . . −1.63 max.

Current . . . . .5ua min.

Logic 1 Voltage out at 25°C: . . . . −.96 min.

Logic 0 Voltage out at 25°C: . . . . −1.65 max.

Operating temperature range: . . . . −30 to +85°C

Storage temperature: . . . . −55 to +125°C

* Delays increase or decrease less than 1% for a respective increase or decrease of 5% in supply voltage.

PART NUMBER TABLE

ϕ DELAYS AND TOLERANCES (in ns)					
Part Number	Rise Time Max.	Output	Part Number	Rise Time Max.	Output
ECLDL-2	2	2 ±.3	ECLDL-50	9	50 ±2
ECLDL-3	2	3 ±.4	ECLDL-55	9	55 ±2
ECLDL-4	3	4 ±.5	ECLDL-60	10	60 ±2
ECLDL-5	3	5 ±1	ECLDL-65	10	65 ±2.5
ECLDL-6	3	6 ±1	ECLDL-70	11	70 ±2.5
ECLDL-7	3	7 ±1	ECLDL-75	11	75 ±2.5
ECLDL-8	3	8 ±1	ECLDL-80	12	80 ±2.5
ECLDL-9	3	9 ±1	ECLDL-85	13	85 ±3
ECLDL-10	4	10 ±1	ECLDL-90	13	90 ±3
ECLDL-11	4	11 ±1	ECLDL-95	14	95 ±3
ECLDL-12	4	12 ±1	ECLDL-100	15	100 ±3
ECLDL-13	4	13 ±1	ECLDL-125	18	125 ±4
ECLDL-14	4	14 ±1	ECLDL-150	20	150 ±4.5
ECLDL-15	5	15 ±1	ECLDL-175	23	175 ±5
ECLDL-16	5	16 ±1	ECLDL-200	25	200 ±6
ECLDL-17	5	17 ±1	ECLDL-225	25	225 ±7
ECLDL-18	5	18 ±1	ECLDL-250	25	250 ±8
ECLDL-19	5	19 ±1	ECLDL-275	25	275 ±9
ECLDL-20	5	20 ±1	ECLDL-300	30	300 ±10
ECLDL-21	6	21 ±1	ECLDL-350	30	350 ±11
ECLDL-22	6	22 ±1	ECLDL-400	30	400 ±12
ECLDL-23	6	23 ±1	ECLDL-450	30	450 ±14
ECLDL-24	6	24 ±1	ECLDL-500	30	500 ±15
ECLDL-25	6	25 ±1	ECLDL-600	30	600 ±18
ECLDL-30	7	30 ±1.5	ECLDL-700	30	700 ±20
ECLDL-35	7	35 ±1.5	ECLDL-800	30	800 ±22
ECLDL-40	8	40 ±1.5	ECLDL-900	30	900 ±24
ECLDL-45	8	45 ±2	ECLDL-1000	30	1000 ±26

ϕ All modules can be operated with a minimum input pulse width of 100% of full delay and pulse period approaching square wave; since delay accuracies may be somewhat degraded, it is suggested that the module be evaluated under the intended specific operating conditions. Special modules can be readily manufactured to improve accuracies and/or provide customer specified random delay times for specific applications.

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