IS25C32B

32K-BIT SPI SERIAL CMOS EEPROM

Advanced Information
JULY 2009

FEATURES

- Serial Peripheral Interface (SPI) Compatible
  — Supports SPI Modes 0 (0,0) and 3 (1,1)
- Wide Voltage Operation
  — Vcc = 1.8V to 5.5V
- Low power CMOS
  — Active current less than 1 mA (1.8V)
  — Standby current less than 1 µA (1.8V)
- Block Write Protection
  — Protect 1/4, 1/2, or Entire Array
- 32 byte page write mode
  — Partial page writes allowed
- 10 MHz Clock Rate (5V)
- Self timed write cycles
  — 5 ms max @ 2.5V
- High-reliability
  — Endurance: 1 million cycles
  — Data retention: 100 years
- Packages (8-pin): SOIC/SOP, TSSOP, PDIP, and DFN

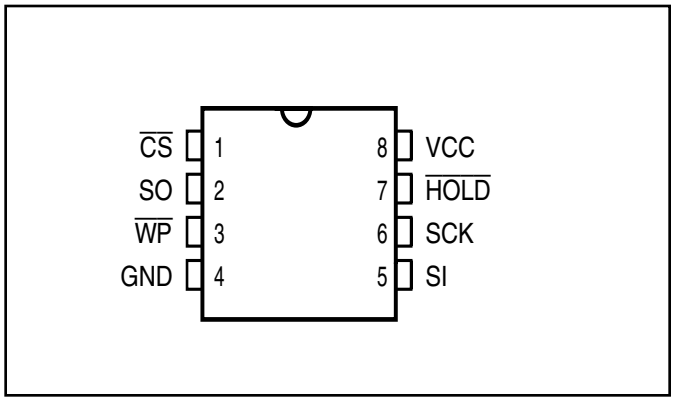
DESCRIPTION

The IS25C32B is an electrically erasable PROM device that uses the Serial Peripheral Interface (SPI) for communications. The IS25C32B is 32Kbit (4096 x 8). It is offered in a wide operating voltage range of 1.8V to 5.5V to be compatible with most application voltages. ISSI designed the IS25C32B to be an efficient SPI EEPROM solution. The devices are packaged in 8-pin SOIC, 8-pin TSSOP, 8-pin PDIP, and 8-pad DFN.

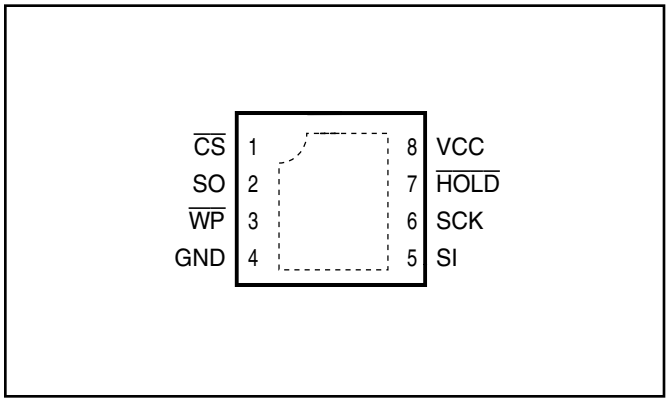
The functional features of the IS25C32B allows them to be among the most advanced serial non-volatile memories available. Each device has a Chip-Select ($\overline{CS}$) pin, and a 3-wire interface of Serial Data In (SI), Serial Data Out (SO), and Serial Clock (SCK). While the 3-wire interface of the IS25C32B provides for high-speed access, a $\overline{HOLD}$ pin allows the memories to ignore the interface in a suspended state; later the $\overline{HOLD}$ pin reactivates communication without re-initializing the serial sequence. A Status Register facilitates a flexible write protection mechanism, and a device-ready bit ($\overline{RDY}$).

PIN CONFIGURATION

8-Pin DIP, SOIC, and TSSOP



8-pad DFN



PIN DESCRIPTIONS

$\overline{CS}$	Chip Select
SCK	Serial Data Clock
SI	Serial Data Input
SO	Serial Data Output
GND	Ground
V_{CC}	Power
$\overline{WP}$	Write Protect
$\overline{HOLD}$	Suspends Serial Input

PIN DESCRIPTIONS

Serial Clock (SCK): This timing signal provides synchronization between the microcontroller and IS25C32B. Op-Codes, byte addresses, and data are latched on SI with a rising edge of the SCK. Data on SO is refreshed on the falling edge of SCK for SPI modes (0,0) and (1,1).

Serial Data Input (SI): This is the input pin for all data that the IS25C32B is required to receive.

Serial Data Output (SO): This is the output pin for all data transmitted from the IS25C32B.

Chip Select ($\overline{CS}$): The $\overline{CS}$ pin activates the device. Upon power-up, $\overline{CS}$ should follow Vcc. When the device is to be enabled for instruction input, the signal requires a High-to-Low transition. While $\overline{CS}$ is stable Low, the master and slave will communicate via SCK, SI, and SO signals. Upon completion of communication, $\overline{CS}$ must be driven High. At this moment, the slave device may start its internal write cycle. When $\overline{CS}$ is high, the device enters a power-saving standby mode, unless an internal write operation is underway. During this mode, the SO pin becomes high impedance.

Write Protect ($\overline{WP}$): The purpose of this input signal is to initiate Hardware Write Protection mode. This mode prevents the Block Protection bits and the WPEN bit in the Status Register from being altered. To cause Hardware Write Protection, $\overline{WP}$ must be Low at the same time WPEN is 1. $\overline{WP}$ may be hardwired to Vcc or GND.

HOLD ($\overline{HOLD}$): This input signal is used to suspend the device in the middle of a serial sequence and temporarily ignore further communication on the bus (SI, SO, SCK). Together with Chip Select, the $\overline{HOLD}$ signal allows multiple slaves to share the bus. The $\overline{HOLD}$ signal transitions must occur only when SCK is Low, and be held stable during SCK transitions. (See Figure 8 for Hold timing) To disable this feature, $\overline{HOLD}$ may be hardwired to Vcc.

SERIAL INTERFACE DESCRIPTION

MASTER: The device that provides a clock signal.

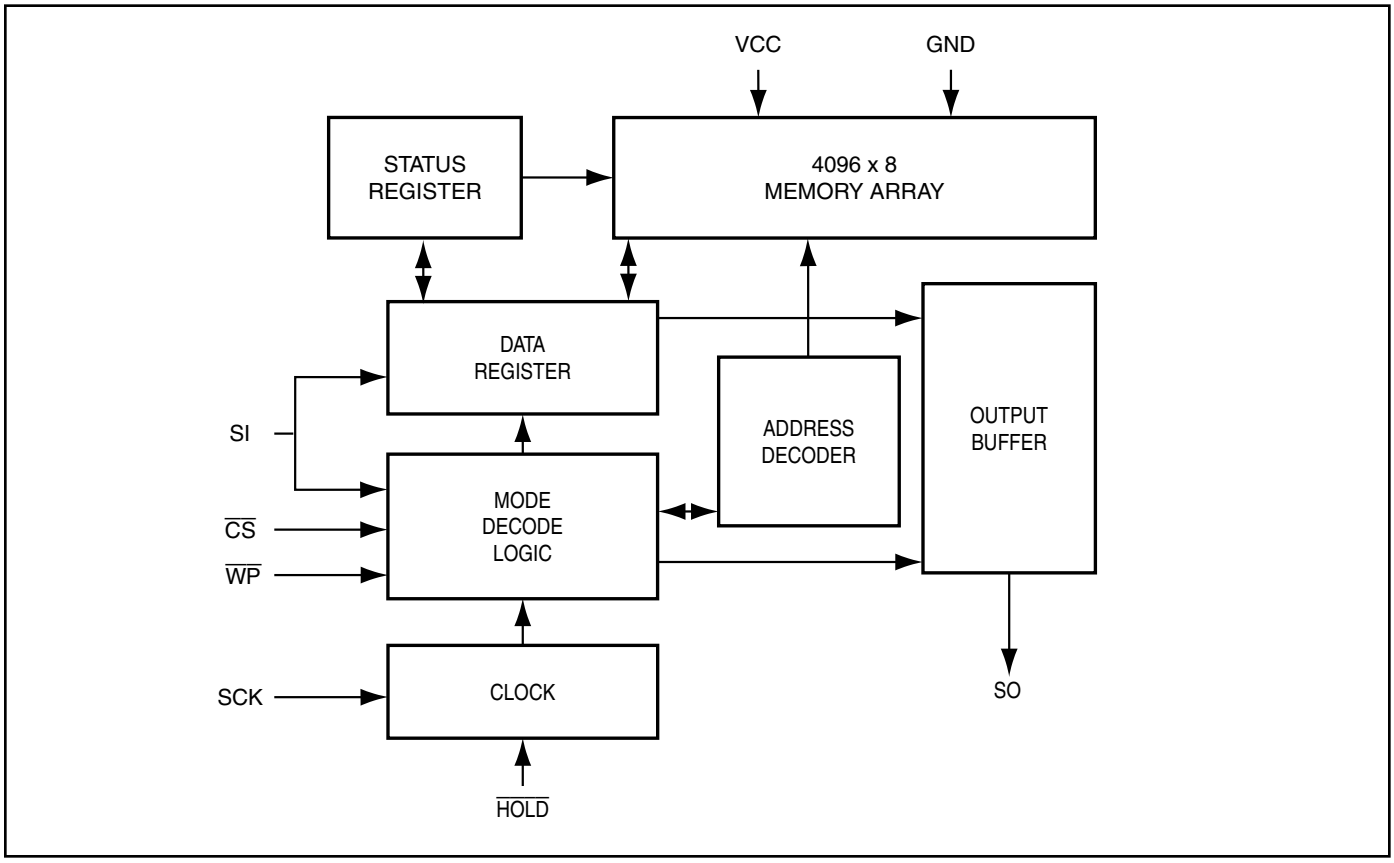
SLAVE: The IS25C32B is a slave because the clock signal is an input.

TRANSMITTER/RECEIVER: The IS25C32B has both data input (SI) and data output (SO).

MSB: The most significant bit. It is always the first bit transmitted or received.

OP-CODE: The first byte transmitted to the slave following CS transition to LOW. If the OP-CODE is a valid member of the IS25C32B instruction set (Table 3), then it is decoded appropriately. If the OP-CODE is not valid, and the SO pin remains in high impedance.

BLOCK DIAGRAM



STATUS REGISTER

The status register contains 8-bits for write protection control and write status. (See Table 1). It is the only region of memory other than the main array that is accessible by the user.

Table 1. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
WPEN	X	X	X	BP1	BP0	WEN	$\overline{RDY}$

Notes:
1. X = Don't care bit.
2. During internal write cycles, bits 0 to 7 are temporarily 1's.

The Status Register is Read-Only if either: a) Hardware Write Protection is enabled or b) WEN is set to 0. If neither is true, it can be modified by a valid instruction.

Ready ($\overline{RDY}$), Bit 0: When $\overline{RDY}$ = 1, it indicates that the device is busy with a write cycle. $\overline{RDY}$ = 0 indicates that the device is ready for an instruction. If $\overline{RDY}$ = 1, the only command that will be handled by the device is Read Status Register.

Write Enable (WEN), Bit 1: This bit represents the status of device write protection. If WEN = 0, the Status Register and the entire array is protected from modification, regardless of the setting of WPEN, $\overline{WP}$ pin, or block protection. The only way to set WEN to 1 is via the Write Enable command (WREN). WEN is reset to 0 upon power-up.

Block Protect (BP1, BP0), Bits 2-3: Together, these bits represent one of four block protection configurations implemented for the memory array. (See Table 2 for details.)
BP0 and BP1 are non-volatile cells similar to regular array cells, and factory programmed to 0. The block of memory defined by these bits is always protected, regardless of the setting of WPEN, $\overline{WP}$, or WEN.

Table 2. Block Protection

	Status Register Bits		Array Addresses Protected
Level	BP1	BP0	IS25C32B
0	0	0	None
1(1/4)	0	1	0C00h -0FFFh
2(1/2)	1	0	0800h -0FFFh
3(All)	1	1	0000h -0FFFh

Don't Care, Bits 4-6: Each of these bits can receive either 0 or 1, but values will not be retained. When these bits are read from the register, they are always 0.

Write Protect Enable (WPEN), Bit 7: This bit can be used in conjunction with $\overline{WP}$ pin to enable Hardware Write Protection, which causes the Status Register to be read-only. The memory array is not protected by this mode. Hardware Write Protection requires that $\overline{WP}$ = 0 *and* WPEN = 1; it is disabled otherwise. Note: WPEN cannot be changed from 1 to 0 if the $\overline{WP}$ pin is already set to Low. (See Table 4 for data protection relationship)

DEVICE OPERATION

The operations of the IS25C32B are controlled by a set of instructions that are clocked-in serially SI pin. (See Table 3). To begin an instruction, the chip select ($\overline{CS}$) should be dropped Low. Subsequently, each Low-to-High transition of the clock (SK) will latch a stable value on the SI pin. After the 8-bit op-code, it may be appropriate to continue to input an address or data to SI, or to output data from SO. During data output, values appear on the falling edge of SK. All bits are transferred with MSB first. Upon the last bit of communication, but prior to any following Low-to-High transition of SK, $\overline{CS}$ should be raised High to end the transaction. The device then would enter Standby Mode if no internal programming were underway.

Table 3. Instruction Set

Name	Op-code	Operation	Address	Data(SI)	Data (SO)
WREN	0000 X110	Set Write Enable Latch	-	-	-
WRDI	0000 X100	Reset Write Enable Latch	-	-	-
RDSR	0000 X101	Read Status Register	-	-	D7-D0,...
WRSR	0000 X001	Write Status Register	-	D7-D0	-
READ	0000 X011	Read Data from Array	A15-A0	-	D7-D0,...
WRITE	0000 X010	Write Data to Array	A15-A0	D7-D0,...	-

1. X = Don't care bit. For consistency, it is best to use "0".
2. Some address bits are don't care. See Table 5.
3. If the bits clocked-in for an op-code are invalid, SO remains high impedance, and upon CS going High there is no affect. A valid op-code with an invalid number of bits clocked-in for address or data will cause an attempt to modify the array or Status Register to be ignored.

WRITE ENABLE (WREN)

When Vcc is initially applied, the device powers up with both status register and entire array in a write-disabled state. Upon completion of Write Disable (WRDI), Write Status Register (WRSR), or Write Data to Array (WRITE), the device resets the WEN bit in the Status Register to 0. Prior to any data modification, a WREN instruction is necessary to set WEN to 1. (See Figure 2 for timing).

WRITE DISABLE (WRDI)

The device can be completely protected from modification by resetting WEN to 0 through the WRDI instruction. (See Figure 3 for timing).

READ STATUS REGISTER (RDSR)

The Read Status instruction tells the user the status of Write Protect Enable, the Block Protection setting (see Table 2), the Write Enable state, and the $\overline{RDY}$ status. RDSR is the only instruction accepted when a write cycle is underway. It is recommended that the status of Write Enable and $\overline{RDY}$ be checked, especially prior to an attempted modification of data. The 8 bits of the Status Register can be repeatedly output on SO after the initial Op-code. (See Figure 4 for timing).

WRITE STATUS REGISTER (WRSR)

This instruction lets the user choose a Block Protection setting, and set or reset the WPEN bit. The values of the other data bits incorporated into WRSR can be 0 or 1, and are not stored in the Status Register. WRSR will be ignored unless both the following are true: a) WEN = 1, due to a prior WREN instruction; and b) Hardware Write Protection is not enabled. (See Table 4 for details). Except for the $\overline{RDY}$ status, the values in the Status Register remain unchanged until the moment when the write cycle is complete and the register is updated. Note: WPEN can be changed from 1 to 0 only if $\overline{WP}$ is already set High. Once completed, WEN is reset for complete chip write protection. (See Figure 5 for timing).

READ DATA (READ)

This instruction begins with the op-code and the 16-bit address, and causes the selected data byte to be shifted out on SO. Following this first data byte, additional sequential bytes are output. If the data byte in the highest address is output, the address rolls-over to the lowest address in the array, and the output could loop indefinitely. At any time, a rising $\overline{CS}$ signal completes the operation. (See Figure 6 for timing).

WRITE DATA (WRITE)

The WRITE instruction begins with the op-code, the 16-bit address of the first byte to be modified, and the first data byte. Additional data bytes may be written sequentially to the array after the first byte. Each WRITE instruction can affect the contents of a 32 byte page, but no more. The page begins at address XXXXXXXX XXX00000, and ends with XXXXXXXX XXX11111. If the last byte of the page is input, the address rolls over to the beginning of the same page. More than 32 data bytes can be input during the same instruction, but upon a completed write cycle, a page would only contain the last 32 bytes.

The region of the array defined within Block Protection cannot be modified as long as that block configuration is selected. The region of the array outside the Block Protection can only be modified if Write Enable (WEN) is set to 1. Therefore, it may be necessary that a WREN instruction occur prior to WRITE. Hardware Write Protection has no affect on the memory array. Once Write is completed, WEN is reset for complete chip write protection. (See Figure 7 for timing).

Table 5. Address Key

Name	IS25C32B
A_N	A_{11}-A_0
Don't Care Bits	A_{15}-A_{12}

Table 4. Write Protection

WPEN	$\overline{WP}$	Hardware Write Protection	WEN	Inside Block	Outside Block	Status Register (WPEN, BP1, BP0)
0	X	Not Enabled	0	Read-only	Read-only	Read-only
0	X	Not Enabled	1	Read-only	Unprotected	Unprotected
1	0	Enabled	0	Read-only	Read-only	Read-only
1	0	Enabled	1	Read-only	Unprotected	Read-only
X	1	Not Enabled	0	Read-only	Read-only	Read-only
X	1	Not Enabled	1	Read-only	Unprotected	Unprotected

Note: X = Don't care bit.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	-0.5 to + 6.5	V
V_P	Voltage on Any Pin	–0.5 to Vcc + 0.5	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	Output Current	5	mA

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE (IS25C32B-2)

Vcc	Ambient Temperature	Grade
1.8V to 5.5V	–40°C to +85°C	Industrial

CAPACITANCE(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters and not 100% tested.
2. Test conditions: T_A = 25°C, f = 1 MHz, Vcc = 5.0V.

DC ELECTRICAL CHARACTERISTICS

T_A = –40°C to +85°C (Industrial)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{CC1}	Operating Current	Read/Write at 5 MHz (Vcc = 1.8V)	—	1.0	mA
I_{CC2}	Operating Current	Read/Write at 10 MHz (Vcc = 2.5V)	—	3.0	mA
I_{CC3}	Operating Current	Read/Write at 10 MHz (Vcc = 5V)	—	5.0	mA
I_{SB1}	Standby Current	Vcc = 1.8V, V_{IN} = V_{CC} or GND $\overline{CS}$ = Vcc	—	1.0	µA
I_{SB2}	Standby Current	Vcc = 2.5V, V_{IN} = V_{CC} or GND $\overline{CS}$ = Vcc	—	2.0	µA
I_{SB3}	Standby Current	Vcc = 5.0V, V_{IN} = V_{CC} or GND $\overline{CS}$ = Vcc	—	3.0	µA
V_{OL1}	Output LOW Voltage	V_{CC} = 1.8V, I_{OL} = 0.15 mA	—	0.2	V
V_{OL2}	Output LOW Voltage	V_{CC} = 2.5V, I_{OL} = 1.5 mA	—	0.4	V
V_{OL3}	Output LOW Voltage	V_{CC} = 5V, I_{OL} = 2 mA	—	0.4	V
V_{OH1}	Output HIGH Voltage	V_{CC} = 1.8V, I_{OH} = -0.1mA	0.8 x V_{CC}	—	V
V_{OH2}	Output HIGH Voltage	V_{CC} = 2.5V, I_{OH} = -0.4mA	0.8 x V_{CC}	—	V
V_{OH3}	Output HIGH Voltage	V_{CC} = 5V, I_{OH} = -2 mA	0.8 x V_{CC}	—	V
V_{IH}	Input HIGH Voltage		0.7x V_{CC}	V_{CC} + 1	V
V_{IL}	Input LOW Voltage		-0.3	0.3 x V_{CC}	V
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}	-2	2	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}, $\overline{CS}$ = V_{CC}	-2	2	µA

AC Characteristics

T_A = –40°C to +85°C (Industrial)

Symbol	Parameter	1.8V ≤ Vcc < 2.5V Min	1.8V ≤ Vcc < 2.5V Max	2.5V ≤ Vcc < 5.5V Min	2.5V ≤ Vcc < 5.5V Max	Units
f_{SCK}	SCK Clock Frequency	0	5	0	10	MHz
t_{RI}	Input Rise Time	—	2	—	2	µs
t_{FI}	Input Fall Time	—	2	—	2	µs
t_{WH}	SCK High Time	80	—	40	—	ns
t_{WL}	SCK Low Time	80	—	40	—	ns
t_{CS}	$\overline{CS}$ High Time	100	—	50	—	ns
t_{CSS}	$\overline{CS}$ Setup Time	100	—	50	—	ns
t_{CSH}	$\overline{CS}$ Hold Time	100	—	50	—	ns
t_{SU}	Data In Setup Time	20	—	10	—	ns
t_H	Data In Hold Time	20	—	10	—	ns
t_{HD}	$\overline{Hold}$ Setup Time	20	—	10	—	ns
t_{CD}	$\overline{Hold}$ Hold Time	20	—	10	—	ns
t_V	Output Valid	0	80	0	40	ns
t_{HO}	Output Hold Time	0	—	0	—	ns
t_{LZ}	$\overline{Hold}$ to Output Low Z	0	80	0	40	ns
t_{HZ}	$\overline{Hold}$ to Output High Z	—	80	—	40	ns
t_{DIS}	Output Disable Time	—	80	—	40	ns
t_{WC}	Write Cycle Time	—	5	—	5	ms

C_L = 100pF

TIMING DIAGRAMS

Figure 1. Synchronous Data Timing

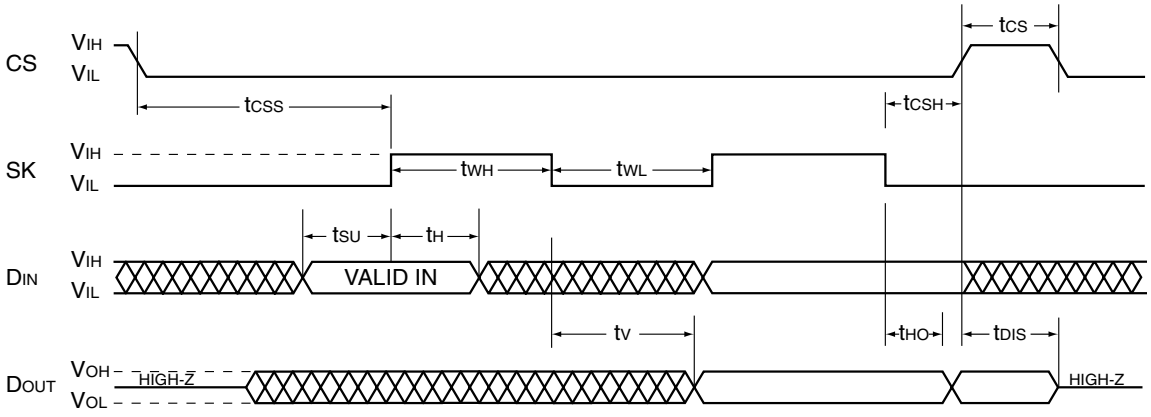


Figure 2. WREN Timing

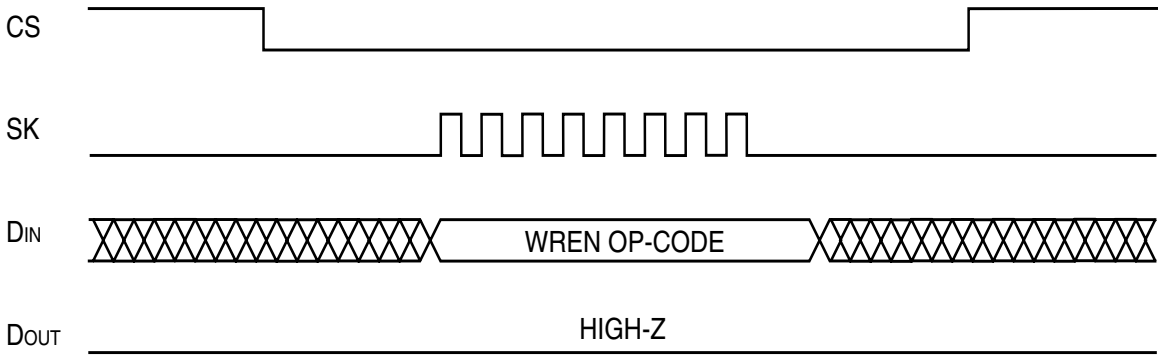


Figure 3. WRDI Timing

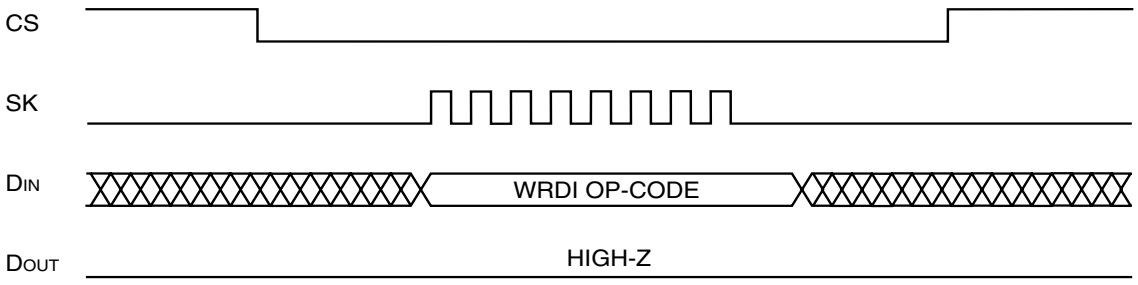


Figure 4. RDSR Timing

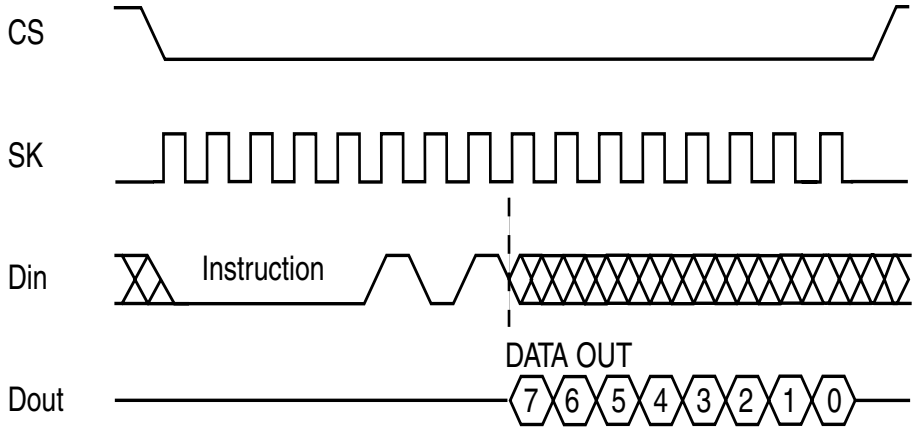


Figure 5. WRSR Timing

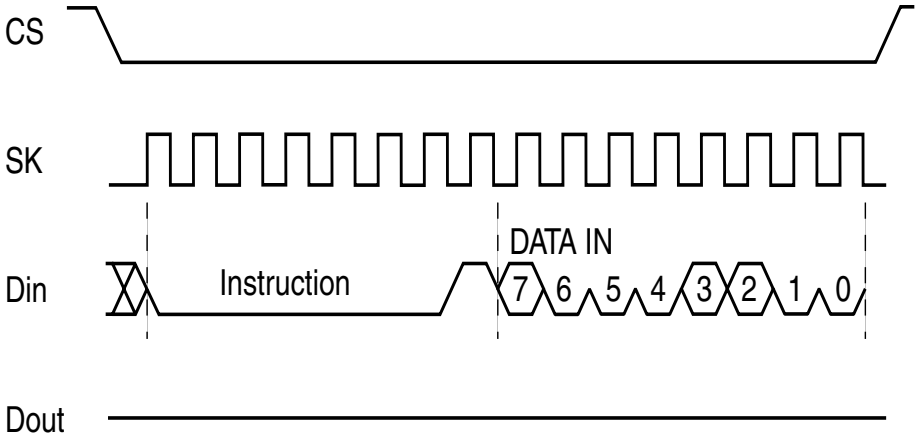


Figure 6. READ Timing

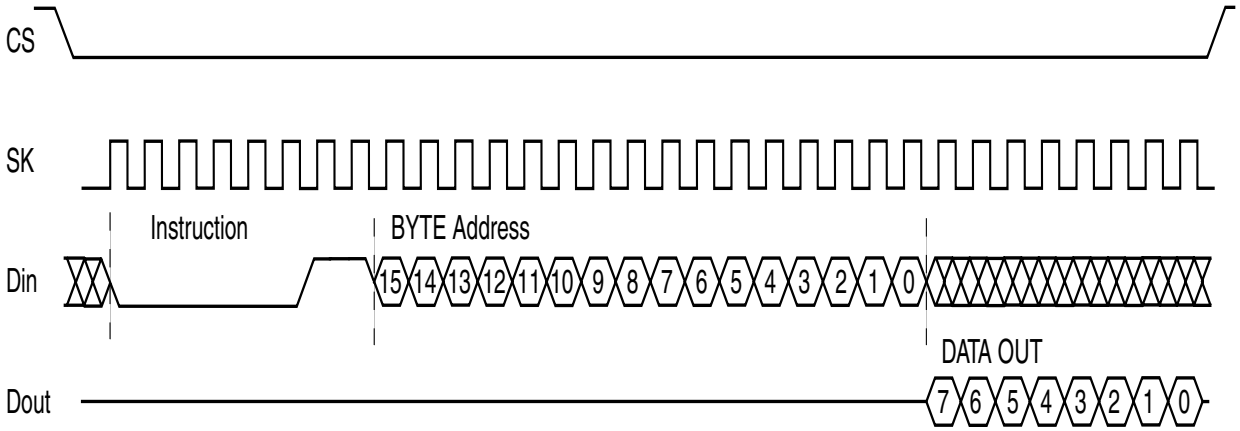


Figure 7. WRITE Timing

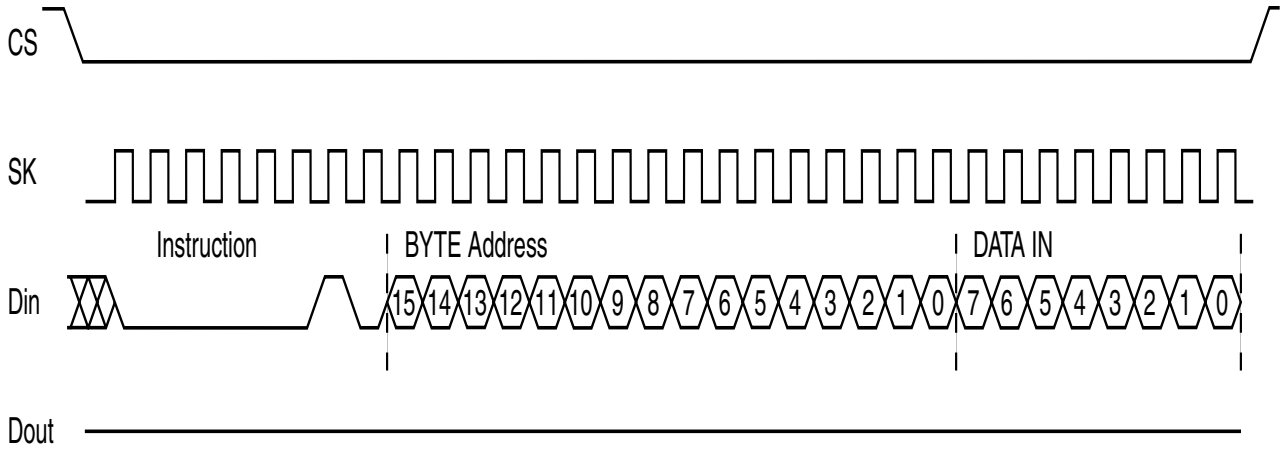
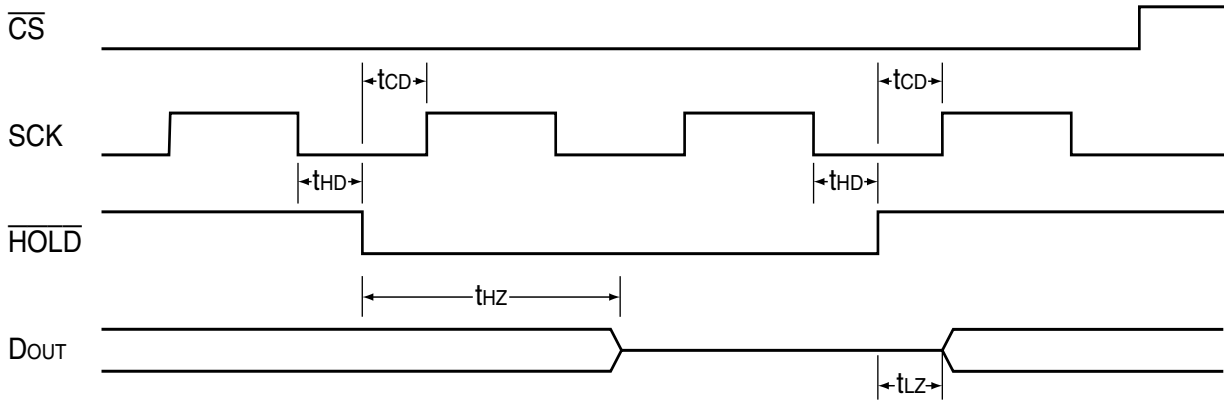


Figure 8. $\overline{\text{HOLD}}$ Timing



ORDERING INFORMATION

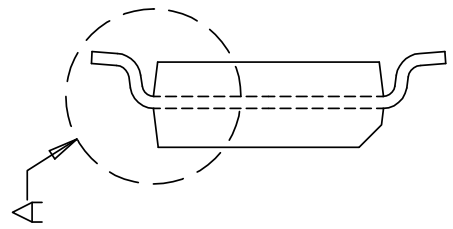
Industrial Range: -40°C to +85°C, Lead-free

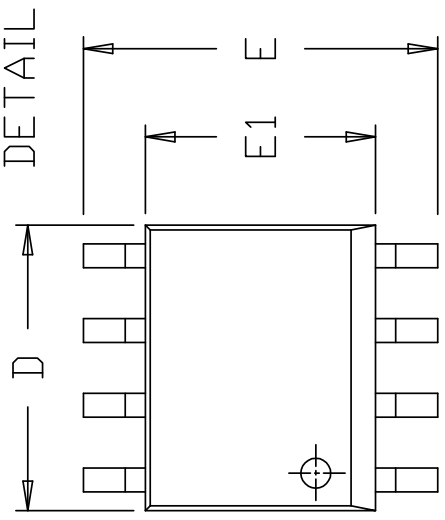
Voltage Range	Part Number	Package (8-pin)*
1.8V to 5.5V	IS25C32B-2GLI	150 mil SOIC (JEDEC STD)
	IS25C32B-2ZLI	3 x 4.4 mm TSSOP
	IS25C32B-2PLI	Plastic DIP
	IS25C32B-2DLI-TR	2 x 3 mm DFN

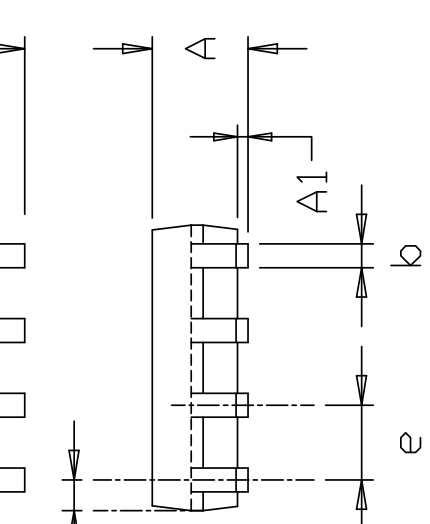
*

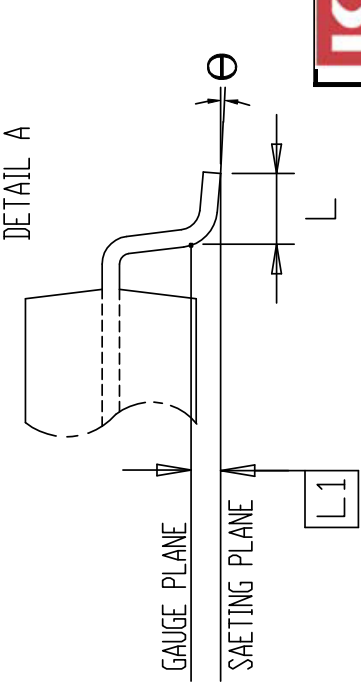
1. Contact ISSI Sales Representatives for availability and other package information.
2. Most listed part numbers are packed in tube, except DFN in tape and reel “-TR”.
3. For tape and reel, add “-TR” at the end of the P/N (4K per reel). DFN is 5K per reel.
4. Refer to ISSI website for related declaration document on lead free, RoHS, halogen free, or Green, whichever is applicable.
5. ISSI offers Industrial grade for Commercial applications (0°C to +70°C).

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	—	1.75	0.053	—	0.069
A1	0.10	—	0.25	0.004	—	0.010
b	0.33	—	0.51	0.013	—	0.020
D	4.80	—	5.00	0.189	—	0.197
E	5.80	—	6.20	0.228	—	0.244
E1	3.80	—	4.00	0.150	—	0.157
e	1.27 BSC.			0.050 BSC.		
L	0.38	—	1.27	0.015	—	0.050
L1	0.25 BSC.			0.010 BSC.		
ZD	0.545 REF.			0.021 REF.		
θ	0	—	8°	0	—	8°









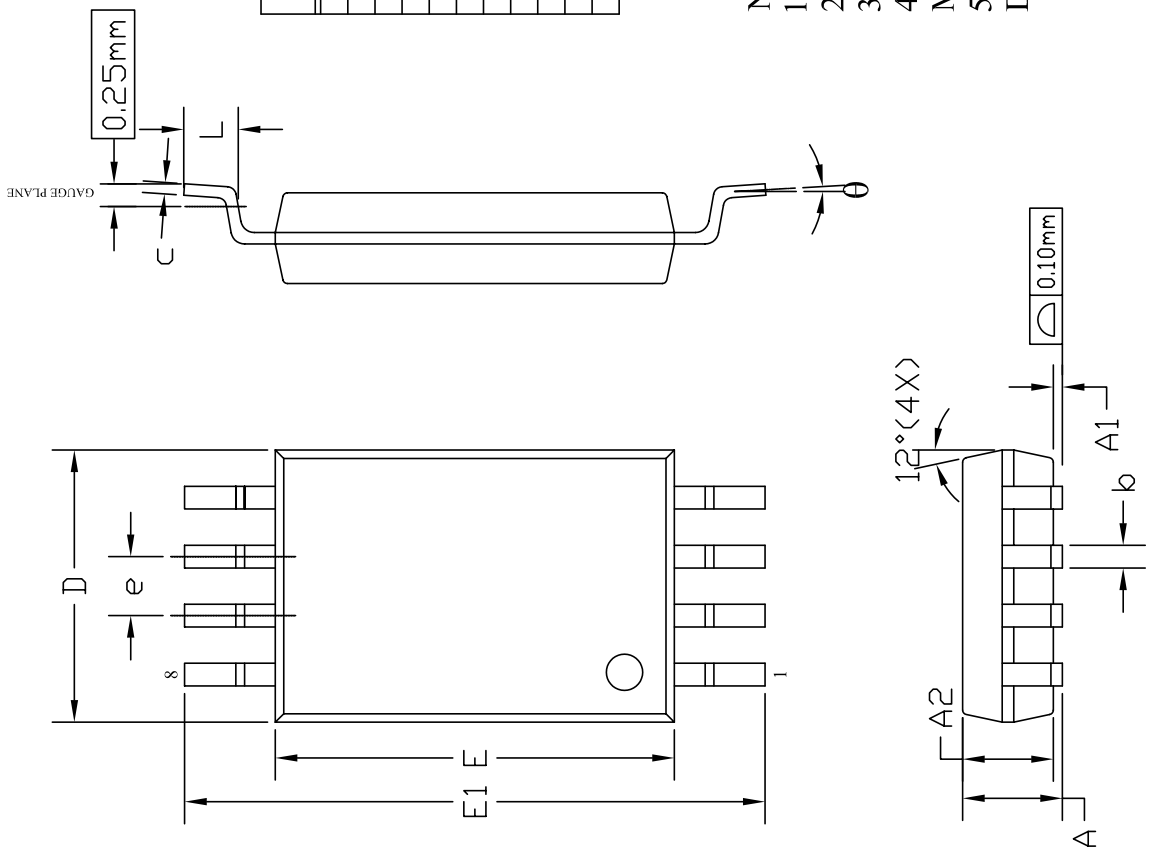
NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

	TITLE	8L 150mil SOP Package Outline	REV.	B	DATE	07/20/2001

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	—	0.30	0.007	—	0.012
c	0.09	—	0.20	0.004	—	0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E1	6.40 BSC			0.252 BSC		
E	4.30	4.40	4.50	0.169	0.173	0.177
e	0.65 BSC			0.026 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
θ	0°	—	8°	0°	—	8°

NOTE
1. CONTROLLING DIMENSION IS MILLIMETER.
2. REFER TO JEDEC STANDARD MO-153 AA.
3. PACKAGE MAY HAVE EXPOSED TIE BAR.
4. DIMENSION "D" AND "E1" DOES NOT INCLUDE MOLD PROTRUSION.
5. DIMENSION "b" DOES NOT INCLUDE DAM BAR PROTRUSION.

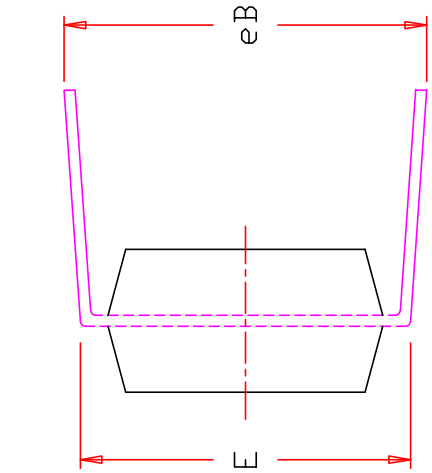


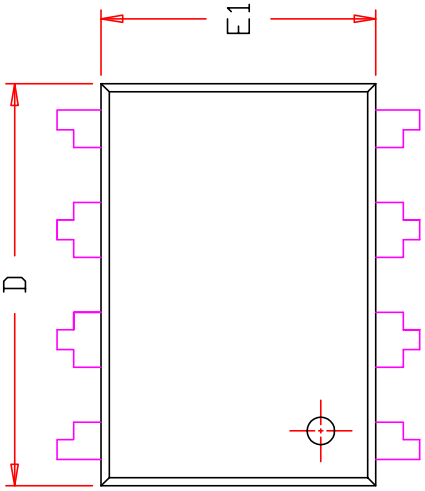
ISSI	TITLE	8L 3x4.4mm TSSOP Package Outline	REV. A	DATE 5/11/2009

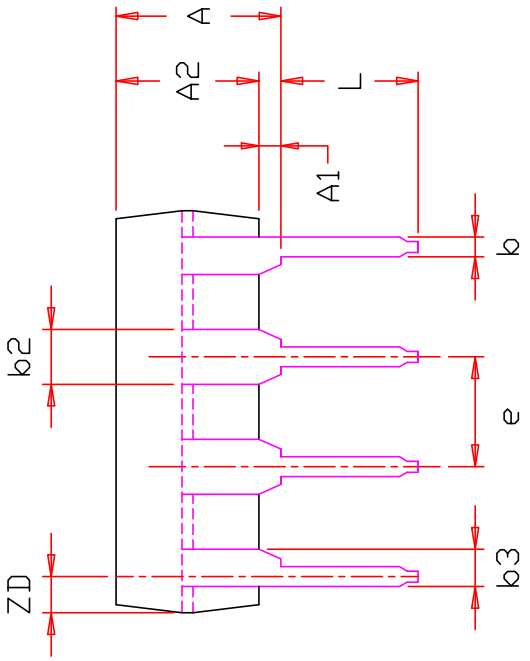
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	3.60	—	4.20	0.142	—	0.165
A1	0.38	—	0.75	0.015	—	0.030
A2	3.25	—	3.45	0.128	—	0.136
b	0.36	—	0.56	0.014	—	0.022
b2	1.40	—	1.65	0.055	—	0.065
b3	0.81	—	1.17	0.032	—	0.046
D	9.01	—	9.53	0.355	—	0.375
E	7.49	—	8.26	0.295	—	0.325
E1	6.20	—	6.60	0.244	—	0.260
e	2.54 BSC.			0.100 BSC.		
eB	8.12	—	9.65	0.320	—	0.380
L	3.18	—	3.80	0.125	—	0.150
ZD	0.825 REF.			0.032 REF.		

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b2 AND b3 DO NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

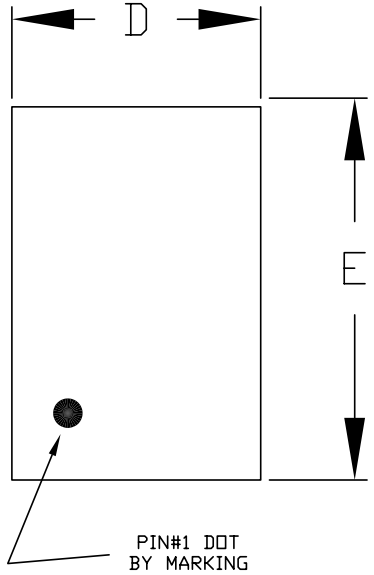




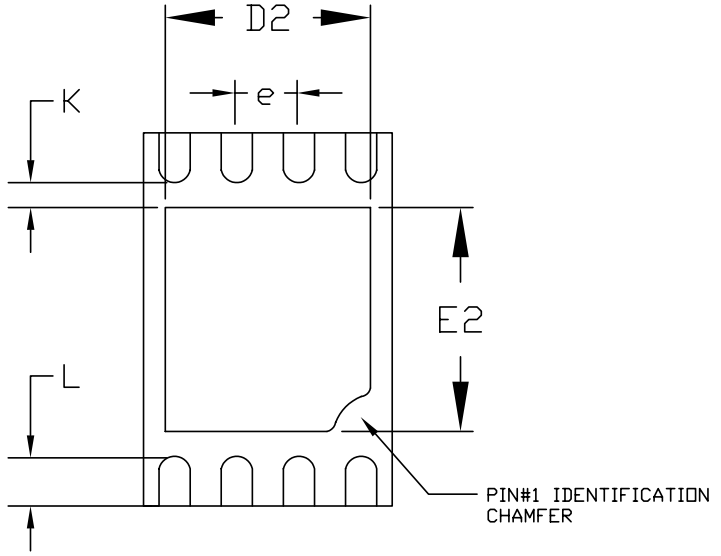


ISSI	TITLE	8L 300mil PDIP Package Outline	REV.	C	DATE	05/08/2009

280-600-011 REV. A



TOP VIEW



BOTTOM VIEW

SIDE VIEW

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
A3		0.20 REF			0.008 REF	
D		2.00 REF			0.079 REF	
D2	1.50	—	1.75	0.059	—	0.069
E		3.00 REF			0.118 REF	
E2	1.65	—	1.90	0.065	—	0.075
e		0.50 BSC			0.020 BSC	
K		0.2 REF			0.008 REF	
L	0.30	0.40	0.50	0.012	0.016	0.020

NOTE
1. CONTROLLING DIMENSION IS MILLIMETER.
2. Refer to JEDEC Drawing MO-229.
3. Package may have exposed tie bars, ending flush with package edge.

ISSI	TITLE	8L 2x3mm DFN Package Outline	REV.	A	DATE	1/8/2009

REVISION HISTORY

Rev.	Date	Description
00A	January 2007	Draft version
00B	June 2008	Initial version
00C	July 2009	Advanced version