N-CHANNEL ENHANCEMENT—MODE D-MOS POWER FET

FEATURES

- Lateral D-MOS Design
- Low ON Resistance — 1.1 ohms (typ)
- Extremely Low Drive Current
- Bi-Direction

APPLICATIONS

- Broadband, High-Gain, RF Power Amplifiers
- Bi-Directional Logic Compatible Switches
- High Speed Line Drivers
- Bi-Directional Power Switches

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

V_{DS}	Drain-Source Voltage	+25V
V_{SD}	Source-Drain Voltage	+15V
V_{DB}	Drain-Body Voltage	+20V −0.3V
V_{SB}	Source-Body Voltage	+20V −0.3V
V_{GS}	Gate-Source Voltage	±30V
V_{GD}	Gate-Drain Voltage	±30V
V_{GB}	Gate-Body Voltage	±30V
$I_{D(on)}$	Continuous Drain Current (Note 1, Note 3)	2.0A
$I_{D(on)}$	Peak Drain Current (Note 1, Note 3)	3.0A

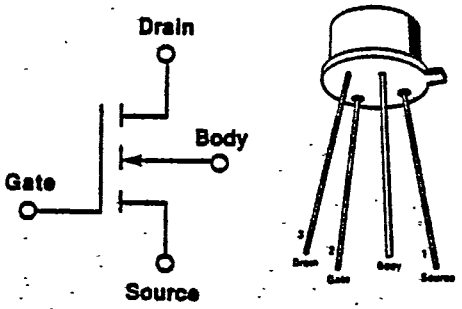
P_D	Continuous Power Dissipation (Note 1)	
	T_A = +25°C (Note 2)	1.0W
	T_C = +25°C (Note 3)	5.0W
	Power Derating Factors (Note 1)	
	Free Air	10mW/°C
	Infinite Heat Sink	50mW/°C
	Thermal Resistance (Note 1)	
θ_{ja}	Junction to Ambient	100°C/W
θ_{jc}	Junction to Case	20°C/W
T_{op}	Operating Junction Temperature Range	−55 to +125°C
T_{stg}	Storage Temperature Range	−55 to +150°C

Note 1: Not applicable to chips. Final value depends upon mounting.
Note 2: Free Air
Note 3: Infinite Heat Sink

ORDERING INFORMATION

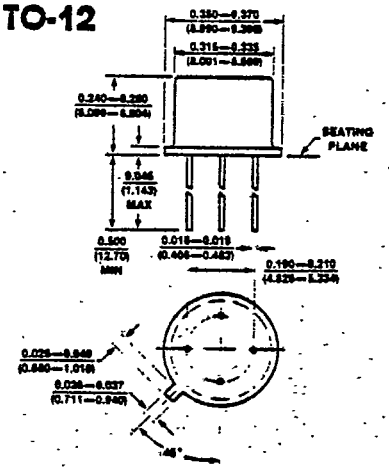
Sorted Chips in Carriers	XSD224
TO-12 Package	SD224H

SCHEMATIC DIAGRAM



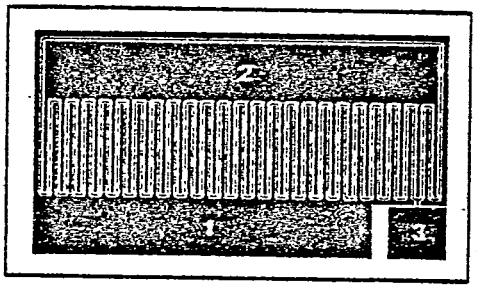
PACKAGE DIMENSIONS

TO-12



All dimensions in inches and (millimeters)

CHIP CONFIGURATION



PAD NO.	FUNCTION
1	SOURCE
2	DRAIN
3	GATE

Dimensions .091 x .055 x .010 inches

2144 F-11

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		CHARACTERISTIC	SD224 MIN	SD224 TYP	SD224 MAX	UNITS	TEST CONDITIONS	
1	STATIC	BV_{DSS} Drain-Source Breakdown Voltage	25	30		V	I_D = 1.0μA, V_{GS} = V_{BS} = 0	
2	STATIC	BV_{SDS} Source-Drain Breakdown Voltage	15			V	I_S = 1.0μA, V_{GD} = V_{BD} = −5V	
3	STATIC	BV_{DB} Drain-Body Breakdown Voltage	20			V	I_D = 1.0μA, V_{GB} = 0 Source Open	
4	STATIC	BV_{SB} Source-Body Breakdown Voltage	20			V	I_S = 1.0μA, V_{GB} = 0 Drain Open	
5	STATIC	I_{GSS} Gate-Body Leakage Current			±1.0	nA	V_{GB} = ±30V, V_{DB} = V_{SB} = 0	
6	STATIC	I_{DSS} Drain-Source OFF Leakage Current		0.1	1.0	μA	V_{DS} = 25V, V_{GS} = V_{BS} = 0	
7	STATIC	$V_{GS(th)}$ Gate-Source Threshold Voltage	0.1	1.0	2.3	V	I_D = 10μA	V_{DS} = V_{GS}, V_{BS} = 0
8	STATIC	$V_{GS(th)}$ Gate-Source Threshold Voltage	0.5	1.5	3.0	V	I_D = 1.0mA	V_{DS} = V_{GS}, V_{BS} = 0
9	STATIC	$I_{D(on)}$ Drain-Source ON Current	1.4	2.0		A	V_{DS} = 2.2V	V_{GS} = 10V, V_{BS} = 0 (Note 4)
10	STATIC	$I_{D(on)}$ Drain-Source ON Current	2.2	3.0		A	V_{DS} = 3.3V	V_{GS} = 10V, V_{BS} = 0 (Note 4)
11	STATIC	$r_{DS(on)}$ Drain-Source ON Resistance		1.4	2.0	ohms	V_{GS} = 5V, V_{BS} = 0	I_D = 50mA (Note 4)
12	STATIC	$r_{DS(on)}$ Drain-Source ON Resistance		1.1	1.5	ohms	V_{GS} = 10V, V_{BS} = 0	I_D = 50mA (Note 4)
13	STATIC	$r_{DS(on)}$ Drain-Source ON Resistance		1.1	1.5	ohms	V_{GS} = 10V, V_{BS} = 0	I_D = 500mA (Note 4)
14	DYNAMIC	g_{fs} Common-Source Forward Transconductance	700	750		mmhos	V_{DS} = 15V, I_D = 2.0A, V_{SB} = 0, f = 1KHz (Note 4)	
15	DYNAMIC	C_{iss} Common-Source Input Capacitance		35	45	pF	V_{DS} = 15V, V_{GS} = V_{BS} = 0, f = 1MHz	
16	DYNAMIC	C_{rss} Common-Source Reverse Transfer Capacitance		5.0	6.0	pF	V_{DS} = 15V, V_{GS} = V_{BS} = 0, f = 1MHz	
17	DYNAMIC	C_{oss} Common-Source Output Capacitance		20	25	pF	V_{DS} = 15V, V_{GS} = V_{BS} = 0, f = 1MHz	
18	DYNAMIC	$t_{d(on)}$ Turn-On Delay Time		1.0	2.0	nSec	V_{DD} = 25V, R_L = 25 ohms, R_G = 51 ohm, V_{IN} = 5V	
19	DYNAMIC	t_r Rise Time		1.0	3.0	nSec	V_{DD} = 25V, R_L = 25 ohms, R_G = 51 ohm, V_{IN} = 5V	
20	DYNAMIC	t_f Fall Time		3.0	5.0	nSec	V_{DD} = 25V, R_L = 25 ohms, R_G = 51 ohm, V_{IN} = 5V	

Note 4: Pulse Test 80μSec, 1% Duty Cycle