

Description

The μPD43251B is a 262,144-word by 1-bit static RAM fabricated with advanced silicon-gate technology. A unique design that uses CMOS peripheral circuits and N-channel memory cells with polysilicon resistors makes the μPD43251B a high-speed device that requires no clock or refreshing.

The μPD43251B is available in 24-pin plastic DIP or 24-pin plastic SOJ packaging.

Features

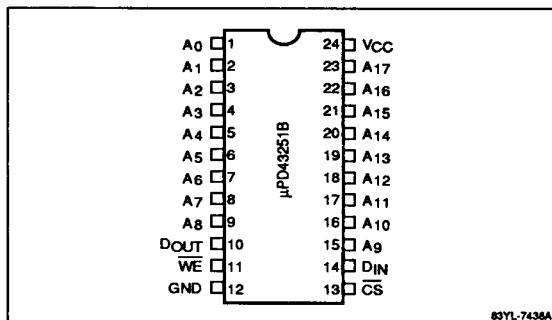
- 262,144-word x 1-bit organization
- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Separated data input and output
- Three-state outputs
- Power dissipation
 - 120 mA max (active)
 - 2 mA max (standby)
- Standard 300-mil, 24-pin plastic DIP or 24-pin plastic SOJ packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD43251BCR-15	15 ns	24-pin plastic DIP
CR-20	20 ns	
CR-25	25 ns	
μPD43251BLA-15	15 ns	24-pin plastic SOJ
LA-20	20 ns	
LA-25	25 ns	

Pin Configuration

24-Pin Plastic DIP or SOJ



Pin Identification

Symbol	Function
A ₀ - A ₁₇	Address inputs
D _{IN}	Data input
D _{OUT}	Data output
CS	Chip select
WE	Write enable
GND	Ground
V _{CC}	+5-volt power supply

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Power supply voltage, V_{CC}	-0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	-0.5 to + V_{CC} + 0.3
Output voltage, V_{OUT}	-0.5 to + V_{CC} + 0.3
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	-55 to +125°C

Notes:

Truth Table

Function	$\overline{\text{CS}}$	$\overline{\text{WE}}$	D_{OUT}	I_{CC}
Not selected	H	X	High-Z	Standby
Read	L	H	Output data	Active
Write	L	L	High-Z	Active

$T_A = +25^{\circ}\text{C}$; $f = 1\text{ MHz}$ (Note 1); V_{IN} and $V_{OUT} = 0\text{ V}$

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			6	pF
Output capacitance	C_O			8	pF

(1) This parameter is sampled and not 100% tested.

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low (Note 1)	V_{IL}	-0.5		0.8	V
Input voltage, high	V_{IH}	2.2		$V_{CC} + 0.3$	V
Ambient temperature	T_A	0		70	°C

(1) $V_{IL} = -3.0\text{ V}$ min for 10 ns maximum pulse.

DC Characteristics

$T_A = 0 \text{ to } +70^\circ\text{C}; V_{CC} = +5.0 \text{ V} \pm 10\%$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	-2		2	μA	$V_{IN} = 0 \text{ V to } V_{CC}$
Output leakage current	I_{LO}	-2		2	μA	$V_{OUT} = 0 \text{ V to } V_{CC}; \overline{CS} = V_{IH}$
Standby supply current	I_{SB}			30	mA	$\overline{CS} = V_{IH}; V_{IN} = V_{IH} \text{ or } V_{IL}$
	I_{SB1}			2	mA	$\overline{CS} \geq V_{CC} - 0.2 \text{ V}; V_{IN} \leq 0.2 \text{ V or } \geq V_{CC} - 0.2 \text{ V}$
Output voltage, low	V_{OL}			0.4	V	$I_{OL} = 8.0 \text{ mA}$
Output voltage, high	V_{OH}	2.4			V	$I_{OH} = -4.0 \text{ mA}$

AC Characteristics

$T_A = 0 \text{ to } +70^\circ\text{C}; V_{CC} = +5.0 \text{ V} \pm 10\%$

Parameter	Symbol	μPD43251B-15		μPD43251B-20		μPD43251B-25		Unit	Test Conditions (Note 1)
		Min	Max	Min	Max	Min	Max		
Read Operation									
Operating supply current	I _{CC}		120		100		100	mA	$\overline{CS} = V_{IL}$ (min cycle); I _{OUT} = 0 mA
Read cycle time	t _{RC}	15		20		25		ns	(Note 2)
Read access time	t _{AA}		15		20		25	ns	
Chip select access time	t _{ACS}		15		20		25	ns	
Output hold from address change	t _{OH}	3		3		3		ns	
Chip select to output in low-Z	t _{CLZ}	3		3		3		ns	(Note 3)
Chip deselect to output in high-Z	t _{CHZ}	0	6	0	8	0	10	ns	(Note 4)
Write Operation									
Write cycle time	t _{WC}	15		20		25		ns	(Note 2)
Chip select to end of write	t _{CW}	13		15		20		ns	
Address valid to end of write	t _{AW}	13		15		20		ns	
Address setup time	t _{AS}	0		0		0		ns	
Write pulse width	t _{WP}	12		14		18		ns	
Write recovery time	t _{WR}	0		0		0		ns	
Data valid to end of write	t _{DW}	10		12		14		ns	
Data hold time	t _{DH}	0		0		0		ns	
Write enable to output in high-Z	t _{WHZ}	0	6	0	8	0	10	ns	(Note 4)
Output active from end of write	t _{OW}	0		0		0		ns	(Note 3)

Notes:

- (1) Input pulse levels = GND to 3.0 V; input pulse rise and fall time = 5 ns; timing reference levels = 1.5 V; see figures 1 and 2 for the output load.
- (2) All read and write cycle timings are referenced from the last valid address to the first transitioning address.
- (3) The transition is measured $\pm 200 \text{ mV}$ from steady-state voltage with the loading shown in figure 2.
- (4) The transition is measured at $V_{OL} + 200 \text{ mV}$ and $V_{OH} - 200 \text{ mV}$ with the loading shown in figure 2.

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Figure 1. Output Load

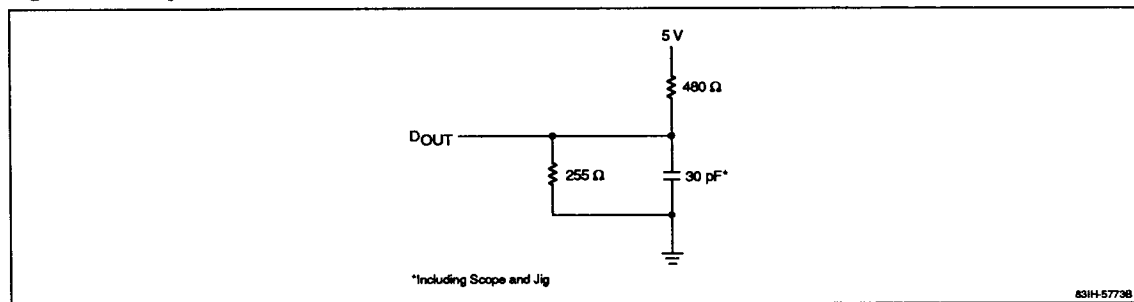
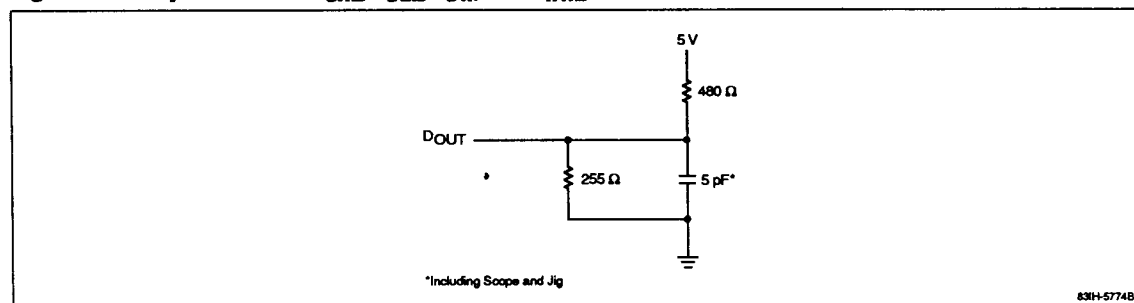
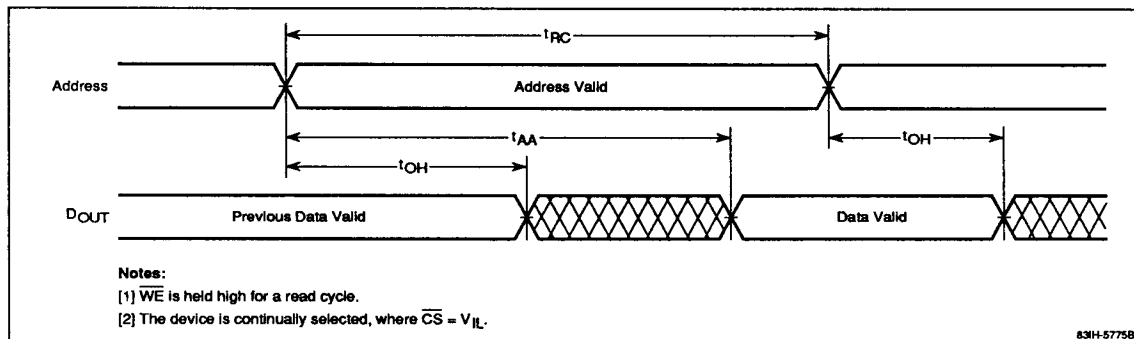


Figure 2. Output Load for t_{CHZ} , t_{CLZ} , t_{OW} , and t_{WHZ}

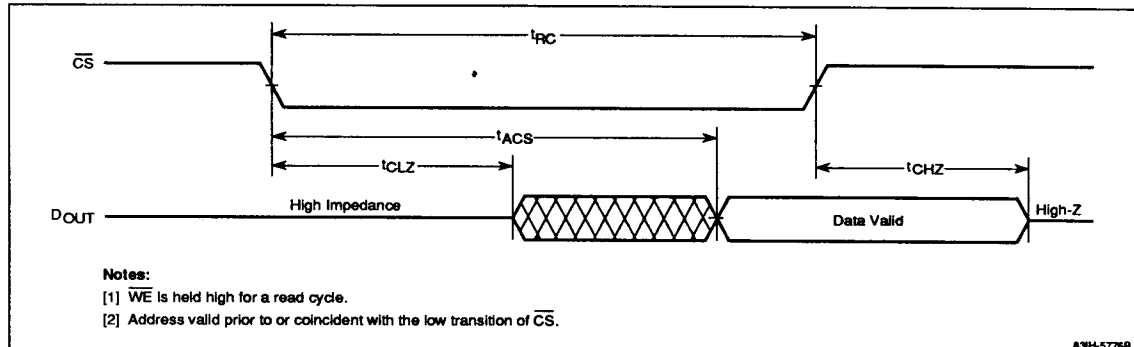


Timing Waveforms

Address Access Cycle



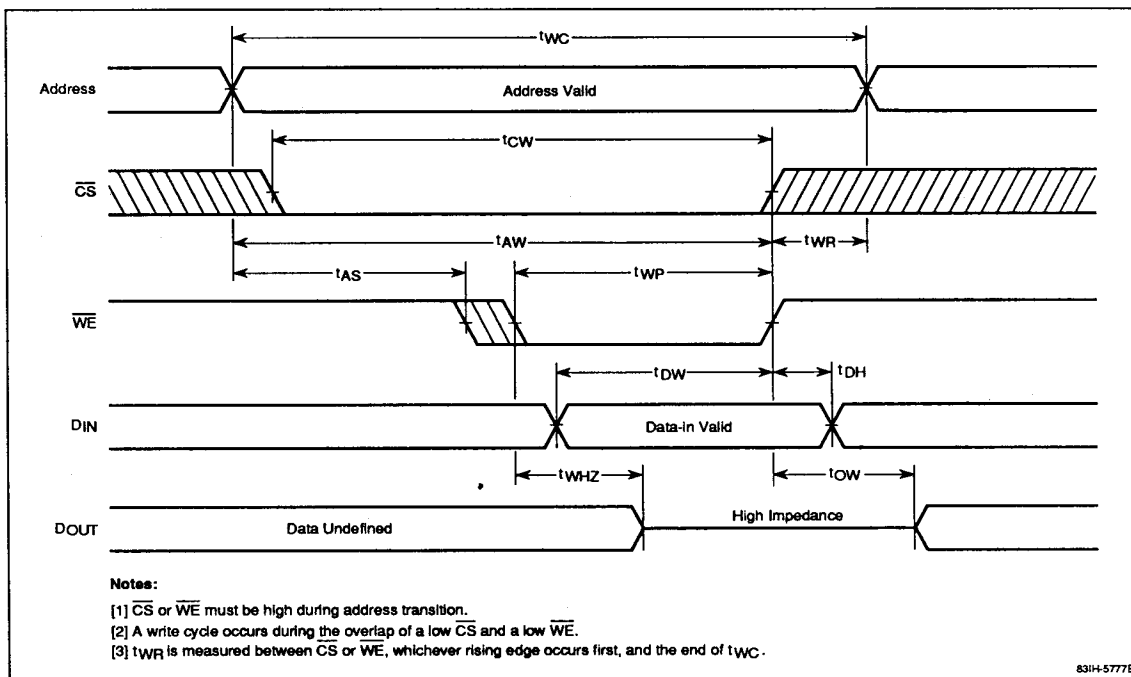
Chip Select Access Cycle



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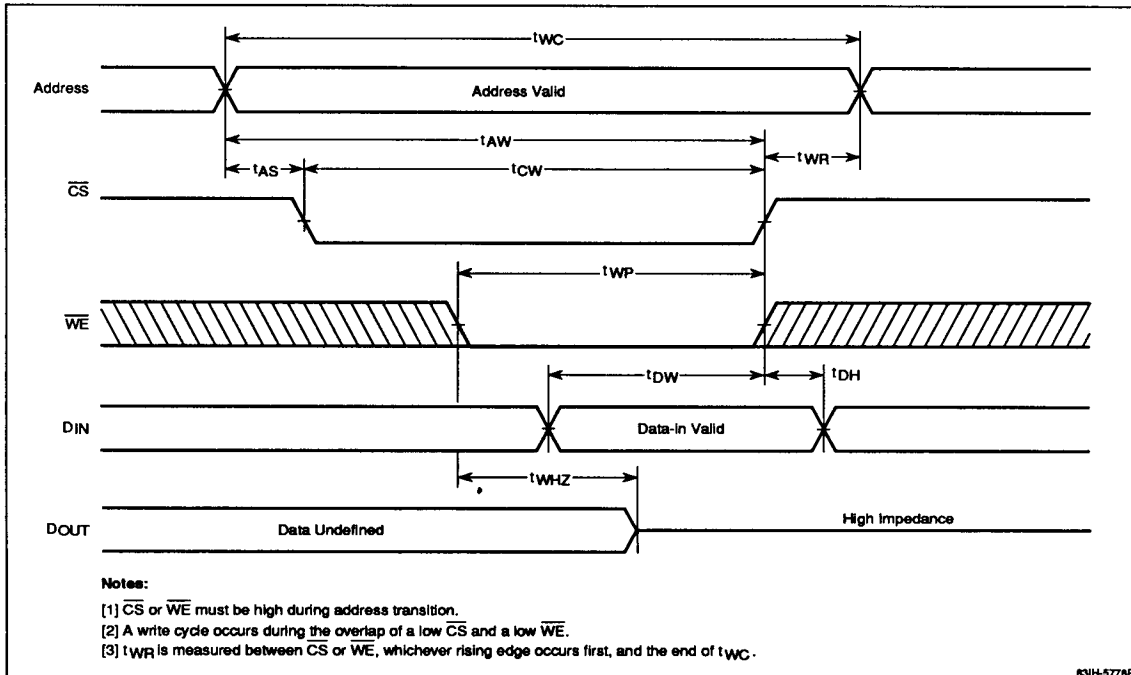
Timing Waveforms (cont)

$\overline{WE}$ -Controlled Write Cycle



Timing Waveforms (cont)

$\overline{CS}$ -Controlled Write Cycle



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