μPD43253B
65,536 x 4-Bit
Static CMOS RAM

Description

The μPD43253B is a 65,536-word by 4-bit static RAM fabricated with advanced silicon-gate technology. CMOS peripheral circuits and N-channel memory cells with polysilicon resistors make the μPD43253B a high-speed device that requires very low power and no clock or refreshing.

The μPD43253B is available in standard 28-pin plastic DIP and SOJ packaging.

Features

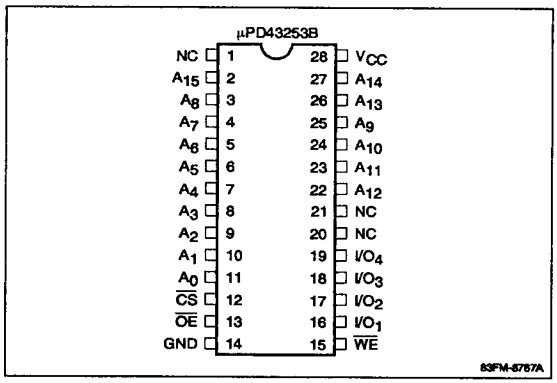
- 65,536-word x 4-bit organization
- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O capability
- Output enable ($\overline{OE}$) control
- Low power dissipation
  - 140 mA max (active)
  - 2 mA max (standby)
- Standard 28-pin, 300-mil plastic DIP and SOJ packages

Ordering Information

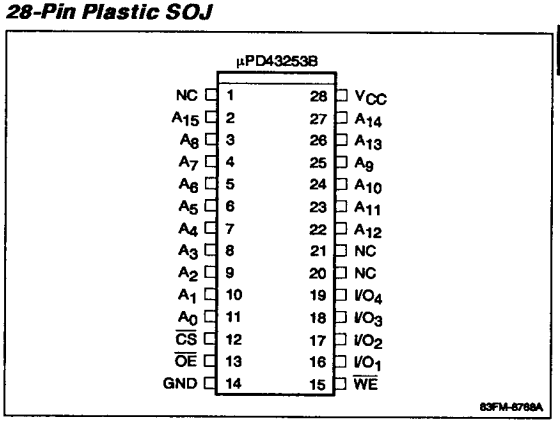
Part Number	Access Time (max)	Package
μPD43253BCR-15	15 ns	28-pin plastic DIP
CR-20	20 ns	
CR-25	25 ns	
μPD43253BLA-15	15 ns	28-pin plastic SOJ
LA-20	20 ns	
LA-25	25 ns	

Pin Configurations

28-Pin Plastic DIP



28-Pin Plastic SOJ



Pin Identification

Symbol	Function
A_0 - A_{15}	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.5 to +7.0 V
Input and output voltages, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) V_{IN} (min) = −3.0 V for 10-ns pulse.

Capacitance

T_A = 25°C; V_{IN} and V_{DOUT} = 0 V; f = 1 MHz

Parameter	Symbol	Min	Max	Unit
Input capacitance	C_{IN}		6	pF
Output capacitance	C_{DOUT}		8	pF

Capacitance is sampled and not 100% tested.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.5		0.8	V
Operating temperature	T_A	0		70	°C

Notes:

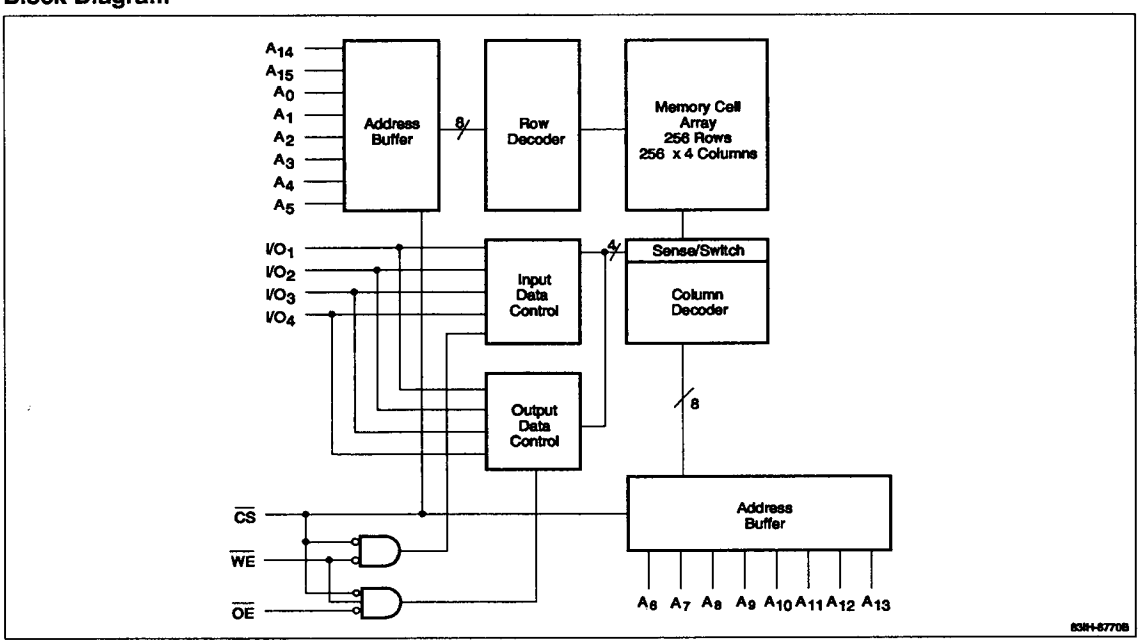
(1) V_{IL} = −3.0 V for 20-ns pulse.

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	Output	I_{CC}
H	X	X	Not selected	High-Z	Standby
L	H	H	Output disable		Active
L	L	X	Write	D_{IN}	Active
L	H	L	Read	D_{OUT}	

X = don't care.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}
Output leakage current	I_{LO}	−2		2	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CS}$ = V_{IH}
Standby supply current	I_{SB}			30	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}			2	mA	$\overline{CS}$ ≥ V_{CC} − 0.2 V; V_{IN} ≤ 0.2 V or ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		μPD43253B-15		μPD43253B-20		μPD43253B-25			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Read Operation									
Operating supply current	I_{CC}		140		120		120	mA	$\overline{CS}$ = V_{IL}; I_{DOUT} = 0 mA
Address access time	t_{AA}		15		20		25	ns	
Chip select access time	t_{ACS}		15		20		25	ns	
Chip deselection to output in high-Z	t_{CHZ}	0	6	0	8	0	10	ns	(Note 4)
Chip selection to output in low-Z	t_{CLZ}	3		3		3		ns	(Note 3)
Output enable access time	t_{OE}		8		10		12	ns	
Output hold from address change	t_{OH}	3		3		3		ns	
Output enable to output in high-Z	t_{OHZ}		6		8		10	ns	
Output enable to output in low-Z	t_{OLZ}	0		0		0		ns	
Read cycle time	t_{RC}	15		20		25		ns	(Note 2)
Write Operation									
Address setup time	t_{AS}	0		0		0		ns	
Address valid to end of write	t_{AW}	13		15		20		ns	
Chip select to end of write	t_{CW}	13		15		20		ns	
Data hold time	t_{DH}	0		0		0		ns	
Data valid to end of write	t_{DW}	10		12		14		ns	
Output active from end of write	t_{OW}	0		0		0		ns	(Note 3)
Write cycle time	t_{WC}	15		20		25		ns	
Write enable to output in high-Z	t_{WHZ}	0	6	0	8	0	10	ns	(Note 4)
Write pulse width	t_{WP}	12		14		18		ns	
Write recovery time	t_{WR}	0		0		0		ns	

Notes:

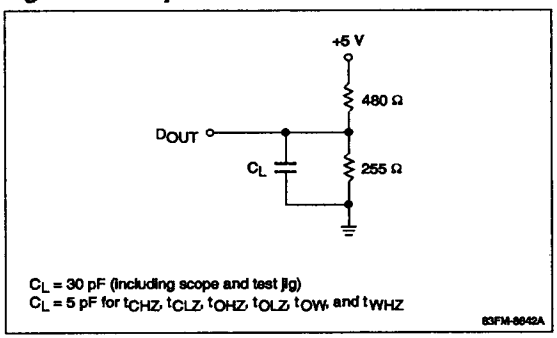
(1) Input pulse levels = GND to 3.0 V; input pulse rise and fall times = 3 ns; timing reference levels = 1.5 V; see figure 1 for output load.

(2) All read cycle timings are referenced from the last valid address to the first transitioning address.

(3) Transition is measured at ±200 mV from steady-state voltage with the load shown in figure 1.

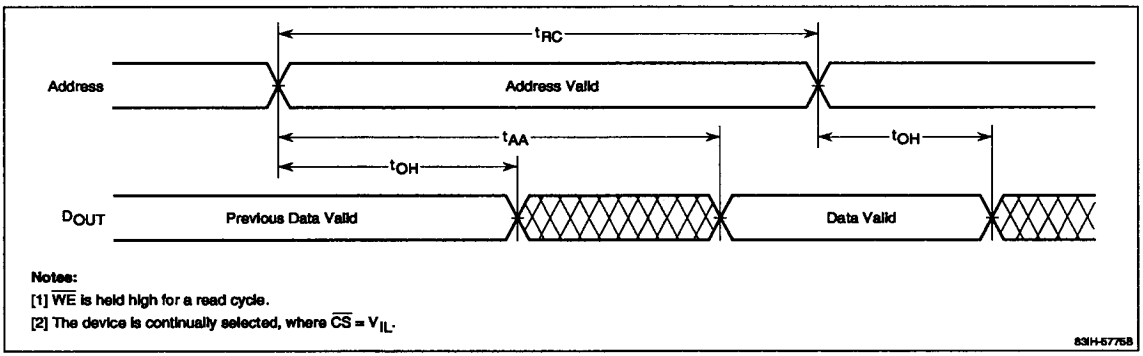
(4) Transition is measured at V_{OL} + 200 mV and V_{OH} − 200 mV with the load shown in figure 1.

Figure 1. Output Loads



Timing Waveforms

Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = V_{IL}$.

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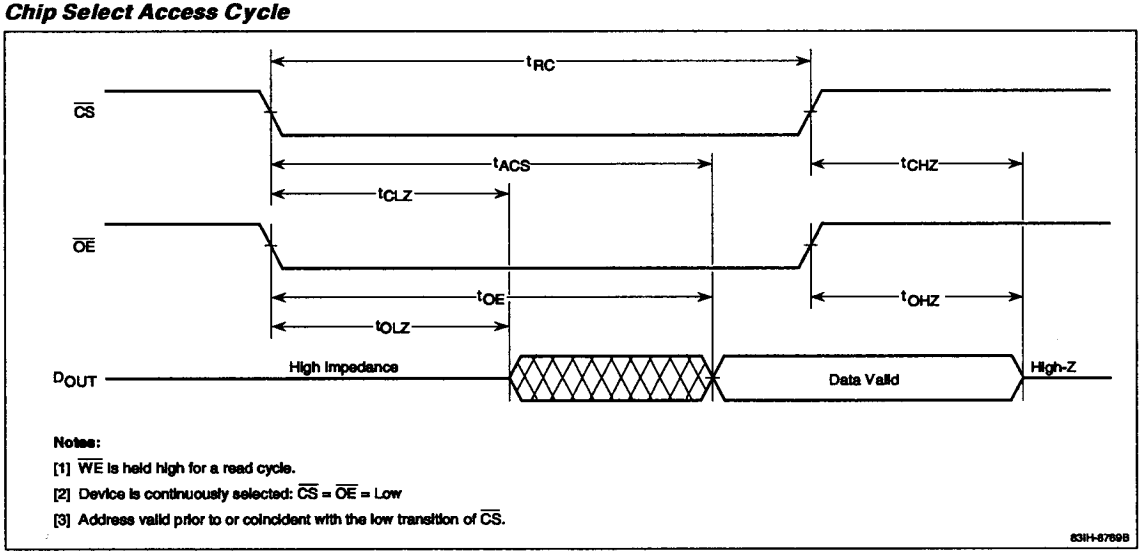
Chip Select Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] Device is continuously selected: $\overline{CS} = \overline{OE}$ = Low
[3] Address valid prior to or coincident with the low transition of $\overline{CS}$.

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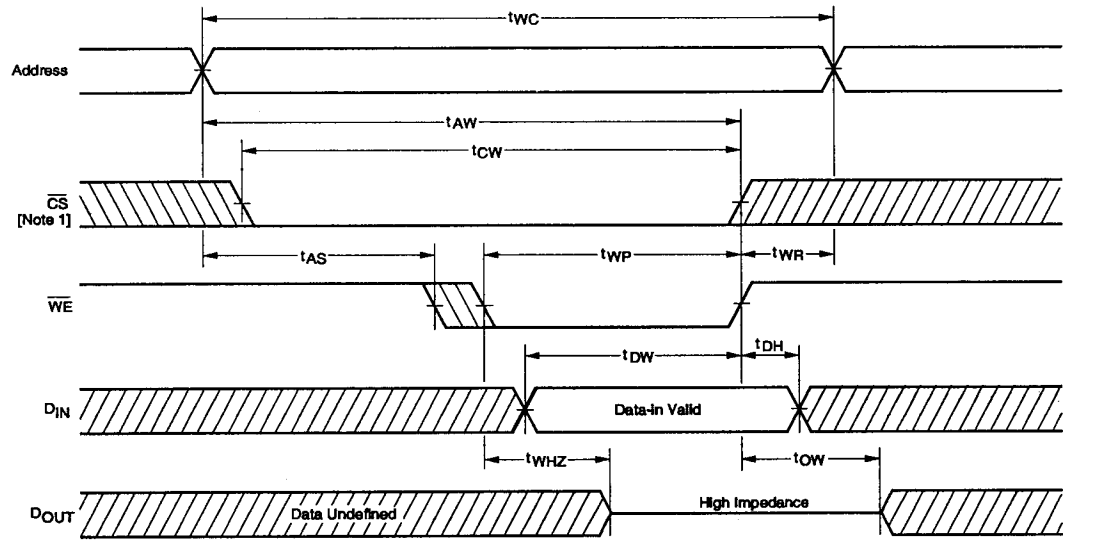
Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.
[2] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
[3] t_{WR} is measured between the rising edge of either $\overline{CS}$ or $\overline{WE}$, whichever occurs first, and the end of t_{WC}.

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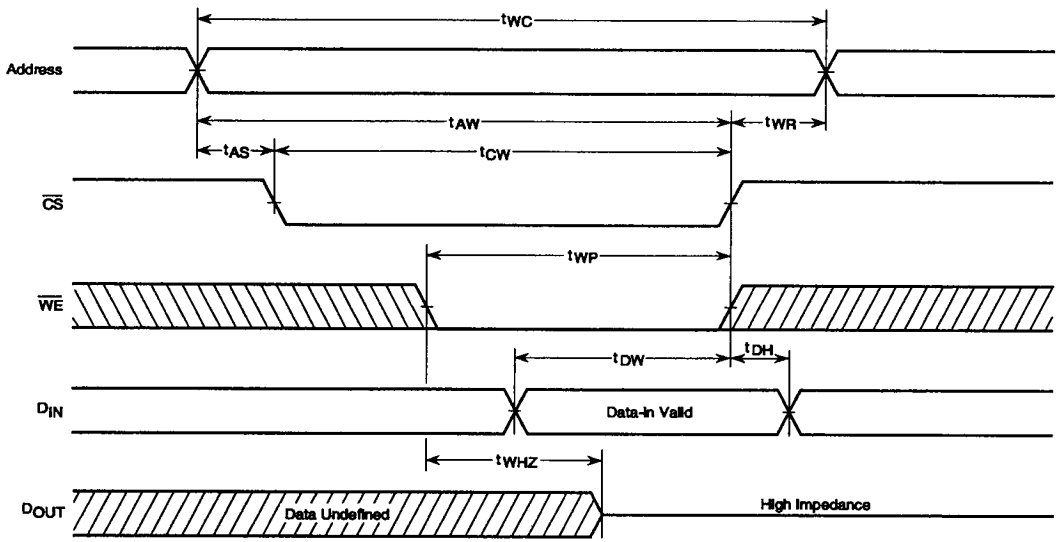
Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.
[2] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
[3] t_{WR} is measured between the rising edge of either $\overline{CS}$ or $\overline{WE}$, whichever occurs first, and the end of t_{WC}.

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