μPD43259A
32,768 x 9-Bit
Static CMOS RAM

Description

The μPD43259A is a 32,768-word by 9-bit static RAM fabricated with advanced silicon-gate technology. Its unique design uses CMOS peripheral circuits and N-channel memory cells with polysilicon resistors to make the μPD43259A a high-speed device that requires very low power and no clock or refreshing.

Minimum standby power is drawn when $\overline{CS}$ is high, independent of the other inputs' levels. The μPD43259A is available in standard 32-pin plastic DIP or SOJ packaging.

Features

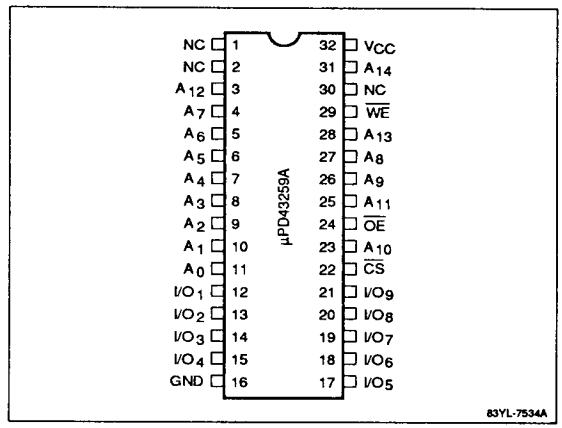
- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O using three-state outputs
- One $\overline{CS}$ pin and one $\overline{OE}$ pin for easy application
- Standard 32-pin plastic DIP and SOJ packaging
- Fast access time of 15 ns (max)

Ordering Information

Part Number	Access Time (max)	Package
μPD43259ACR-15	15 ns	32-pin plastic DIP
CR-20	20 ns	
CR-25	25 ns	
μPD43259ALA-15	15 ns	32-pin plastic SOJ
LA-20	20 ns	
LA-25	25 ns	

Pin Configuration

32-Pin Plastic DIP or SOJ



Pin Identification

Symbol	Function
A_0 - A_{14}	Address inputs
I/O_1 - I/O_9	Data inputs and outputs
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

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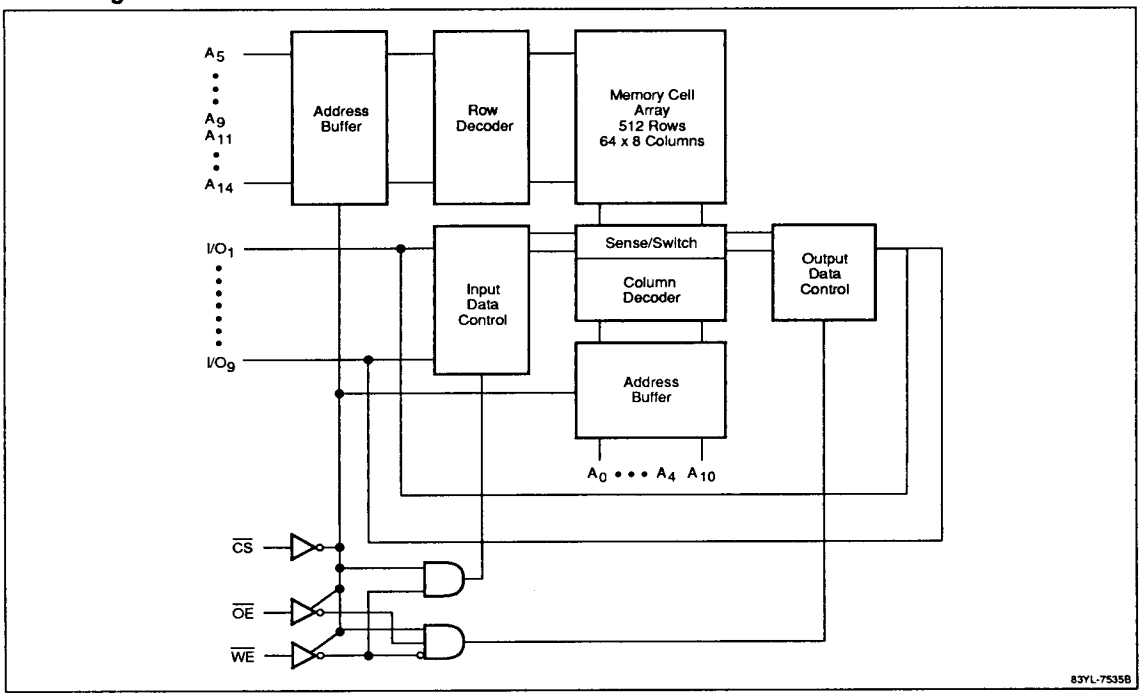
Block Diagram



Truth Table

Function	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	I_{CC}
Not selected	H	X	X	High-Z	Standby
Outputs disabled	L	H	H	High-Z	Active
Read	L	L	H	D_{OUT}	Active
Write	L	X	L	D_{IN}	Active

Notes:

(1) X = don't care.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low (Note 1)	V_{IL}	−0.5		0.8	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Ambient temperature	T_A	0		70	°C

Notes:

(1) −3.0 V minimum (pulse width = 10 ns).

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}
I/O leakage current	I_{LO}	−2		2	μA	$V_{I/O}$ = 0 V to V_{CC}; $\overline{CS} \geq V_{IH}$ or $\overline{OE} \geq V_{IH}$ or $\overline{WE} \leq V_{IL}$
Standby supply current	I_{SB}			30	ma	$\overline{CS} \geq V_{IH}$; $V_{IN} = V_{IH}$ or V_{IL}
	I_{SB1}			2	mA	$\overline{CS} \geq V_{CC} - 0.2$ V; $V_{IN} \leq 0.2$ V or $\geq V_{CC} - 0.2$ V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

Absolute Maximum Ratings

Supply voltage, V_{CC} (Note 1)	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.5 V
Output voltage, $V_{I/O}$ (Note 1)	−0.5 to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) −3.0 V minimum (pulse width = 10 ns).

Capacitance

T_A = +25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Max	Unit
Input capacitance	C_I		6	pF
Input/output capacitance	$C_{I/O}$		8	pF

Notes:

(1) This parameter is sampled and not 100% tested.

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

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Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Read Operation									
Operating supply current	I_{CC}		150		140		130	mA	$\overline{CS} \le V_{IL}$ (min cycle); $I_{I/O}$ = 0 mA
Read cycle time	t_{RC}	15		20		25		ns	(Note 2)
Address access time	t_{AA}		15		20		25	ns	(Note 2)
Chip select access time	t_{ACS}		15		20		25	ns	(Note 2)
Output enable to output valid	t_{OE}		9		10		12	ns	(Note 2)
Output hold from address change	t_{OH}	3		3		3		ns	(Note 2)
Chip select to output in low-Z	t_{CLZ}	3		3		3		ns	(Note 3)
Output enable to output in low-Z	t_{OLZ}	0		0		0		ns	(Note 3)
Chip select to output in high-Z	t_{CHZ}		10		10		10	ns	(Note 3)
Output enable to output in high-Z	t_{OHZ}		8		8		10	ns	(Note 3)
Write Operation									
Write cycle time	t_{WC}	15		20		25		ns	
Chip select to end of write	t_{CW}	12		13		15		ns	
Address valid to end of write	t_{AW}	12		13		15		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	12		13		15		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	9		10		12		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in high-Z	t_{WHZ}		8		8		10	ns	(Note 3)
Output active from end of write	t_{OW}	0		0		0		ns	(Note 3)

Notes:

(1) Input pulse levels = 0 to 3 V; input pulse rise and fall times = 5 ns; timing reference levels = 1.5 V.

(2) See figure 1 for output load.

(3) See figure 2 for output load.

Figure 1. Output Load

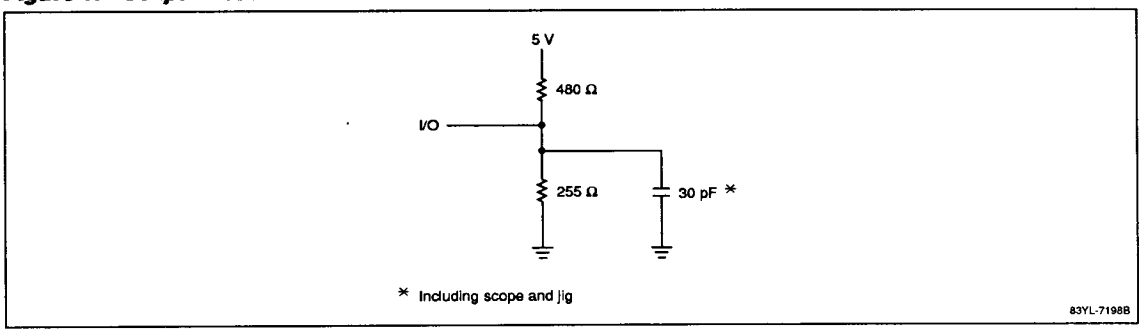
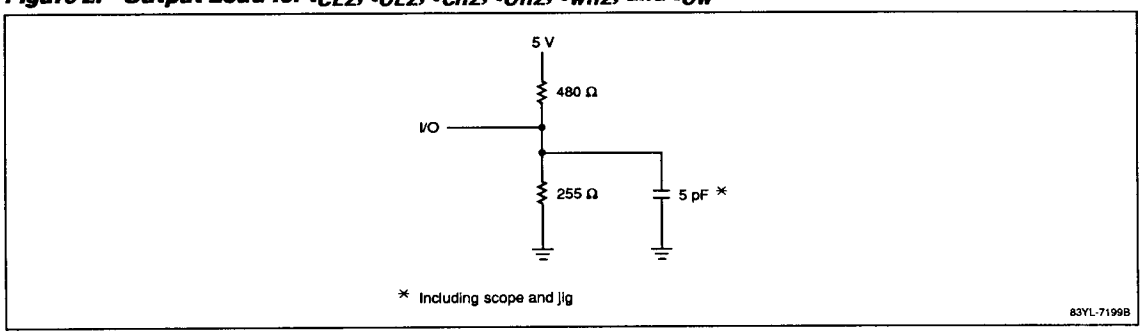
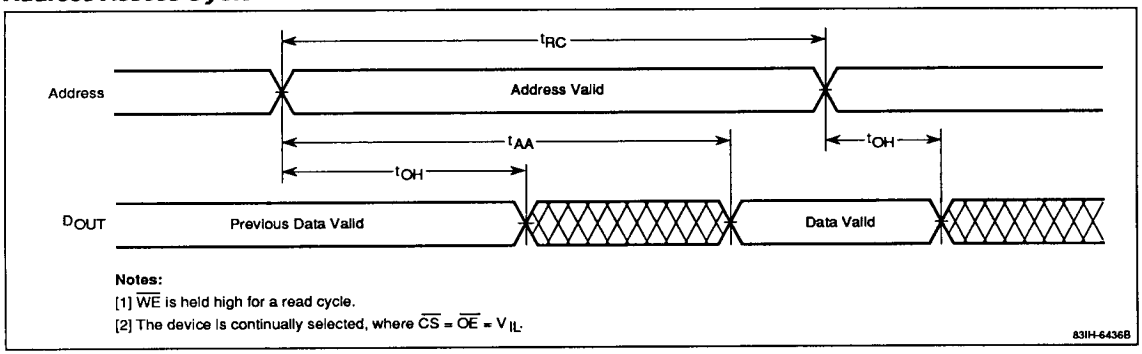


Figure 2. Output Load for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{OW}



Timing Waveforms

Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS}$ = $\overline{OE}$ = V_{IL}.

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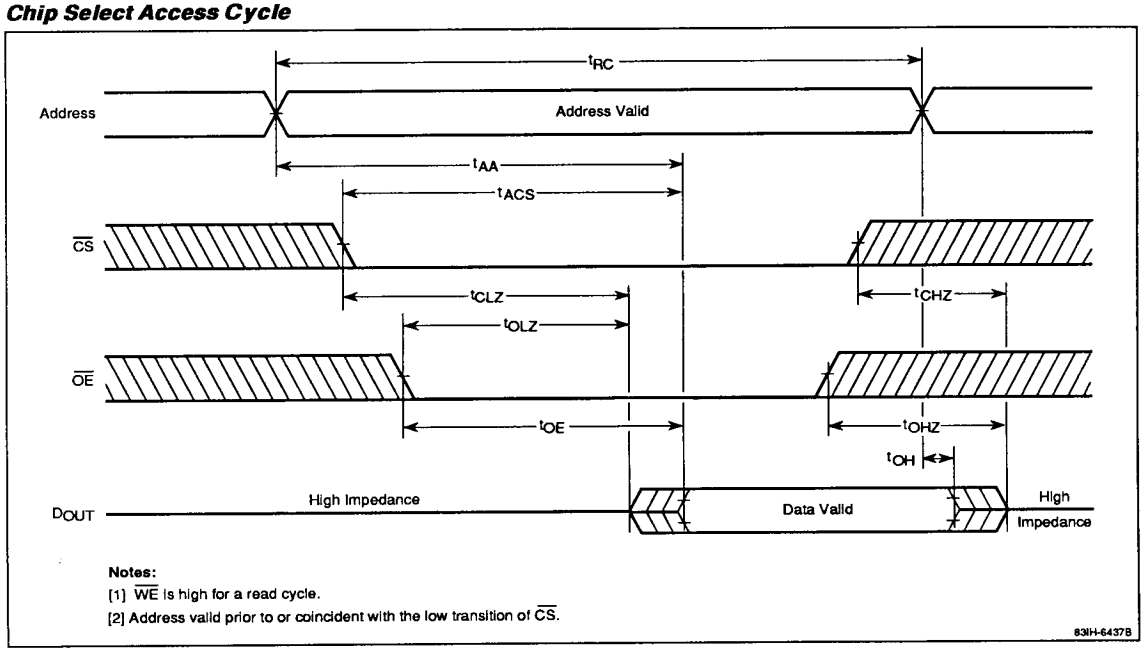
Chip Select Access Cycle



Notes:
[1] $\overline{WE}$ is high for a read cycle.
[2] Address valid prior to or coincident with the low transition of $\overline{CS}$.

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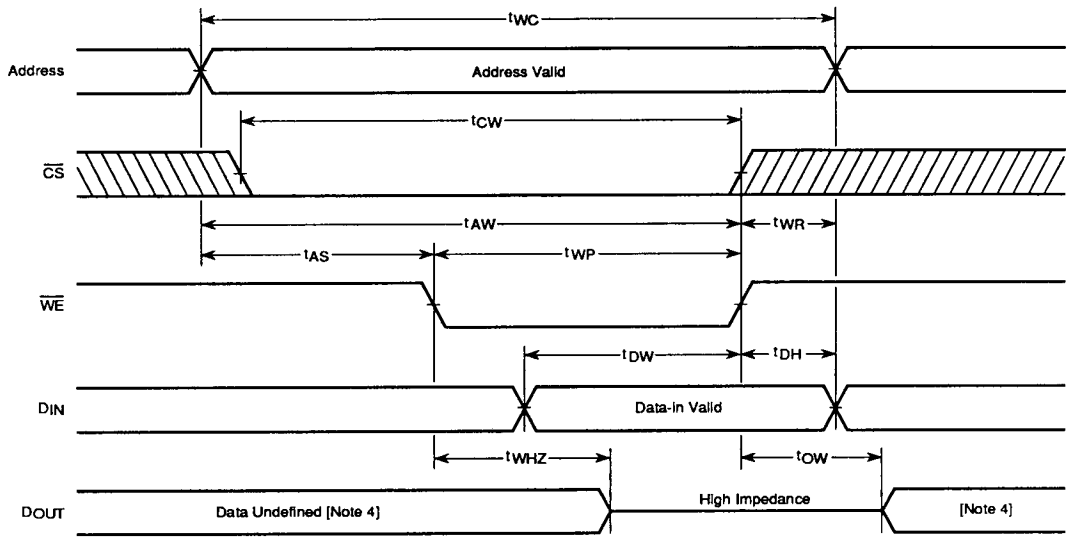
Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[2] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[3] If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.

[4] During this period, the I/O pins may be in the output state. Therefore, input signals of opposite phase must not be applied.

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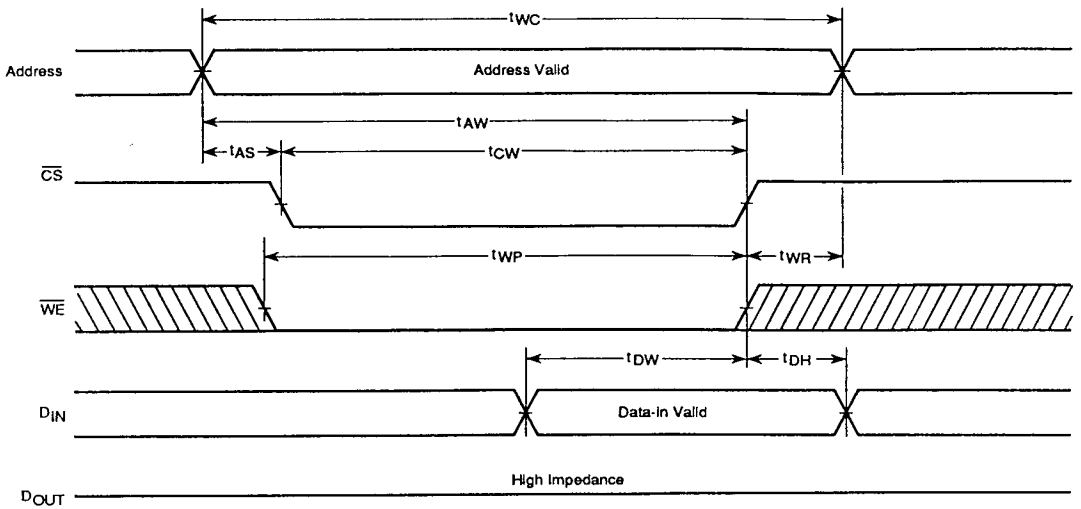
Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[2] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[3] If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.

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