VP5311D/VP5511D

NTSC/PAL Digital Video Encoder

Supersedes March 1998 edition DS4773 2.3

DS4773 -3.5 October 1998

The VP55311D/VP5511D converts digital Y, Cr, Cb, data into analog NTSC/PAL composite video and S-video signals. The outputs are capable of driving doubly terminated 75 ohm loads with standard video levels.

The device accepts data inputs complying with CCIR Recommendation 601 and 656. The data is time multiplexed on an 8 bit bus at 27MHz and is formatted as Cb, Y, Cr, Y (i.e. 4:2:2). The video blanking and sync information from REC 656 is included in the data stream when the VP5311D/ VP5511D is working in slave mode.

The output pixel rate is 27MHz and the input pixel rate is half this frequency, i.e. 13.5MHz.

All necessary synchronisation signals are generated internally when the device is operating in master mode. In slave mode the device will lock to the TRS codes or the HS and VS inputs.

The rise and fall times of sync, burst envelope and video blanking are internally controlled to be within composite video specifications.

Three digital to analog converters (DACs) are used to convert the digital luminance, chrominance and composite data into true analog signals. An internally generated reference voltage provides the biasing for the DACs.

FEATURES

- Converts Y, Cr, Cb data to analog composite video, S-video and YUV to SMTE and Betacam levels
- Supports CCIR recommendations 601 and 656
- All digital video encoding
- Selectable master/slave mode for sync signals
- Switchable chrominance and luma bandwidth
- Switchable pedestal with gain compensation
- SMPTE 170M NTSC or CCIR 624 PAL compatible outputs
- GENLOCK mode
- Line 21 Closed Caption encoding
- I²C bus serial microprocessor interface
- VP5311D supports Macrovision V7.01anti-taping format

APPLICATIONS

- Digital Cable TV
- Digital Satellite TV
- Multi-media
- DVD
- Karaoke
- Digital VCRs

ORDERING INFORMATION

VP5311D/CG/GP1N
VP5511D/CG/GP1N

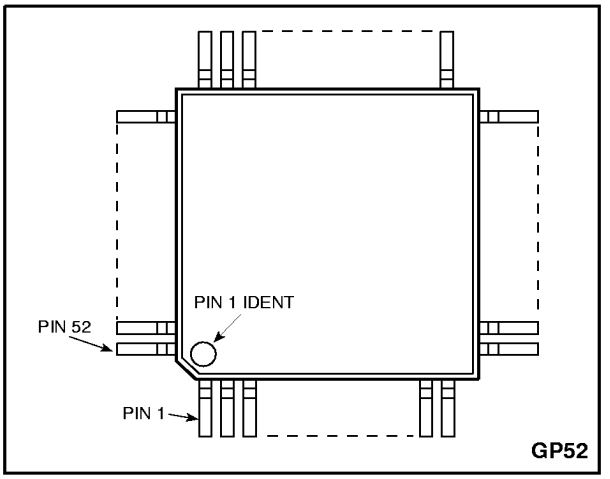

Figure1 Pin connections (top view)

PIN	FUNCTION	PIN	FUNCTION
1	D0 (VS I/O)	27	$\overline{\text{RESET}}$
2	D1 (HS I/O)	28	REFSQ
3	D2 (FC0 O/P)	29	GND
4	D3 (FC1 O/P)	30	PD7
5	D4 (FC2 O/P)	31	PD6
6	D5	32	PD5
7	D6 (SCSYNC I/P)	33	PD4
8	D7 (PALID I/P)	34	PD3
9	GND	35	PD2
10	VDD	36	PD1
11	GND	37	PD0
12	PXCK	38	GND
13	VDD	39	VDD
14	CLAMP	40	AGND
15	COMPSYNC	41	VREF
16	TDO	42	DACGAIN
17	TDI	43	COMP
18	TMS	44	AVDD
19	TCK	45	LUMA
20	GND	46	AGND
21	SA1	47	CVBS/V
22	SA2	48	AGND
23	SCL	49	CHROMA/U
24	VDD	50	AVDD
25	SDA	51	AVDD
26	VDD	52	AVDD

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): As specified in Recommended Operating Conditions

DC CHARACTERISTICS

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Units
Digital Inputs TTL compatible (except SDA, SCL)						
Input high voltage		VIH	2.0			V
Input low voltage		VIL			0.8	V
Digital Inputs SDA, SCL						
Input high voltage		VIH	0.7 VDD			V
Input low voltage		VIL			0.3 VDD	V
Input high current	VIN = VDD	IIH			10	µA
Input low current	VIN = VSS	IIL			-10	µA
Digital Outputs CMOS compatible						
Output high voltage	IOH = -1mA	VOH	3.7			V
Output low voltage	IOL = +4mA	VOL			0.4	V
Digital Output SDA						
Output low voltage	IOL = +6mA	VOL			0.6	V

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): As specified in Recommended Operating Conditions

DC CHARACTERISTICS DACs

Parameter	Symbol	Min.	Typ.	Max.	Units
Accuracy (each DAC)					
Integral linearity error	INL			±1.5	LSB
Diffential linearity error	DNL			±1	LSB
DAC matching error				±5	%
Monotonicity			guaranteed		
LSB size			66.83		µA
Internal reference voltage	V_{REF}		1.050		V
Internal reference voltage output impedance	Z_R		27k		Ω
Reference Current (V_{REF}/R_{REF}) R_{REF} = 769Ω	I_{REF}		1.3699		mA
DAC Gain Factor ($V_{OUT} = K_{DAC} \times IREF \times R_L$), V_{OUT} = DAC code 511	K_{DAC}		24.93		
Peak Glitch Energy (see figure3)			50		pV-s
CVBS, Y and C - NTSC (pedestal enabled)					
Maximum output, relative to sync bottom			33.75		mA
White level relative to black level			17.64		mA
Black level relative to blank level			1.40		mA
Blank level relative to sync level			7.62		mA
Colour burst peak - peak			7.62		mA
DC offset (bottom sync)			0.40		mA
CVBS, Y and C - PAL					
Maximum output			34.15		mA
White level relative to black level			18.71		mA
White level relative to sync level			26.73		mA
Black level relative to sync level			8.02		mA
Colour burst peak - peak			8.02		mA
DC offset (bottom sync)			0.00		mA

Note: All figures are for: R_{REF} = 769Ω R_L = 37.5Ω. When the device is set up in NTSC mode there is a +0.25% error in the PAL levels. If R_L = 75Ω then R_{REF} = 1538Ω.

ABSOLUTE MAXIMUM RATINGS

Supply voltage	VDD, AVDD	-0·3 to 7·0V
Voltage on any non power pin		-0·3 to VDD+0·3V
Ambient operating temperature		0 to 70°C
Storage temperature		-55°C to 150°C

Note: Stresses exceeding these listed under Absolute Maximum Ratings may induce failure. Exposure to Absolute Maximum Ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Units
Power supply voltage	VDD, AVDD	4.75	5.00	5.25	V
Power supply current (including analog outputs)	IDD		150		mA
Input clock frequency	PXCK	-50ppm	27.00	+50ppm	MHz
SCL clock frequency	f_{SCL}			500	kHz
Analog video output load			37.5		Ω
DAC gain resistor			769		Ω
Ambient operating temperature		0		70	°C

VIDEO CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Units
Luminance bandwidth (high)			6.16		MHz
Luminance bandwidth (medium)			4.34		MHz
Luminance bandwidth (low)			2.79		MHz
Chrominance bandwidth (Extended B/W mode)			1.3		MHz
Chrominance bandwidth (Reduced B/W mode)			650		kHz
Burst frequency (NTSC)			3.57954545		MHz
Burst frequency (PAL-B, D,G,H,I)			4.43361875		MHz
Burst frequency (PAL-N Argentina)			3.58205625		MHz
Burst cycles (NTSC and PAL-N)			9		Fsc cycles
Burst cycles (PAL-B, D, G, H,I)			10		Fsc cycles
Burst envelope rise / fall time (all standards)			300		ns
Analog video sync rise / fall time (NTSC and PAL-N)			145		ns
Analog video sync rise / fall time (PAL-B, D, G, H,I)			245		ns
Differential gain			1.0		% pk-pk
Differential phase			0.5		° pk-pk
Signal to noise ratio (unmodulated ramp)				-61	dB
Chroma AM signal to noise ratio (100% red field)				-56	dB
Chroma PM signal to noise ratio (100% red field)				-58	dB
Hue accuracy				2.5	%
Colour saturation accuracy				2.5	%
Residual sub carrier			-60		dB
Luminance / chrominance delay		-5	0	+5	ns

ESD COMPLIANCE

Pins	Test	Test Levels	Notes
All pins	Human body model	2kV on 100pF through 1k5Ω	Meets Mil-Std-883 Class 2
All pins	Machine model	200V on 200pF through 0Ω & 500nH	

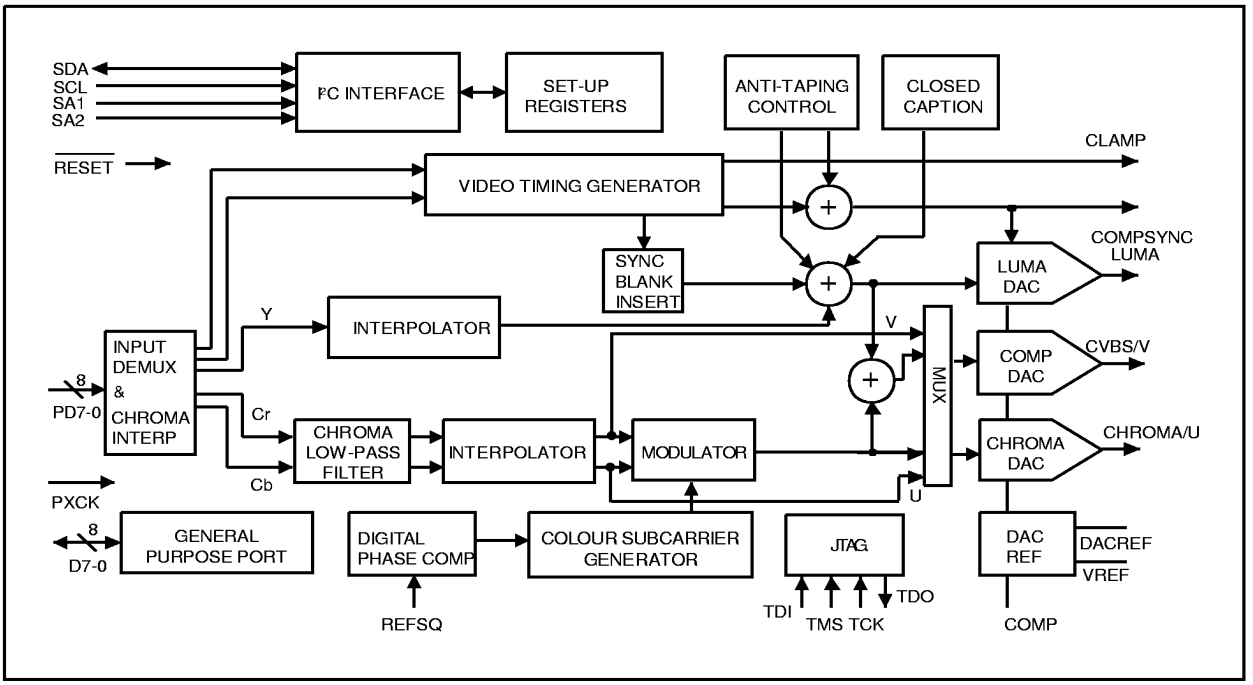

Figure 2 Functional block diagram of the VP5311D, the VP5511D is identical except there is no Anti-Taping Control

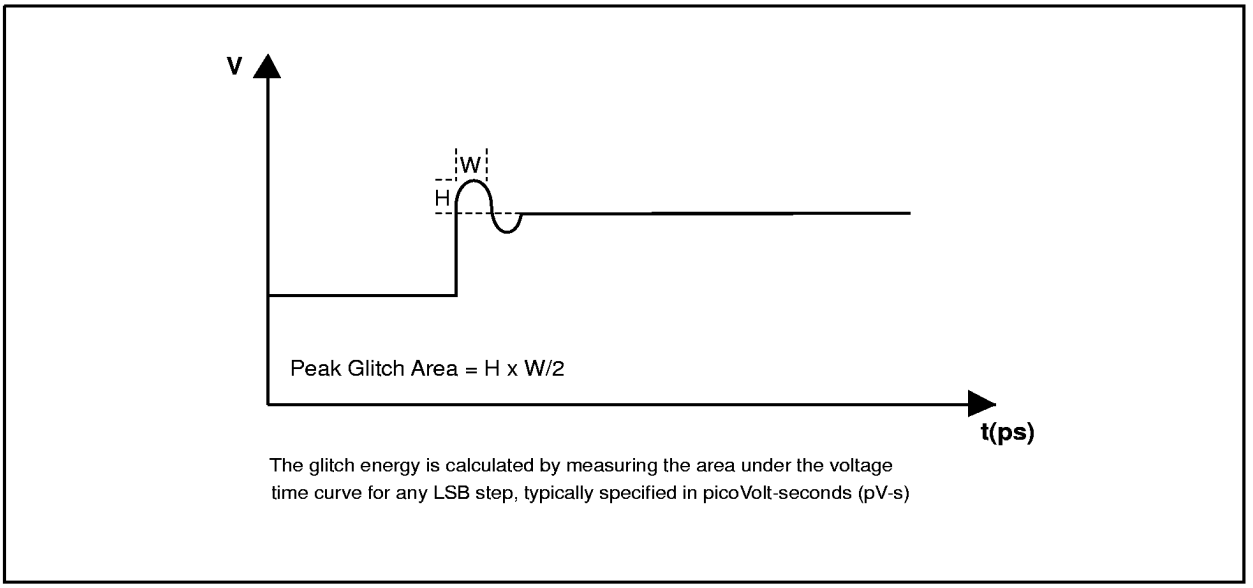

Figure 3 Glitch Energy

PIN DESCRIPTIONS

Pin Name	Pin No.	Description
PD7-0	30 - 37	8 Bit Pixel Data inputs clocked by PXCK. PD0 is the least significant bit, corresponding to Pin 37. These pins are internally pulled low.
D0-7	1 - 8	8 Bit General Purpose Port input/output. D0 is the least significant bit, corresponding to Pin 1. These pins are internally pulled low.
PXCK	12	27MHz Pixel Clock input. The VP5311D/5511D internally divides PXCK by two to provide the pixel clock.
CLAMP	14	The CLAMP output signal is synchronised to COMPSYNC output and indicates the position of the BURST pulse, (lines 10-263 and 273-525 for NTSC; lines 6-310 and 319-623 for PAL-B,D, G,I,N(Argentina)).
COMPSYNC	15	Composite sync pulse output. This is an active low output signal.
TDO	16	JTAG Data output port.
TDI	17	JTAG Data input port.
TMS	18	JTAG mode select input.
TCK	19	JTAG clock input.
SA1	21	I²C slave address select
SA2	22	I²C slave address select.
SCL	23	Standard I²C bus serial clock input.
SDA	25	Standard I²C bus serial data input/output.
$\overline{\text{RESET}}$	27	Master reset. This is an asynchronous, active low, input signal and must be asserted for a minimum 200ns in order to reset the VP5311D/5511D.
REFSQ	28	Reference square wave input used only during Genlock mode.
VREF	41	Voltage reference input/output. This pin is nominally 1.055V and should be decoupled with a 100nF capacitor to GND.
DACGAIN	42	DAC full scale current control. A resistor connected between this pin and GND sets the magnitude of the video output current. An internal loop amplifier controls a reference current flowing through this resistor so that the voltage across it is equal to the Vref voltage.
COMP	43	DAC compensation. A 100nF ceramic capacitor must be connected between pin 43 and pin 44.
LUMA	45	True luminance, composite and chrominance video signal outputs. These are high impedance current source outputs. A DC path to GND must exist from each of these pins.
CVBS/V	47	
CHROMA/U	49	
VDD	10, 13, 24, 26, 39	Positive supply input. All VDD pins must be connected.
AVDD	44, 50, 51, 52	Analog positive supply input. All AVDD pins must be connected.
GND	9, 11, 20, 29, 38	Negative supply input. All GND pins must be connected.
AGND	40, 46, 48	Negative supply input. All AGND pins must be connected.

REGISTERS MAP

See Register Details for further explanations.

ADDRESS hex	REGISTER NAME	7	6	5	4	3	2	1	0	R/W	DEFAULT hex
	BAR	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	W	
00	PART ID2	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	R	13
01	PART ID1	ID0F	ID0E	ID0D	ID0C	ID0B	ID0A	ID09	ID08	R	66
02	PART ID0	ID07	ID06	ID05	ID04	ID03	ID02	ID01	ID00	R	58
03	REV ID	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	R	07
04	GCR	-	CLP656DIS	YCDELAY	RAMPEN	SLH&V	CVBSCLP	VFS1	VFS0	R/W	00
05	VOCR	LUMA714	CLAMPDIS	CHRBW	SYNCDIS	BURDIS	LUMDIS	CHRDIS	PEDEN	R/W	00
06	HANC	LBW1	LBW0	DF2	DF1	DF0	Reserved	Reserved	ACTREN	*	00
07	ANCID	AN7	AN6	AN5	AN4	AN3	AN2	AN1	PARITY	R/W	00
08	SC_ADJ	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	R/W	9C
09	FREQ2	FR17	FR16	FR15	FR14	FR13	FR12	FR11	FR10	R/W	87
0A	FREQ1	FR0F	FR0E	FR0D	FR0C	FR0B	FR0A	FR09	FR08	R/W	C1
0B	FREQ0	FR07	FR06	FR05	FR04	FR03	FR02	FR01	FR00	R/W	F1
0C	SCHPHM	-	-	-	-	-	-	-	SCH8	R/W	00
0D	SCHPHL	SCH7	SCH6	SCH5	SCH4	SCH3	SCH2	SCH1	SCH0	R/W	00
0E to 1F	Reserved										
20	GPPCTL	CTL7	CTL6	CTL5	CTL4	CTL3	CTL2	CTL1	CTL0	W	FF
21	GPPRD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	R	-
22	GPPWR	WR7	WR6	WR5	WR4	WR3	WR2	WR1	WR0	W	00
23-33	Reserved										
34 to EF	Not used										
F0	CCREG1	-	F1W1D6	F1W1D5	F1W1D4	F1W1D3	F1W1D2	F1W1D1	F1W1D0	R/W	--
F1	CCREG2	-	F1W2D6	F1W2D5	F1W2D4	F1W2D3	F1W2D2	F1W2D1	F1W2D0	R/W	--
F2	CCREG3	-	F2W1D6	F2W1D5	F2W1D4	F2W1D3	F2W1D2	F2W1D1	F2W1D0	R/W	--
F3	CCREG4	-	F2W2D6	F2W2D5	F2W2D4	F2W2D3	F2W2D2	F2W2D1	F2W2D0	R/W	--
F4	CC_CTL	-	-	-	-	F2ST	F1ST	F2EN	F1EN	R/W	0C
F5 to F7	Reserved										
F8	HSOFFL	HSOFF7	HSOFF6	HSOFF5	HSOFF4	HSOFF3	HSOFF2	HSOFF1	HS0FF0	R/W	7E
F9	HSOFFM	-	-	-	-	-	-	HSOFF9	HSOFF8	R/W	00
FA	Reserved										
FB	SLAVE1	NCORSTD	VBITDIS	VSMODE	F_SWAP	SL_HS1	SL_HS0	HCNT9	HCNT8	R/W	00
FC	SLAVE2	HCNT7	HCNT6	HCNT5	HCNT4	HCNT3	HCNT2	HCNT1	HCNT0	R/W	00
FD	DACCFG	YUVMODE	BETACAM	YDACD	CDACD	CVDACD	YCLKHI	CCLKHI	CVCLKHI	R/W	00
FE	TEST2			REGISTER	RESERVED	FOR	TEST			R/W	
FF	GPSCTL	FSC4SEL	GENDITH	GENLKEN	NOLOCK	PALIDEN	TSURST	CHRMCLIP	TRSEL	R/W	00

Table.1 Register map

NOTE * For register HANC, bits 3, 4 and 5 are read only. Bits 1 and 2 are reserved. N/A = not applicable.
For register PART ID0 the VP5511D value is AB

Standard	Lines/ field	Field freq. Hz	Number of pixels/line at 27MHz	Horizontal freq. kHz. f_H	Subcarrier freq. kHz. f_{SC}	f_{SC}/f_H	SC_ADJ register hex	FREQ2-0 registers hex
NTSC (default)	525	59.94	1716	15.734266	3.57954545	(455/2)	xx	87 C1 F1
PAL-B, G, H, I	625	50	1728	15.625000	4.43361875	(1135/4+1/625)	9C	A8 26 2B
PAL-N (Argentina)	625	50	1728	15.625000	3.58205625	(917/4+1/625)	57	87 DA 51

Table.2 Line, field and subcarrier standards and register settings

xx = don't care.

The calculation of the FREQ register value is according to the following formula:-

$$FREQ = 2^{26} \times f_{SC}/PXCK \text{ hex, where PXCK} = 27.00\text{MHz}$$

The NTSC value is rounded UP from the decimal number. PAL-B, D, G, H, I and N (Argentina) are rounded DOWN. The SC_ADJ value is derived from the adjustment needed to be added after 8 fields to ensure accuracy of the Subcarrier frequency. Note the SC_ADJ value of 9C required for PAL-B, D, G, H, I, is different to the default state of the register.
In NTSC the NCO is reset at the end of every line, this can be disabled by setting the NCORSTD bit in SLAVE1, this allows the VP5311D to cope with line lengths that are not exactly as specified in REC656.

REGISTER DETAILS

BAR **Base register**
RA7-0 Register address.

PART ID 2-0 **Part number**
ID17-00 Chip part identification (ID) number.

REV ID **Revision number**
REV7-0 Chip revision ID number.

GCR **Global Control**
CLP656DIS 1 = Disable input clamp to Rec656 levels

YCDELAY Luma to Chroma delay, high = 37ns, low = normal operation

RAMPEN Modulated ramp enable when set high, low = normal operation

SLH&V 1 = Slave to HS and VS inputs

CVBSCLMP 1 = Enables clamp on composite output, to prevent flatenning of chroma peaks and troughs.

VFS1-0 Video format select

VFS1	VFS0	
0	0	NTSC (default)
0	1	PAL-B,D,G,H,I,N(Argentina)
1	0	Reserved
1	1	Reserved

VOCR **Video Output Control**
LUMA714 Forces 700mV luma peak in YUV mode only

CLAMPDIS Clamp signal disable

CHRBW Chroma bandwidth select.
0 = ± 650kHz 1 = ± 1.3MHz

SYNCDIS Sync disable (in comosite video signal) COMPSYNC is not affected.

BURDIS Chroma burst disable

LUMDIS Luma input disable - force black level

COLDIS Colour output disable
- force monochrome

PEDEN High = Pedestal (set-up) enable a 7·5 IRE pedestal on lines 23-262 and 286-525. Valid for NTSC only

HANC **Horizontal Ancillary Data Control**

LBW1-0 Luma filter control

LBW1	LBW0	-3dB Bandwidth
0	0	6.16MHz
0	1	4.34MHz
1	X	2.79MHz

DF2-0(read only) Digital Field Identification, 000=Field1

ANCTREN Ancillary timing reference enable. When High use FIELD COUNT from ancillary data stream. When low, data is ignored.

ANCID **Ancillary data ID**
AN7-1 Ancillary data ID
Parity Parity bit (odd)

SC_ADJ **Sub Carrier Adjust**
SC7-0 Sub carrier frequency seed value,

FREQ2-0 **Sub carrier frequency**
FR17-00 24 bit Sub carrier frequency programmed via I²C bus, FREQ3 is the MSB.

SCHPHM-L **Sub carrier phase offset**
SCH8-0 9 bit Sub carrier phase relative to the 50% point of the leading edge of the horizontal part of composite sync. SCHPHM bit 0 is the MSB.

GPPCTL **General purpose port control**
CTL7-0 Each bit controls port direction
0 = output 1 = input

GPPRD **General purpose port read data**
RD7-0 I²C bus read from general purpose port (only INPUTS defined in GPPCTL)

GPPWR **General purpose port write data**
WR7-0 I²C bus write to general purpose port (only OUTPUTS defined in GPPCTL)

F2ST Field two (line 284) status
High = data has been encoded
Low = new data has been loaded to CCREG3-4

GPPRD **General purpose port read data**
RD7-0 I²C bus read from general purpose port (only INPUTS defined in GPPCTL)

GPPWT **General purpose port write data**
WR7-0 I²C bus write to general purpose port (only OUTPUTS defined in GPPCTL)

CCREG1 **Closed Caption register 1**
F1W1D6-0 Field one (line 21), first data byte

CCREG2 **Closed Caption register 2**
F1W2D6-0 Field one (line 21), second data byte

CCREG3 **Closed Caption register 3**

F2W2D6-0	Field two (line 284), first data byte
CCCTL	**Closed Caption control register**
F1ST	Field one (line 21) status High = data has been encoded Low = new data has been loaded to CCREG1-2
F2ST	Field two (line 284) status High = data has been encoded Low = new data has been loaded to CCREG3-4
F1EN	Closed Caption field one (line 21) High = enable Low = disable (default)
F2EN	Closed Caption field two (line 284) High = enable Low = disable (default)
HSOFFM-L	**HS offset**
HSOFF9-0	This is a 10 bit number which allows the user to offset the start of digital data input with reference to the pulse HS.
SLAVE1	**H &V Slave mode control register**
NCORSTD	1 = NCO Line Reset Disable (NTSC only)
VBITDIS	0 = Video blanked when Rec601 V bit set 1 = V bit is ignored
VSMODE	0 = Standard Vsync I/P 1 = Even/Odd Field I/P
F_SWAP	The odd and even fields are swapped
SL_HS1-0	Selects pixel sample (0 to 4)
HCNT9-8	As HCNT7-0 but MSBs
SLAVE2	**H &V Slave position register**
HCNT7-0	Adjusts for delay at which pixel data occurs relative to HS
DACCFG	DAC Configuration register
YUV	1 = YUV Output Mode 0 = SVHS (Default) Mode
BETACAM	1 = Betacam scaling for YUV output 0 = SMPTE scaling for YUV output
YDACD	1 = Luma DAC Disabled
CDACD	1 = Chroma DAC Disabled
CDACD	1 = Composite Video DAC Disabled
YCLKHI	1 = LUMA DAC Clock held High
CCLKHI	CHROMA DAC Clock held High
CVCLKHI	CVBS DAC Clock held High

GPSCTL	**GPS Control**
FSC4SEL	When high, REFSQ = 4xFSC and GPP bit D6 becomes an input for a SCSYNC signal (1 = reset), which provides a synchronous phase reset for FSC divider. When low, normal operation with REFSQ = 1*FSC.
GENDITH	1 = Genlock dither added.
GENLKEN	High = enable Genlock to REFSQ input. Low = internal subcarrier generation
PALIDEN	High = enable external PAL ID phase control and GPP bit D7 becomes an input for PALID signal, (0 = +135°, 1 = -135°). When low, normal operation, internal PAL switch is used.
TSURST	High = chip soft reset. Low = normal operation
CHRMCLIP	High = enable clipping of chroma data when luma is clipped. Low = no chroma clipping
TRSEL	High = master mode, GPP bits D0 - 4 become a video timing port with VS, HS and FIELD outputs. Low = slave mode, timing from REC656.

I²C BUS CONTROL INTERFACE

I²C bus address

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
0	0	0	1	1	SA2	SA1	X

The serial microprocessor interface is via the bi-directional port consisting of a data (SDA) and a clock (SCL) line. It is compatible to the Philips I²C bus standard (Jan. 1992 publication number 9398 393 40011). The interface is a slave transmitter - receiver with a sub-address capability. All communication is controlled by the microprocessor. The SCL line is input only. The most significant bit (MSB) is sent first. Data must be stable during SCL high periods.

A bus free state is indicated by both SDA and SCL lines being high. START of transmission is indicated by SDA being pulled low while SCL is high. The end of transmission, referred to as a STOP, is indicated by SDA going from low to high while SCL is high. The STOP state can be omitted if a repeated START is sent after the acknowledge bit. The reading device acknowledges each byte by pulling the SDA line low on the ninth clock pulse, after which the SDA line is released to allow the transmitting device access to the bus.

The device address can be partially programmed by the setting of the pins SA1 and SA2. This allows the device to respond to one of four addresses, providing for system flexibility. The I²C bus address is seven bits long with the last bit indicating read / $\overline{\text{write}}$ for subsequent bytes.

The first data byte sent after the device address, is the sub-address - BAR (base address register). The next byte will be written to the register addressed by BAR and subsequent bytes to the succeeding registers. The BAR maintains its data after a STOP signal.

NTSC/PAL Video Standards

Both NTSC (4-field, 525 lines) and PAL (8-field, 625 lines) video standards are supported by the VP5311D/VP5511D. All raster synchronisation, colour sub-carrier and burst characteristics are adapted to the standard selected. The VP5311D/VP5511D generates outputs which follow the requirements of SMPTE 170M and CCIR 624 for PAL signals.

The device supports the following:
NTSC,
PAL B, D, G, H, I, and N (Argentina).

Video Blanking

The VP5311D/VP5511D automatically performs standard composite video blanking. Lines 1-9, 264-272 inclusive, as well as the last half of line 263 are blanked in NTSC mode. In PAL mode, lines 1-5, 311-318, 624-625 inclusive, as well as the last half of line 623 are blanked.

The V bit within REC656 defines the video blanking when TRSEL (bit 0 of GPSCTL register) is set low. When in MASTER mode with TRSEL set high the video encoder is still enabled. Therefore if these lines are required to be blank they must have no video signal input.

Rec. 656 Clamp

By default the Rec. 656 chrominance data is clamped if it exceeds levels that cannot be processed by the internal circuitry. The clamp only operates when data goes outside the Rec. 656 legal limits. This clamp can be disabled with the CLP656DIS bit in register GCR.

Interpolator

The luminance and chrominance data are separately passed through interpolating filters to produce output sampling rates double that of the incoming pixel rate. This reduces the sinx/x distortion that is inherent in the digital to analog converters and also simplifies the analog reconstruction filter requirements.

Digital to Analog Converters

The VP5311D/VP5511D contains three 9 bit digital to analog converters which produce the analog video signals. The DACs use a current steering architecture in which bit currents are routed to one of two outputs; thus the DAC has true and complementary outputs. The complementary output is connected to GND internally. The use of identical current sources and current steering their outputs means that monotonicity is guaranteed. An on-chip voltage reference of 1.050V provides the necessary biasing. However, the VP5311D/VP5511D may be used in applications where an external 1V reference is provided on the VREF pin, to adjust the video levels. In this case, the external reference should be temperature compensated and provide a low impedance output.

The full-scale output currents of the DACs is set by an external 769Ω resistor between the DACGAIN and a GND pins. An on-chip loop amplifier stabilises the full-scale output current against temperature and power supply variations.

The analog outputs of the VP5311D/VP5511D are capable of directly driving singly terminated 75Ω loads. For this application the DACGAIN resistor is simply doubled.

SVHS Mode Video Outputs

The Luminance video output (LUMA pin 45) drives a 37.5Ω load at 1.0V, sync tip to peak white. It contains only the luminance content of the image plus the composite sync pulses. In the NTSC mode, a set-up level offset can be added during the active video portion of the raster.

The Chrominance video output (CHROMA/U pin 49) drives a 37.5Ω load at levels proportional in amplitude to the luma output (40 IRE pk-pk burst). This output has a fixed offset current which will produce approximately a 0.5V DC bias across the 37.5Ω load. Burst is injected with the appropriate timing relative to the luma signal.

The composite video output (CVBS/V pin 47) will also drive a 37.5Ω load in CVBS Mode at 1.0V, sync tip to peak white. It contains both the luminance and chrominance content of the signal plus the composite sync pulses.

The CVBS DAC output clipping feature limits the digital data going into the DAC so that if it goes outside the range it is limited to the maximum or minimum (511 or 000). This feature is permanently enabled.

When CVBSCLP in register GCR is set to a '1' an envelope prediction circuit is enabled that establishes if the chroma and luma added together is likely to go outside the CVBS DAC limits. If it is, then a smooth rounding of the chroma peaks is made to stop this happening. This prevents any high frequency components being produced as with the default clipping function which will produce flat peaks. In practice there will be some loss of saturation in the colour.

YUV Mode

The load driving capability is exactly the same as in SVHS mode, likewise the filtering is also the same. In this mode the Luma output remains virtually the same as in SVHS mode, the amplitudes will be as shown in Tables 7 - 9. The U and V outputs are shown in Figures 9, and 10, When there is no signal on the U and V outputs the DC level will be at DAC code 256 (mid point). There is no colour burst on the U/V outputs.

Output sinx/x compensation filters are required on all video outputs, as shown in the typical application diagram, see Figures 11 & 12.

Video Timing - Slave sync mode

The VP5311D/VP5511D has an internal timing generator which produces video timing signals appropriate to the mode of operation. In the default (following reset) slave mode, all timing signals are derived from the input clock, PXCK, which must be derived from a crystal controlled oscillator. Input pixel data is latched on the rising edge of the PXCK clock.

The video timing generator produces the internal blanking and burst gate pulses, together with the composite sync output signal, using timing data (TRS codes) from the Ancillary data in the REC656 input signal.

H & V Slave Mode
HCNT

To ensure that the incoming data is sampled correctly a 10 bit binary number (HCNT) has to be programmed into the SLAVE1 and 2 registers. This will allow the device's internal horizontal counter to align with the video data, each bit represents one 13.5MHz cycle. To calculate this use the formula below:

NTSC
HCNT = SN + 119 (When SN = 0 - 738)
HCNT = SN - 739 (When SN = 739 - 857)

PAL
HCNT = SN + 127 (SN = 0 - 736)
HCNT = SN - 737 (SN = 737 - 863)

where SN is Rec. 656/601 sample number on which the negative edge of HSYNC occurs.

SL_HS

A further adjustment is also required to ensure that the falling edge of HSYNC occurs on a Y sample that precedes a Cr sample. The bits SL_HS1-0 introduce a delay of 0-3 27MHz samples in the CbYCrY sequence, failure to set this correctly will mean corruption of the colour or colour being interpreted as luma.

F_SWAP

If the field synchronisation is wrong it can be swapped by setting this bit.

V_SYNC

When set to a '1' this bit allows an odd/even square wave to provide the field synchronisation.

Example

For more information see H & V Slave Sync Mode Application Brief.

Video Timing - Master sync mode

When TRSEL (bit 0 of GPSCTL register) is set high, the VP5311D/5511D operates in a MASTER sync mode, all REC656 timing reference codes are ignored and GPP bits D0 - 4 become a video timing port with VS, HS and FIELD outputs. The PXCK signal is, however, still used to generate all internal clocks. When TRSEL is set high, the direction setting of bits 4 - 0 of the GPPCTL register is ignored.

VS is the start of the field sync datum in the middle of the equalisation pulses. HS is the line sync which is used by the preceding MPEG2 decoder to define when to output digital video data to the VP5311D/5511D. In NTSC 262.5/262.5 Syncs are output and 312.5/312.5 in PAL.

HS offset

The position of the falling edge of HS relative to the first data Cb0, can be programmed in HSOFFM-L registers, see Figure 4, this is called the pipeline delay and may need adjusting for a particular application. This is done by programming a 10 bit number called HSOFF into the HSOFFM and HSOFFL registers, HSOFFM being the most significant two bits and HSOFFL the least significant eight bits.

The value to program into HSOFF can be looked up in tables 3 &4: where NCK = number of 13.5MHz clock cycles between the falling edge of HS and Cb0 (first data I/P on PD7-0) see Figure. 4.

N_{CK}	HSOFF	Comments
0 to 120	126 to 6	HS normal (64 cks)
121 to 183	863 to 801	HS pulse shortened*
184 to 857	800 to 127	HS normal (64 cks)

Table 3 for NTSC

*HS pulse shortened means that the width of the pulse will be less than the normal 64 13.5MHz clock cycles.

N_{CK}	HSOFF	Comments
0 to 120	126 to 6	HS normal (64 cks)
121 to 183	863 to 801	HS pulse shortened*
184 to 857	800 to 127	HS normal (64 cks)

Table 4 for PAL-B, D,G, H,I, N

*HS pulse shortened means that the width of the pulse will be less than the normal 64 13.5MHz clock cycles.

Decreasing HSOFF advances the HS pulse (numbers are in decimal).

The interruption in the sequence of values is because the HS signal is jumping across a line boundary to the previous line as the offset is increased. The register default value is 7EH and this sets Nck to 0, ie. the HS negative edge and Cb0 are co-incident in NTSC mode.

Genlock using REFSQ input

The VP5311D/5511D can be Genlocked to another video source by setting GENLKEN high (in GPSCTL register) and feeding a phase coherent sub carrier frequency signal into REFSQ. Under normal circumstances, REFSQ will be the same frequency as the sub carrier. By setting FSC4SEL to SCSYNC (pin 7), the frequency of SCSYNC can be at the sub carrier frequency, once per line or once per field, depending on the application. When GENLKEN is set high, the direction setting of bit 6 in the GPPCTL register is ignored.

PALID Input

When in Genlock mode with GENLKEN set high (in GPSCTL register), the VP5311/5511D requires a PAL phase identification signal, to define the correct phase on every line. This is supplied to PALID input (pin 8), High = -135° and low = +135°. The signal is asynchronous and should be changed before the sub carrier burst signal. PALID input is enabled by setting PALIDEN high (in GPSCTL register). When GENLKEN is high, the direction setting of bit 7 of the GPPCTL register is ignored

Master Reset

The VP5311D/VP5511D must be initialised with the RESET pin 27. This is an asynchronous active low signal and must be active for a minimum of 200ns in order for the VP5311D/VP5511D to be reset. The device resets to the start of horizontal sync on line 254 in NTSC and line 301 in PAL (i.e. line blanking active). There is no on-chip power on reset circuitry.

Line 21 coding

Two bytes of data are coded on the line 21 of each field, see Figure 7. In the NTSC Closed Caption service, the default state is to code on line 21 of field one only. An additional service can also be provided using line 21 (284) of the second field. The data is coded as NRZ with odd parity, after a clock run-in and framing code. The clock run-in frequency = 0.5034965MHz which is related to the nominal line period, D = H / 32.

$$D = 63.55555556 / 32\mu s$$

Two data bytes per field are loaded via I²C bus registers CCREG1-4. Each field can be independently enabled by programming the enable bits in the control register (CC_CTL). The data is cleared to zero in the Closed Caption shift registers after it has been encoded by the VP5311D/ VP5511D. Two status bits are provided (in CC_CTL), which are cleared when data is written to the registers and set high when the data has been encoded on the Luma signal. The data is cleared to zero in the Closed Caption shift registers after it has been encoded by the VP5311D/VP5511D. The next data bytes must be written to the registers when the status bit goes high, otherwise the Closed Caption data output will contain Null characters. Null characters are invisible to a Closed Caption receiver. The MSB (bit 7) is the parity bit and is automatically added by the encoder.

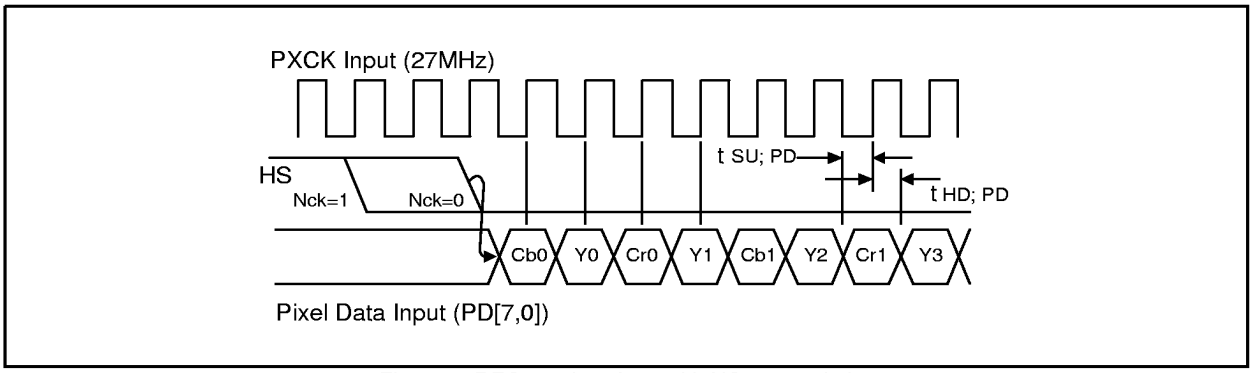

Figure 4 REC 656 interface with HS output timing

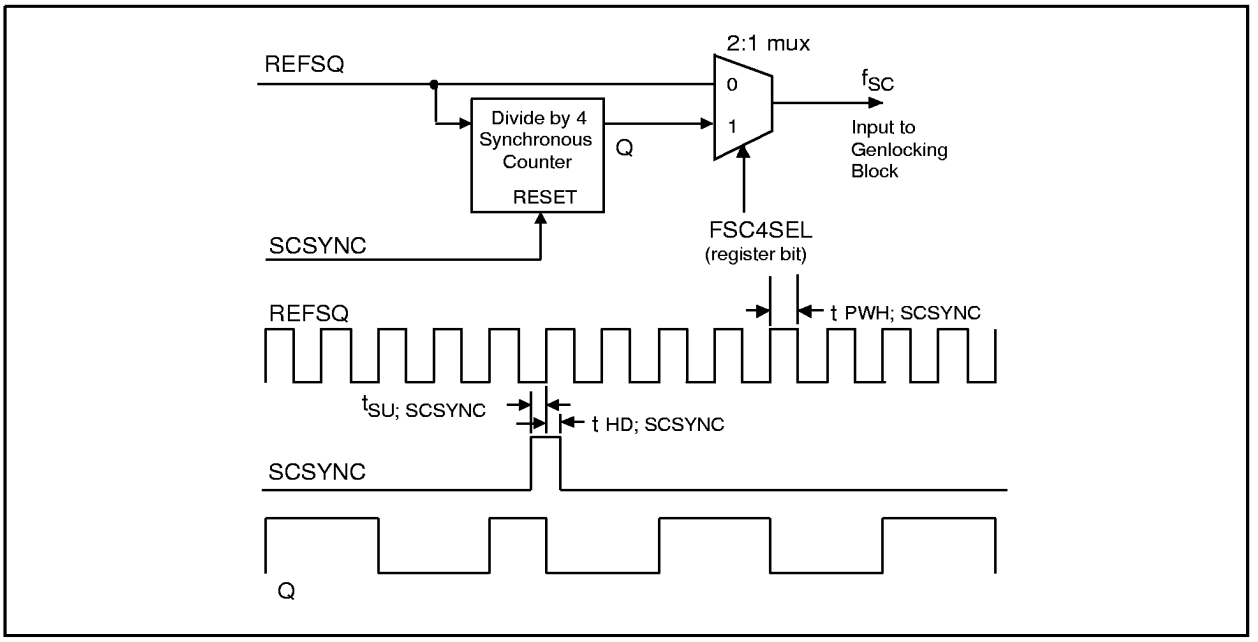

Figure 5 REFSQ and SC SYNC input timing

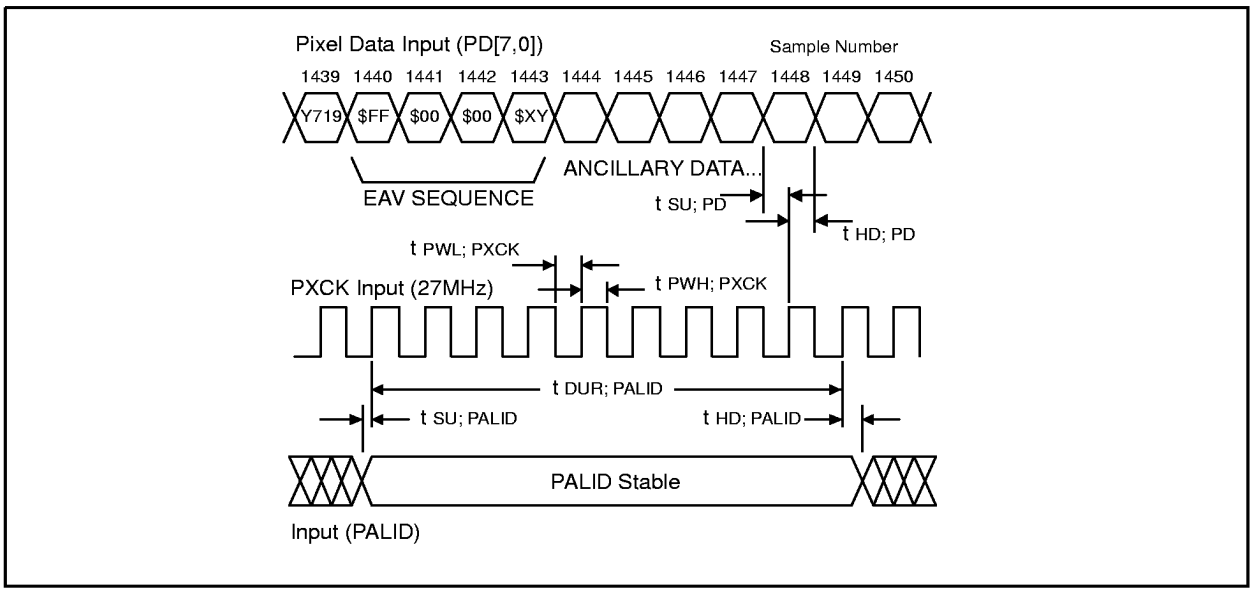

Figure 6 PALID input timing

TIMING INFORMATION

Parameters	Conditions	Symbol	Min.	Typ.	Max.	Units
Master clock frequency (PXCK input)		f_{PXCK}		27.0		MHz
PXCX pulse width, HIGH		$t_{PWH;\ PXCK}$	10			ns
PXCX pulse width, LOW		$t_{PWL;\ PXCK}$	14.5			ns
PXCX rise time	10% to 90% points	t_{RP}			TBD	ns
PXCX fall time	90% to 10% points	t_{FP}			TBD	ns
PD7-0 set up time		$t_{SU;PD}$	10			ns
PD7-0 hold time		$t_{HD;PD}$	5			ns
SCSYNC set up time		$t_{SU;SCSYNC}$	10			ns
SCSYNC hold time		$t_{HD;SCSYNC}$	0			ns
PALID set up time		$t_{SU;PALID}$	10			ns
PALID hold time		$t_{HD;PALID}$	0			ns
PALID duration		$t_{DUR;PALID}$	9			PXCX periods
Output delay	PXCK to COMPSYNC PXCK to CLAMP	t_{DOS}			25	ns

Note: Timing reference points are at the 50% level. Digital C_{LOAD} <40pF.

Table 5 Timing Information

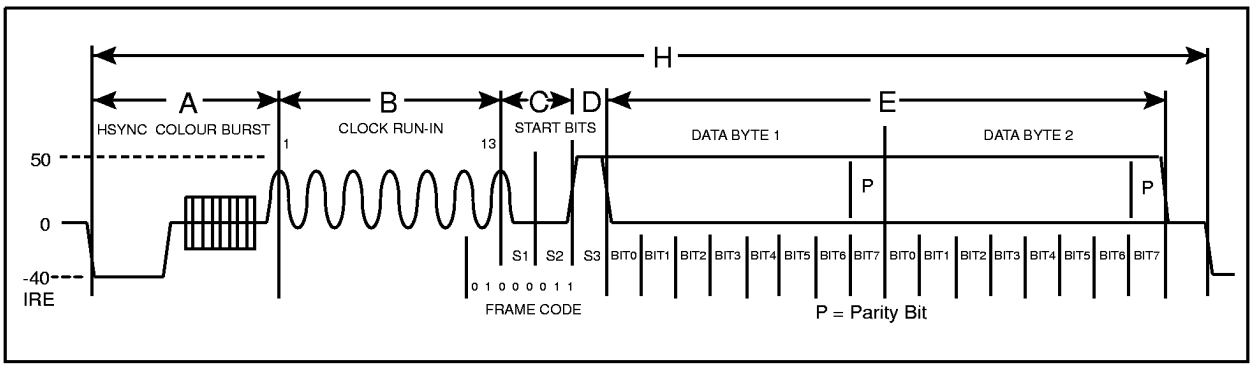

Figure 7 Closed Caption format

Interval	Description	Encoder minimum	Encoder nominal	Encoder maximum
A	H-sync to clock run-in	10.250µs	10.500µs	10.750µs
B	Clock run-in [2, 3]		6.5D (12.910µs)	
C	Clock run-in to third start bit [3]		2.0D (3.972µs)	
D	Data bit [1, 3]		1.0D (1.986µs)	
E	Data characters [4]		16.0D (31.778µs)	
H	Horizontal line [1]		32.0D (63.556µs)	
	Rise / fall time of data bit transitions [5]		0.240µs	0.288µs
	Data bit high (logic level one) [6] Clock run-in maximum	48 IRE	50 IRE	52 IRE
	Data bit low (logic level zero) [6] Clock run-in minimum	0 IRE	0 IRE	2 IRE
	Data bit differential (high - low) Clock run-in differential (max. - min)	48 IRE	50 IRE	52 IRE

Table. 6 Closed Caption data timing. (source EIA R - 4.3 Sept 16 1992)

Notes
1. The Horizontal line frequency f_H is nominally 15734.26Hz ±0.05Hz. Interval D shall be adjusted to D = 1/(f_H x 32) for the instantaneous f_H at line 21.
2. The clock run-in signal consists of 7.0 cycles of a 0.5034965MHz (1/D) sine wave when measured from the leading to trailing 0 IRE points. The sine wave is to be symmetrical about the 25 IRE level.
3. The negative going midpoints (half amplitude) of the clock run-in shall be coherent with the midpoints (half amplitude) of the Start and Data bit transitions.
4. Two characters, each consisting of 7 data bits and 1 odd parity bit.
5. 2 T Bar, measured between the 10% and 90% amplitude points.
6. The clock run-in maximum level shall not differ from the data bit high level by more than ±1 IRE. The clock run-in minimum level shall not differ from the data bit low level by more than ±1 IRE.

YUV Mode 100% Colour Bar Outputs

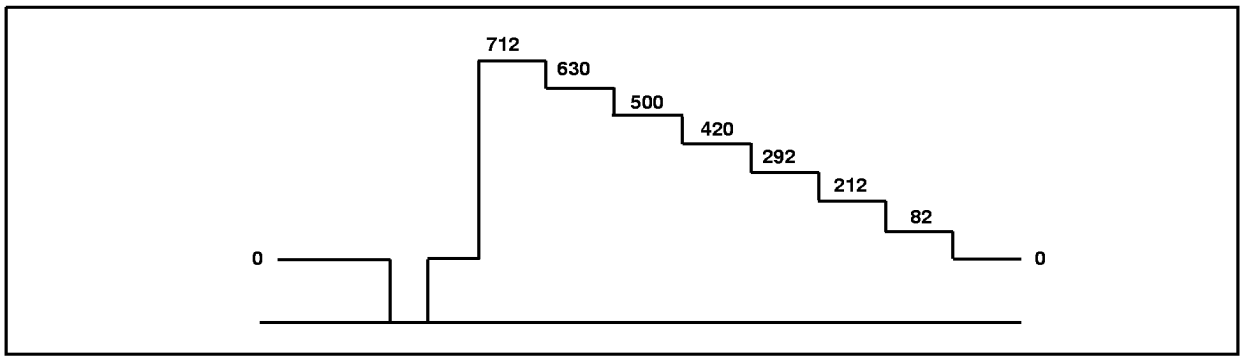

Figure 8 Y Output, SMPTE NTSC Pedestal off, (mV)

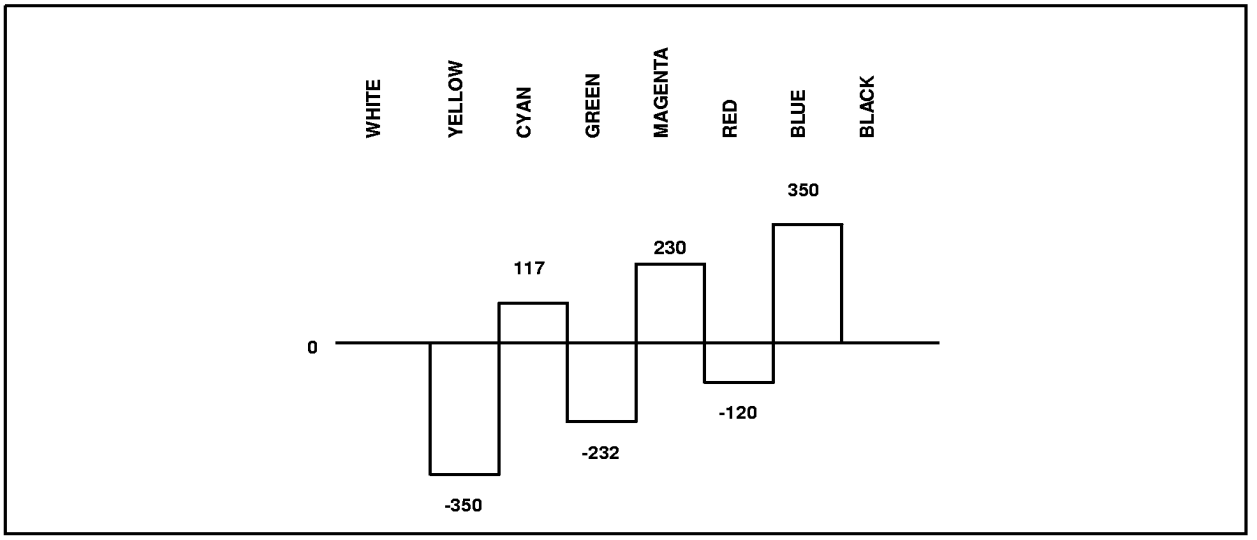

Figure 9 U output, SMPTE NTSC pedestal off, (mV)

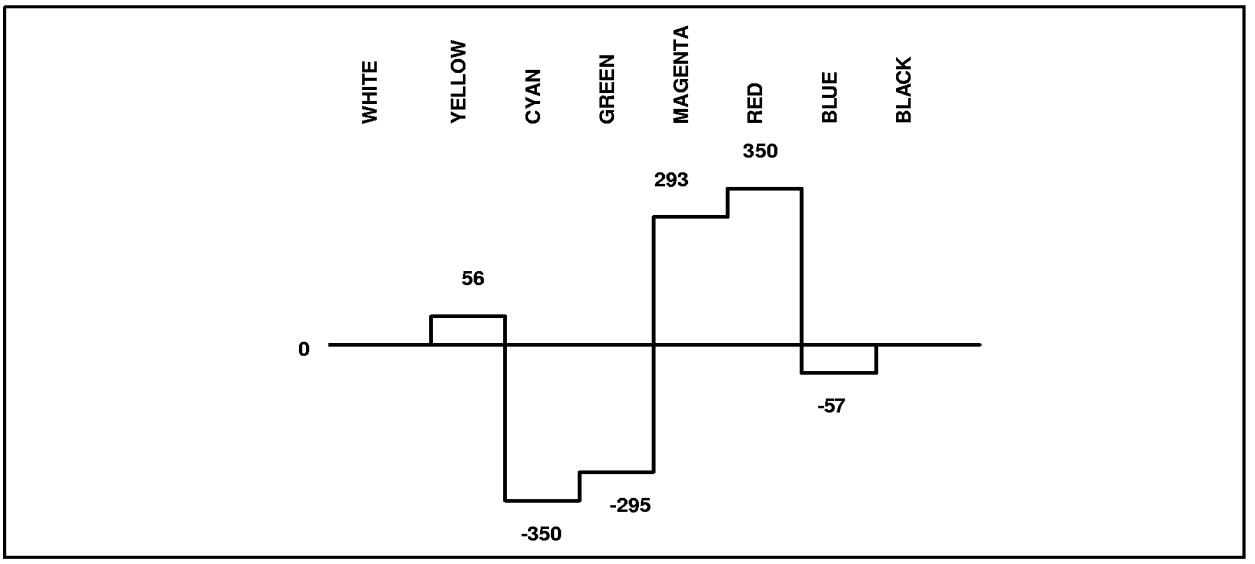

Figure 10 V output, SMPTE NTSC pedestal off, (mV)

The user has a choice of setting up the device for NTSC or PAL, the output levels shown here in Tables 7, 8 and 9, are based on the DACGAIN resistor being set for an output of 2.5mV per LSB. This gives accurate results in PAL mode but has a 2mV error in NTSC.

SMPTE Mode - Output Level (mV)

Colour	NTSC ped off				NTSC ped on			
	Luma	Luma*	U	V	Luma	Luma*	U	V
White	712	700	0	0	712	700	0	0
Yellow	630	620	-350	55	637	627	-325	50
Cyan	500	492	117	-350	517	507	107	-325
Green	420	412	-232	-295	440	435	-217	-275
Magenta	292	287	230	292	322	320	212	270
Red	212	207	-120	350	247	245	-112	325
Blue	82	80	350	-57	127	127	323	-55
Black	0	0	0	0	52	52	0	0
Blanck	0				0			
Sync	285				285			

Table 7

BetaCam Mode - Output Level (mV)

Colour	NTSC ped off				NTSC ped on			
	Luma	Luma*	U	V	Luma	Luma*	U	V
White	712	700	0	0	712	700	0	0
Yellow	630	620	-505	80	637	627	-467	75
Cyan	500	492	170	-505	517	507	157	-467
Green	420	412	-335	-425	440	435	-310	-392
Magenta	292	287	332	422	322	320	307	392
Red	212	207	-172	505	247	245	-160	467
Blue	82	80	505	-82	127	127	467	-75
Black	0	0	0	0	52	52	0	0
Blanck	0				0			
Sync	285				285			

Table 8

Note: *= LUMA_700 bit set to '1', otherwise bit is set to '0'

BetaCam and SMPTE Modes - Output Level (mV)

Colour	Pal		
	Luma	U	V
White	700	0	0
Yellow	620	-350	55
Cyan	492	117	-350
Green	412	-232	-295
Magenta	287	230	292
Red	207	-120	350
Blue	80	350	-57
Black	0	0	0
Blanking		0	
Sync		300	

Table 9

Note: LUMA_700 bit does not have any effect in PAL mode Luma is always 700mV peak.

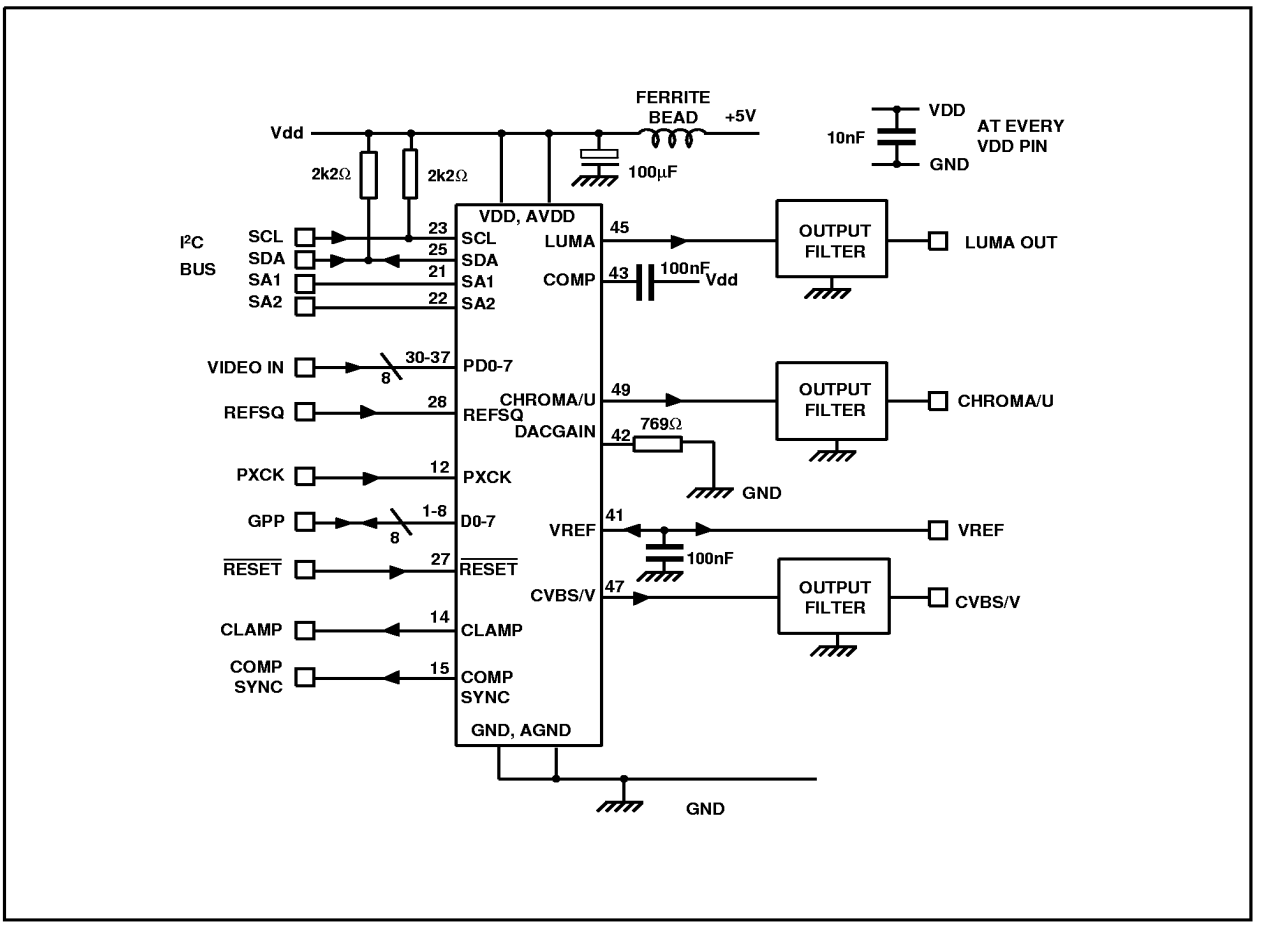

Figure 11 Typical application diagram, SLAVE mode. (Output filter - see Figure 13)

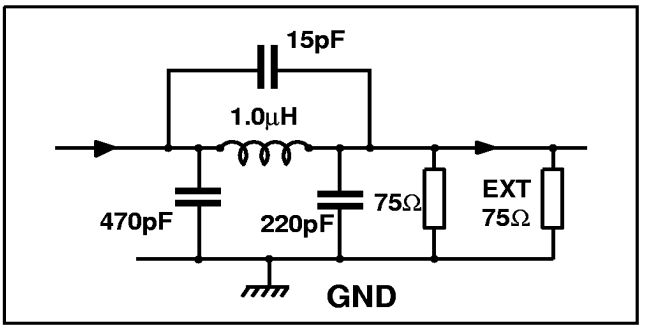

Figure 12 Output reconstruction filter

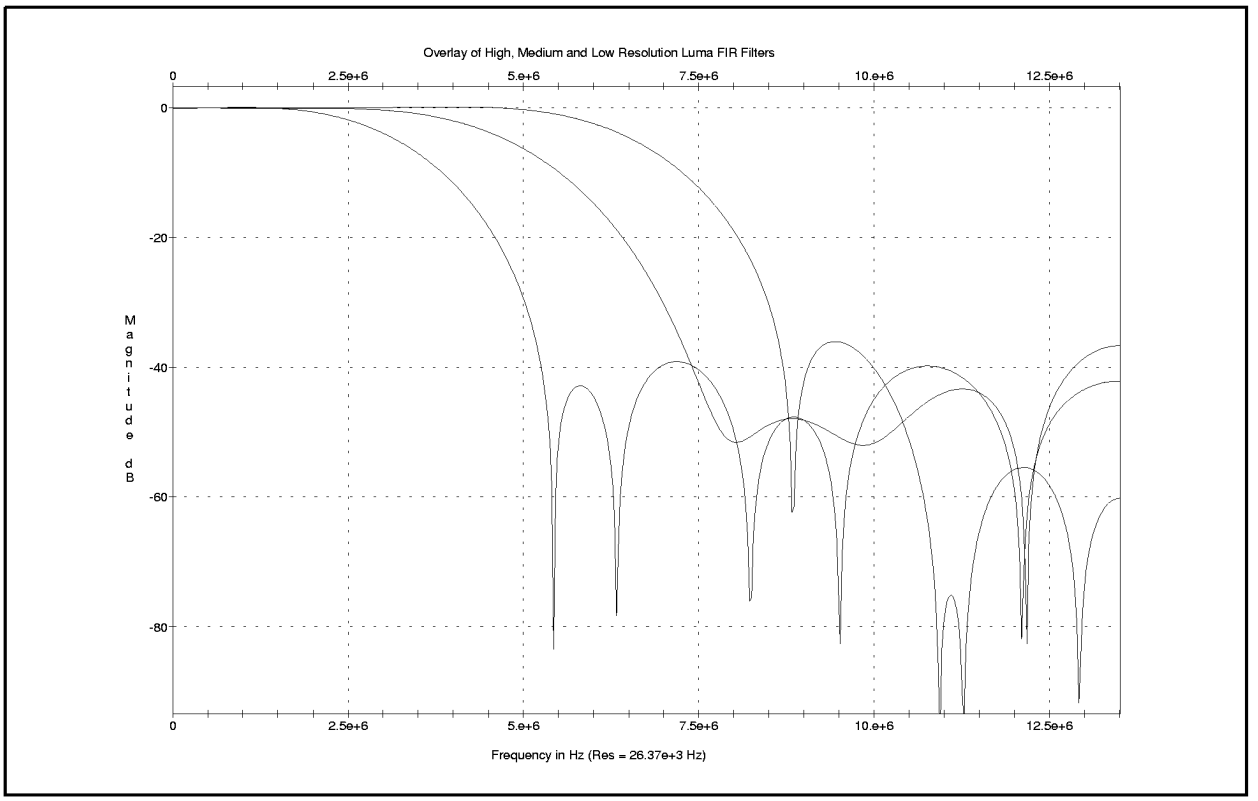

Figure 13 Response of Switchable Luma filter

Switchable Luma Filter

The internal luma interpolation filter can be set to three different frequency responses; low, medium and high, the latter being the default setting. Figure 13 shows the three responses and Table 10 below shows important performance parameters.

Filter Setting	-3dB point MHz	Pass Band MHz	Pass Band Ripple dB	Stop Band dB
Low	2.79	1.36	0.052	-40 @ 5.3MHz
Medium	4.34	2.17	0.058	-35 @ 7.2MHz
High	6.16	4.86	0.138	-36 @ 8.6MHz

Table 10 Luma Filter Performance

Note:

The VP5311D is only available to customers with a valid and existing authorisation to purchase issued by MACROVISION CORPORATION.