P54/74FCT374T/AT/CT—P54/74FCT534T/AT/CT
P54/74FCT564T/AT/CT—P54/74FCT574T/AT/CT
OCTAL D FLIP-FLOPS WITH 3-STATE OUTPUTS

FEATURES

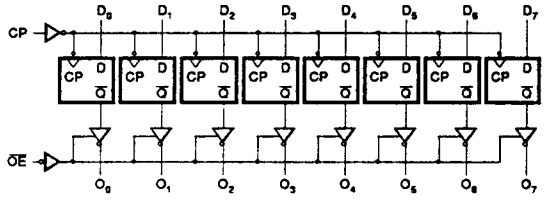
- **Function, Pinout and Drive Compatible with the FCT and F Logic**
- **FCT-C speed at 5.2ns max. (Com'l) FCT-A speed at 6.5ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **ESD protection exceeds 2000V**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **64 mA Sink Current (Com'l), 32 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)**
- **Edge Triggered D Type Inputs**
- **250 MHz Typical Toggle Rate**
- **Buffered Positive Edge Triggered Clock**
- **Manufactured in 0.7 micron PACE Technology™**

DESCRIPTION

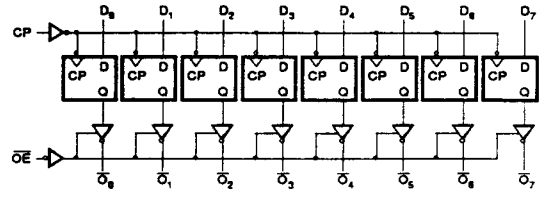
The 'FCT374T, 'FCT534T, 'FCT564T and 'FCT574T are high-speed low power octal D-type flip-flops featuring separate D-type inputs for each flip-flop. Both devices have 3-state outputs for bus oriented applications. A buffered clock (CP) and output enable ($\overline{OE}$) are common to all flip-flops. The 'FCT534T is the same as the 'FCT374T except that the outputs are inverted. The 'FCT574T is identical to 'FCT374T except that all the outputs are on one side of the package and inputs on the other side. The 'FCT564 is the same as the 'FCT574T except that the outputs are inverted. The eight flip-flops contained in the 'FCT374T, 'FCT534T, 'FCT564T and 'FCT574T will store the state of their individual D inputs that meet the setup and hold time requirements on the low-to-high clock (CP) transition. When $\overline{OE}$ is LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs will be in the high impedance state. The state of output enable does not affect the state of the flip-flops.

LOGIC DIAGRAMS

'FCT374T - 'FCT574T



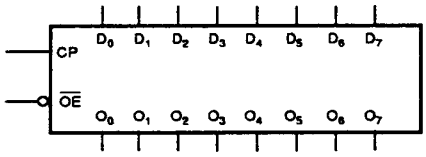
'FCT534T - 'FCT564T



1730 01

LOGIC SYMBOL

'FCT374T - 'FCT534T* - 'FCT564T* - FCT574T

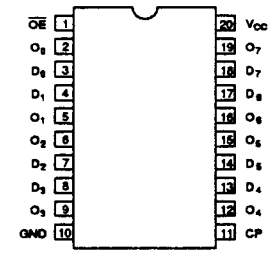


* $\overline{O}_n$ for 'FCT534T and 'FCT564T

1730 02

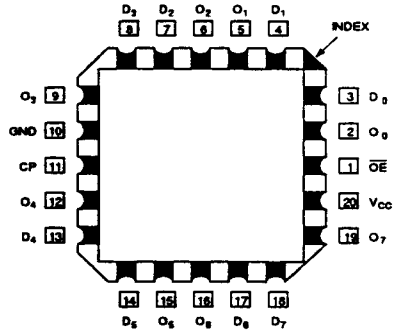
PIN CONFIGURATIONS

'FCT374T - 'FCT534T*



* $\overline{O}_n$ for 'FCT534T

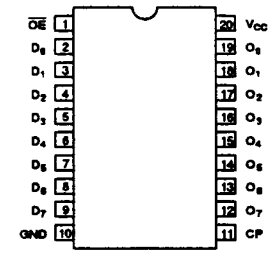
DIP(D2, P2)
SOIC (S2)



LCC(L2)

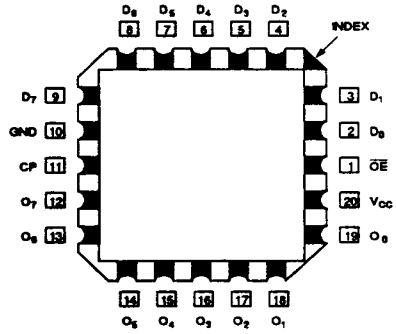
1730 03

'FCT564T - 'FCT574T



* $\overline{O}_n$ for 'FCT564T

DIP(D2, P2)
SOIC (S2)



LCC(L2)

1730 04

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

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Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

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Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

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Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I_{OL} = 32mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 64mA
I_I	Input HIGH Current				20	µA	MAX	V_{IN} = V_{CC}
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				–10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$

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Notes:

1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{os} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ mHz	V_{CC} = MAX, One Bit Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC}-0.2V$
I_C	Total Power Supply Current[5]	1.7	4.0	mA	V_{CC} = MAX, f_0 = 10MHz 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{OE}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.2	6.0	mA	V_{CC} = MAX, f_0 = 10MHz 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{OE}$ = GND, V_{IN} = 3.4V or V_{IN} = GND
		4.0	7.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		6.2	16.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND, V_{IN} = 3.4V or V_{IN} = GND

1730 Tbl 06

Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

TRUTH TABLE

Inputs			Outputs 'FCT374T–'FCT574T	Outputs 'FCT534T–'FCT564T
D_n	CP	$\overline{OE}$	O_n	$\overline{O}_n$
H	⌐	L	H	L
L	⌐	L	L	H
X	X	H	Z	Z

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H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
⌐ = LOW-to-HIGH clock transition
Z = HIGH Impedance

AC CHARACTERISTICS

Sym.	Parameter	'FCT374T-'FCT534T 'FCT564T-'FCT574T				'FCT374AT-'FCT534AT 'FCT564AT-'FCT574AT				'FCT374CT-'FCT534CT 'FCT564CT-'FCT574CT				Units	Fig. No.
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Prop. Delay Clock to Output	2.0	11.0	2.0	10.0	2.0	7.2	2.0	6.5	2.0	6.2	2.0	5.2	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5	14.0	1.5	12.5	1.5	7.5	1.5	6.5	1.5	6.2	1.5	5.5	ns	1,7,8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	8.0	1.5	8.0	1.5	6.5	1.5	5.5	1.5	5.7	1.5	5.0	ns	1,7,8

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Note:
1. AC Characteristics guaranteed with C_L = 50pF as shown in Figure 1.

AC CHARACTERISTICS

Sym.	Parameter	'FCT374T–'FCT534T 'FCT564T–'FCT574T				'FCT374AT–'FCT534AT 'FCT564AT–'FCT574AT				'FCT374CT–'FCT534CT 'FCT564CT–'FCT574CT				Units	Fig. No.
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
$t_S(H)$ $t_S(L)$	Setup Time, High or Low D_n to CP	2.0	–	2.0	–	2.0	–	2.0	–	2.0	–	2.0	–	ns	4
$t_n(H)$ $t_n(L)$	Hold Time, High or Low D_n to CP	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	ns	
$t_W(H)$ $t_W(L)$	Clk Pulse Width[2] High or Low	7.0	–	7.0	–	6.0	–	5.0	–	6.0	–	5.0	–	ns	5

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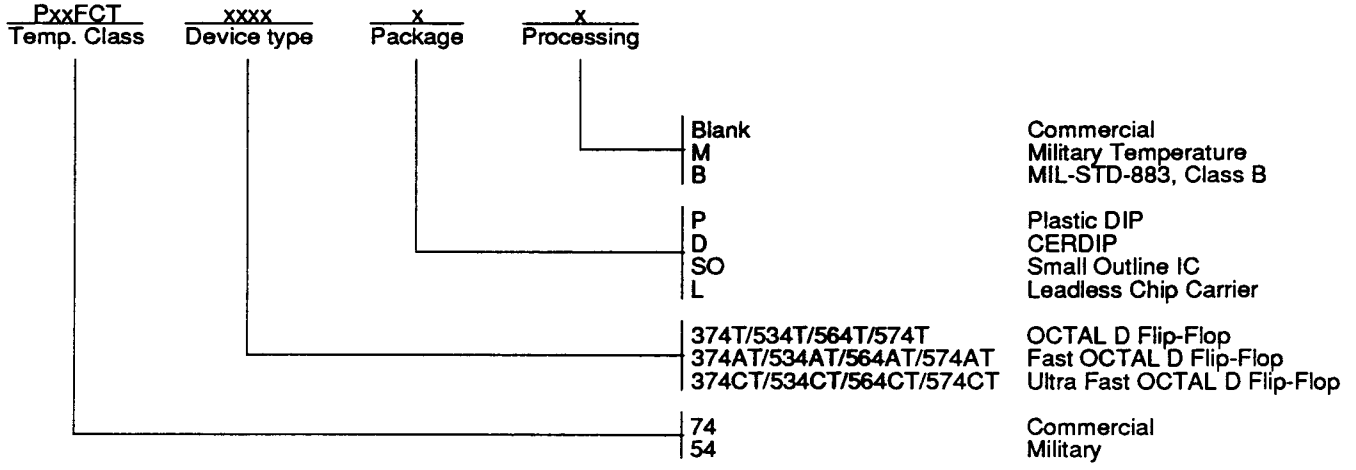
Notes:
1. Minimum limits are guaranteed but not tested on Propagation Delays.
2. With one data channel toggling, $t_W(L) = t_W(H) = 4.0ns$ and $t_r = t_f = 1.0ns$.

ORDERING INFORMATION



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