

Description

The μ PD424101 is a nibble-mode dynamic RAM organized as 4,194,304 words by 1 bit and designed to operate from a single +5-volt power supply. Advanced polycide technology using trench capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state output is controlled by $\overline{\text{CAS}}$ independent of $\overline{\text{RAS}}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{\text{CAS}}$ low. The data output is returned to high impedance by returning $\overline{\text{CAS}}$ high. Nibble-mode read and write cycles can be executed by cycling $\overline{\text{CAS}}$.

Refreshing may be accomplished by a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycle that internally generates the refresh address. Refreshing can also be accomplished by $\overline{\text{RAS}}$ -only refresh cycles or by normal read or write cycles on the 1024 address combinations of $A_0 - A_9$ during a 16-ms refresh period.

Features

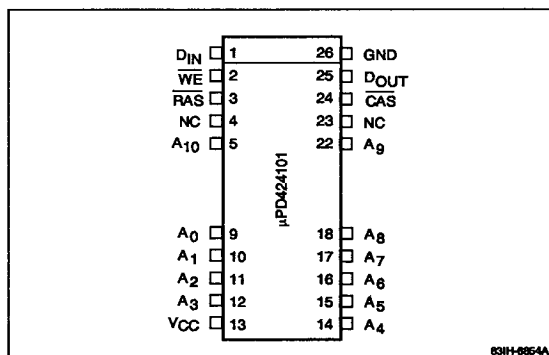
- 4,194,304-word by 1-bit organization
- Single +5-volt power supply
- Nibble-mode option
- Low power dissipation
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles
- Multiplexed address inputs
- On-chip substrate bias generator
- Nonlatched, three-state outputs
- Low input capacitance
- TTL-compatible inputs and outputs
- 1024 refresh cycles every 16 ms
- 26/20-pin SOJ, 20-pin ZIP, or 26/20-pin TSOP plastic packaging

Pin Identification

Name	Function
$A_0 - A_{10}$	Address inputs
$\overline{\text{CAS}}$	Chip select
D_{IN}	Data input
D_{OUT}	Data output
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{WE}}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

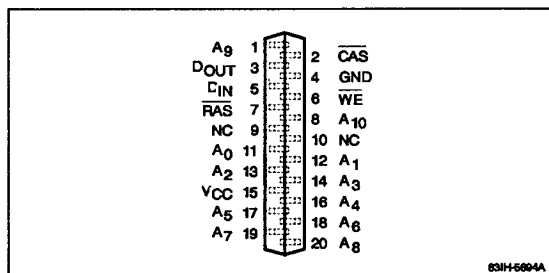
Pin Configurations

26/20-Pin Plastic SOJ



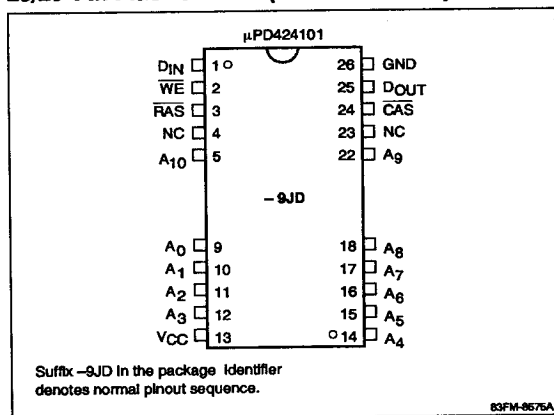
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20-Pin Plastic ZIP

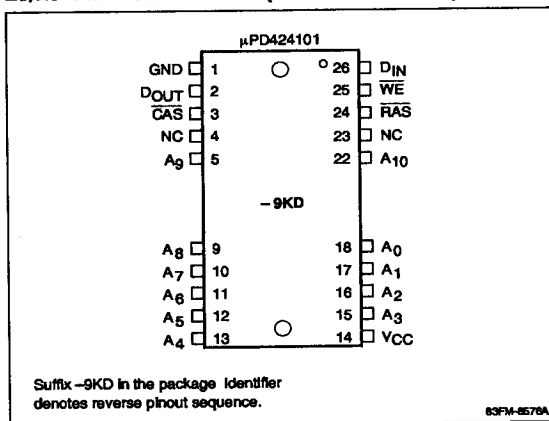


Pin Configurations (cont)

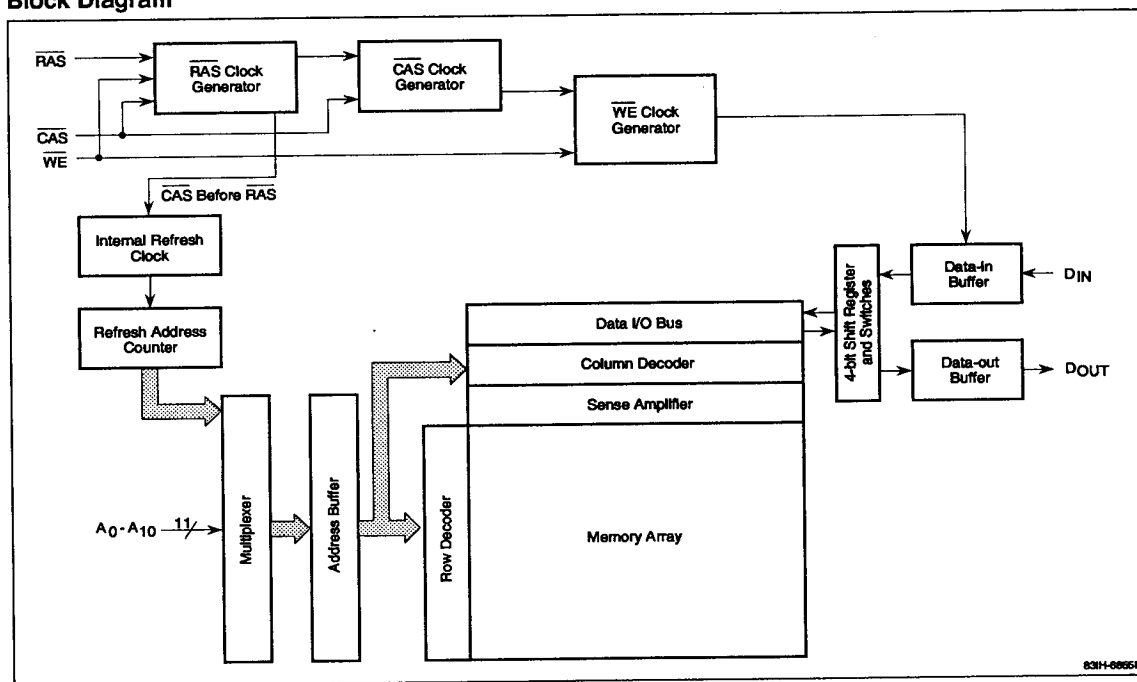
26/20-Pin Plastic TSOP (Normal Pinouts)



26/20-Pin Plastic TSOP (Reverse Pinouts)



Block Diagram



Ordering Information

Part Number	RAS Access Time	R/W Cycle Time	Nibble Cycle Time	Refresh Period	Standby Current	Package
μPD424101LA-60	60 ns	120 ns	40 ns	16 ms	1 mA	26/20-pin plastic SOJ (300-mil)
LA-70	70 ns	140 ns	40 ns			
LA-80	80 ns	160 ns	40 ns			
LA-10	100 ns	190 ns	45 ns			
μPD424101LA-60L	60 ns	120 ns	40 ns	128 ms	300 μA	
LA-70L	70 ns	140 ns	40 ns			
LA-80L	80 ns	160 ns	40 ns			
LA-10L	100 ns	190 ns	45 ns			
μPD424101V-60	60 ns	120 ns	40 ns	16 ms	1 mA	20-pin plastic ZIP
V-70	70 ns	140 ns	40 ns			
V-80	80 ns	160 ns	40 ns			
V-10	100 ns	190 ns	45 ns			
μPD424101V-60L	60 ns	120 ns	40 ns	128 ms	300 μA	
V-70L	70 ns	140 ns	40 ns			
V-80L	80 ns	160 ns	40 ns			
V-10L	100 ns	190 ns	45 ns			
μPD424101GS-60	60 ns	120 ns	40 ns	16 ms	1 mA	26/20-pin plastic TSOP (normal pinouts)
GS-70	70 ns	140 ns	40 ns			
GS-80	80 ns	160 ns	40 ns			
GS-10	100 ns	190 ns	45 ns			
μPD424101GS-60L	60 ns	120 ns	40 ns	128 ms	300 μA	
GS-70L	70 ns	140 ns	40 ns			
GS-80L	80 ns	160 ns	40 ns			
GS-10L	100 ns	190 ns	45 ns			
μPD424101GSM-60	60 ns	120 ns	40 ns	16 ms	1 mA	26/20-pin plastic TSOP (reverse pinouts)
GSM-70	70 ns	140 ns	40 ns			
GSM-80	80 ns	160 ns	40 ns			
GSM-10	100 ns	190 ns	45 ns			
μPD424101GSM-60L	60 ns	120 ns	40 ns	128 ms	300 μA	
GSM-70L	70 ns	140 ns	40 ns			
GSM-80L	80 ns	160 ns	40 ns			
GSM-10L	100 ns	190 ns	45 ns			

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Absolute Maximum Ratings

Voltage on any pin relative to GND	-1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	-55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		$V_{CC} + 1.0$	V
Input voltage, low	V_{IL}	-1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Capacitance

$T_A = 25^\circ\text{C}$; $f = 1\text{ MHz}$

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Address, D_{IN}
	C_{I2}	7	pF	$\overline{RAS}$, CAS , $\overline{WE}$
Output capacitance	C_O	7	pF	D_{OUT}

DC Characteristics

$T_A = 0\text{ to }+70^\circ\text{C}$; $V_{CC} = +5.0\text{ V} \pm 10\%$

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		2.0	mA	$\overline{RAS} = \overline{CAS} \geq V_{IH}(\text{min})$
			1.0	mA	$\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2\text{ V}$
Input leakage current	$I_{I(L)}$	-10	10	μA	$V_{IN} = 0\text{ V to }V_{CC}$; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	-10	10	μA	D_{OUT} disabled; $V_{OUT} = 0\text{ V to }V_{CC}$
Output voltage, low	V_{OL}		0.4	V	$I_{OL} = 4.2\text{ mA}$
Output voltage, high	V_{OH}	2.4		V	$I_{OH} = -5\text{ mA}$

Low-Power Battery Backup (-L Versions Only)

Symbol	Max	Unit	t_{RAS}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	Standby Conditions
I_{CC6}	500	μA	$\leq 1\text{ }\mu\text{s}$	1024 refresh cycles (min) every 128 ms; $\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2\text{ V}$ or $\leq 0.2\text{ V}$, as appropriate; D_{OUT} open; all other inputs $\geq V_{CC} - 0.2\text{ V}$ or $\leq 0.2\text{ V}$	$\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2\text{ V}$; D_{IN} , $\overline{WE}$, Addresses $\geq V_{CC} - 0.2\text{ V}$ or $\leq 0.2\text{ V}$; D_{OUT} open
	300	μA	$\leq 200\text{ }\mu\text{s}$		
t_{REF}	128	ms			

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	μPD424101-60		μPD424101-70		μPD424101-80		μPD424101-10		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
Operating current, average	I _{CC1}		120		100		90		80	mA	RAS and CAS cycling; t _{RC} = t _{RC} min; I _O = 0 mA (Note 5)
Operating current, RAS-only refresh cycle, average	I _{CC3}		120		100		90		80	mA	RAS cycling; CAS ≥ V _{IH} ; t _{RC} = t _{RC} min; I _O = 0 mA (Note 5)
Operating current, nibble mode, average	I _{CC4}		80		80		70		60	mA	RAS ≤ V _{IL} ; CAS cycling; t _{NC} = t _{NC} min; I _O = 0 mA (Note 5)
Operating current, CAS before RAS refresh cycle, average	I _{CC5}		120		100		90		80	mA	RAS cycling; CAS before RAS; t _{RC} = t _{RC} min; I _O = 0 mA (Note 5)
Access time from column address	t _{AA}		30		35		40		50	ns	(Notes 7, 9)
Column address setup time	t _{ASC}	0		0		0		0		ns	
Row address setup time	t _{ASR}	0		0		0		0		ns	
Column address to WE delay time	t _{AWD}	30		35		40		50		ns	(Note 16)
Access time from CAS (falling edge)	t _{CAC}		20		20		20		25	ns	(Notes 7, 9)
Column address hold time	t _{CAH}	15		15		15		20		ns	
CAS pulse width	t _{CAS}	20	10,000	20	10,000	20	10,000	25	10,000	ns	
CAS hold time for CAS before RAS refresh cycle	t _{CHR}	15		15		15		20		ns	
CAS precharge time, non-nibble cycle	t _{CPN}	10		10		10		10		ns	
CAS to RAS precharge time	t _{CRP}	10		10		10		10		ns	(Note 12)
CAS hold time	t _{CSH}	60		70		80		100		ns	
CAS setup time for CAS before RAS refresh cycle	t _{CSR}	10		10		10		10		ns	
CAS to WE delay	t _{CWD}	20		20		20		25		ns	(Note 16)
Write command to CAS lead time	t _{CWL}	15		15		15		20		ns	
Data-in hold time	t _{DH}	15		15		15		20		ns	(Note 15)
Data-in setup time	t _{DS}	0		0		0		0		ns	(Note 15)
Nibble mode access time	t _{NAC}		20		20		20		25	ns	

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AC Characteristics (cont)

Parameter	Symbol	μPD424101-60		μPD424101-70		μPD424101-80		μPD424101-10		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
CAS pulse width in nibble mode	t _{NAS}	20		20		20		25		ns	
Nibble mode cycle time	t _{NC}	40		40		40		45		ns	
CAS to $\overline{WE}$ delay in nibble mode	t _{NCWD}	20		20		20		25		ns	
Write command to CAS lead time in nibble mode	t _{NCWL}	15		15		20		25		ns	
CAS precharge time in nibble mode	t _{NP}	10		10		10		10		ns	
RAS hold time for nibble read cycle	t _{NRRSH}	20		20		20		25		ns	
RAS hold time for nibble write cycle	t _{NWRSH}	20		20		20		25		ns	
Output buffer turnoff delay	t _{OFF}	0	15	0	15	0	20	0	25	ns	(Note 10)
Access time from RAS	t _{RAC}		60		70		80		100	ns	(Notes 7, 8)
RAS to column address delay time	t _{RAD}	15	30	15	35	17	40	17	50	ns	(Note 9)
Row address hold time	t _{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t _{RAL}	30		35		40		50		ns	
RAS pulse width	t _{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
RAS pulse width in nibble mode	t _{RASP}	60	125,000	70	125,000	80	125,000	100	125,000	ns	
Random read or write cycle time	t _{RC}	120		140		160		190		ns	(Note 6)
RAS to CAS delay time	t _{RCD}	20	40	20	50	25	60	25	75	ns	(Note 11)
Read command hold time referenced to $\overline{CAS}$	t _{RCH}	0		0		0		0		ns	(Note 13)
Read command setup time	t _{RCS}	0		0		0		0		ns	
Refresh period	t _{REF}		16		16		16		16	ms	Addresses A ₀ - A ₉
RAS precharge time	t _{RP}	50		60		70		80		ns	
$\overline{RAS}$ precharge CAS hold time	t _{RPC}	10		10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t _{RRH}	10		10		10		10		ns	(Note 13)
RAS hold time	t _{RSH}	20		20		20		25		ns	

AC Characteristics (cont)

Parameter	Symbol	μPD424101-60		μPD424101-70		μPD424101-80		μPD424101-10		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
Read-write cycle time	t_{RWC}	145		165		185		220		ns	(Note 6)
RAS to $\overline{WE}$ delay	t_{RWD}	60		70		80		100		ns	(Note 16)
Write command to RAS lead time	t_{RWL}	20		20		20		25		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	15		15		15		20		ns	
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 16)
$\overline{WE}$ hold time	t_{WHR}	15		15		15		20		ns	
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 14)
$\overline{WE}$ setup time	t_{WSR}	10		10		10		10		ns	

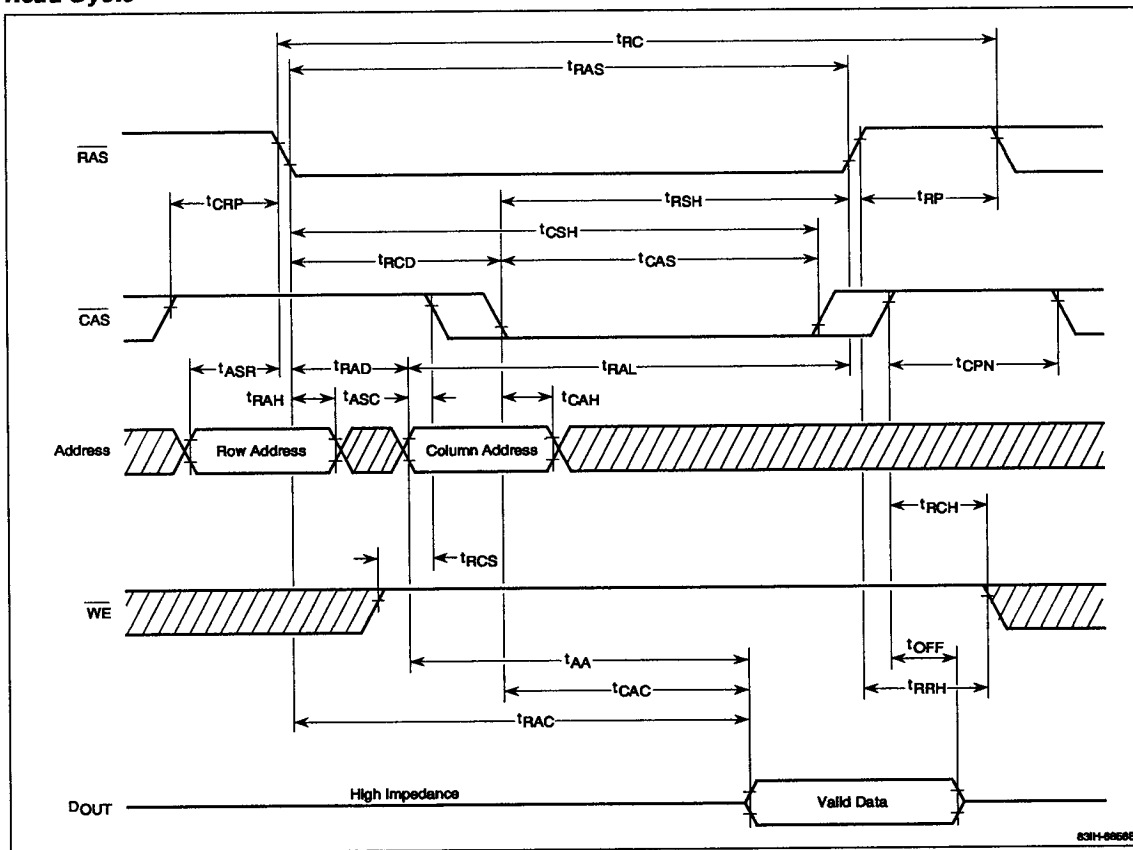
Notes:

- (1) All voltages are referenced to GND.
- (2) An initial pause of 100 μ s is required after power-up, followed by any eight RAS cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a RAS-only refresh or a CAS before RAS refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.
- (3) Ac measurements assume $t_T = 5$ ns.
- (4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL} .
- (5) I_{CC1} , I_{CC3} , I_{CC4} , and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during RAS-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each nibble cycle.
- (6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range ($T_A = 0$ to $+70^\circ\text{C}$) is assured.
- (7) Load = 2 TTL (-1 mA, $+4$ mA) loads and 100 pF.
- (8) Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.
- (9) If $t_{RAD} \geq t_{RAD}(\text{max})$, then the access time is defined by t_{AA} .
- (10) $t_{OFF}(\text{max})$ defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL} .
- (11) Operation within the $t_{RCD}(\text{max})$ limit assures that $t_{RAC}(\text{max})$ can be met. $t_{RCD}(\text{max})$ is specified as a reference point only; if t_{RCD} is greater than $t_{RCD}(\text{max})$, then access time is controlled exclusively by t_{CAC} .
- (12) The t_{CDP} requirement should be applicable for RAS/CAS cycles preceded by any cycle.
- (13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
- (14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.
- (15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.
- (16) t_{WCS} , t_{RWD} , t_{CWD} , and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}(\text{min})$, $t_{RWD} \geq t_{RWD}(\text{min})$, and $t_{AWD} \geq t_{AWD}(\text{min})$, the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.
- (17) A test mode may be initiated by executing a $\overline{CAS}$ before RAS refresh cycle with $\overline{WE}$ held at V_{IL} . This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH} , either a RAS-only or CAS before RAS refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

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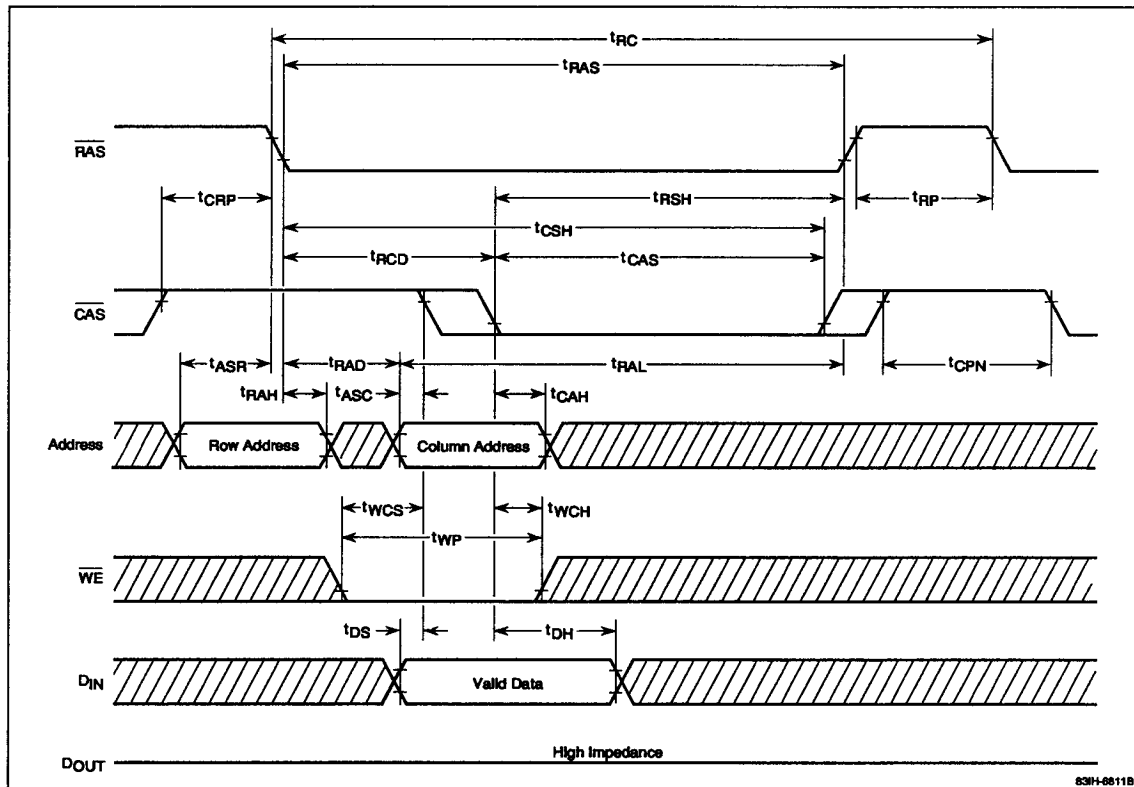
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

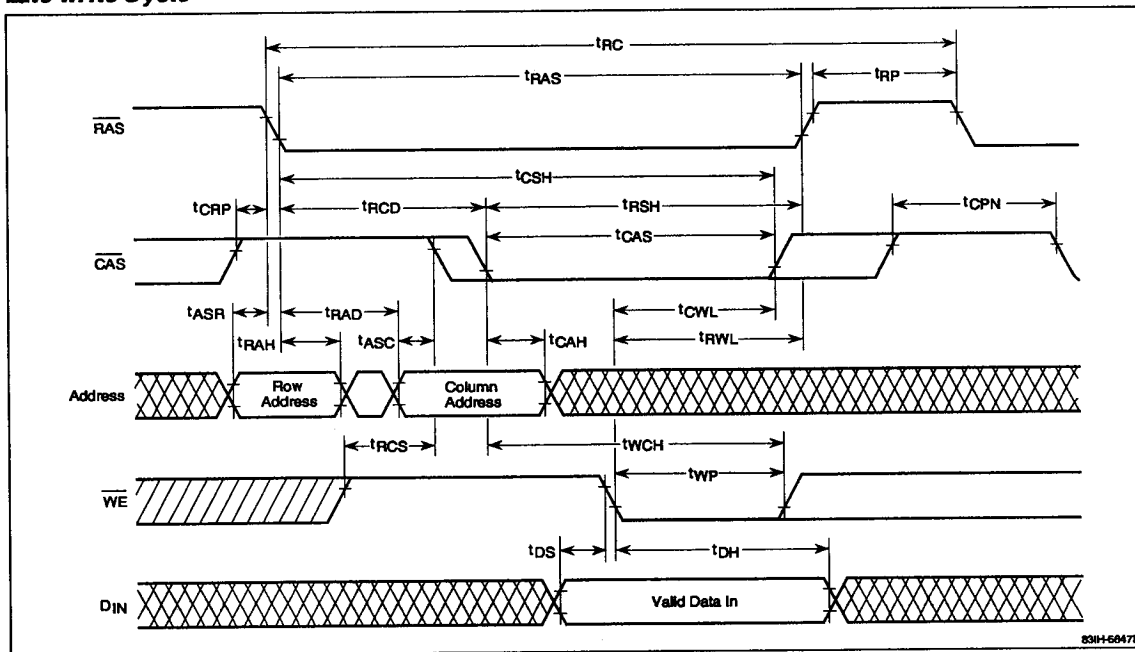
Early Write Cycle



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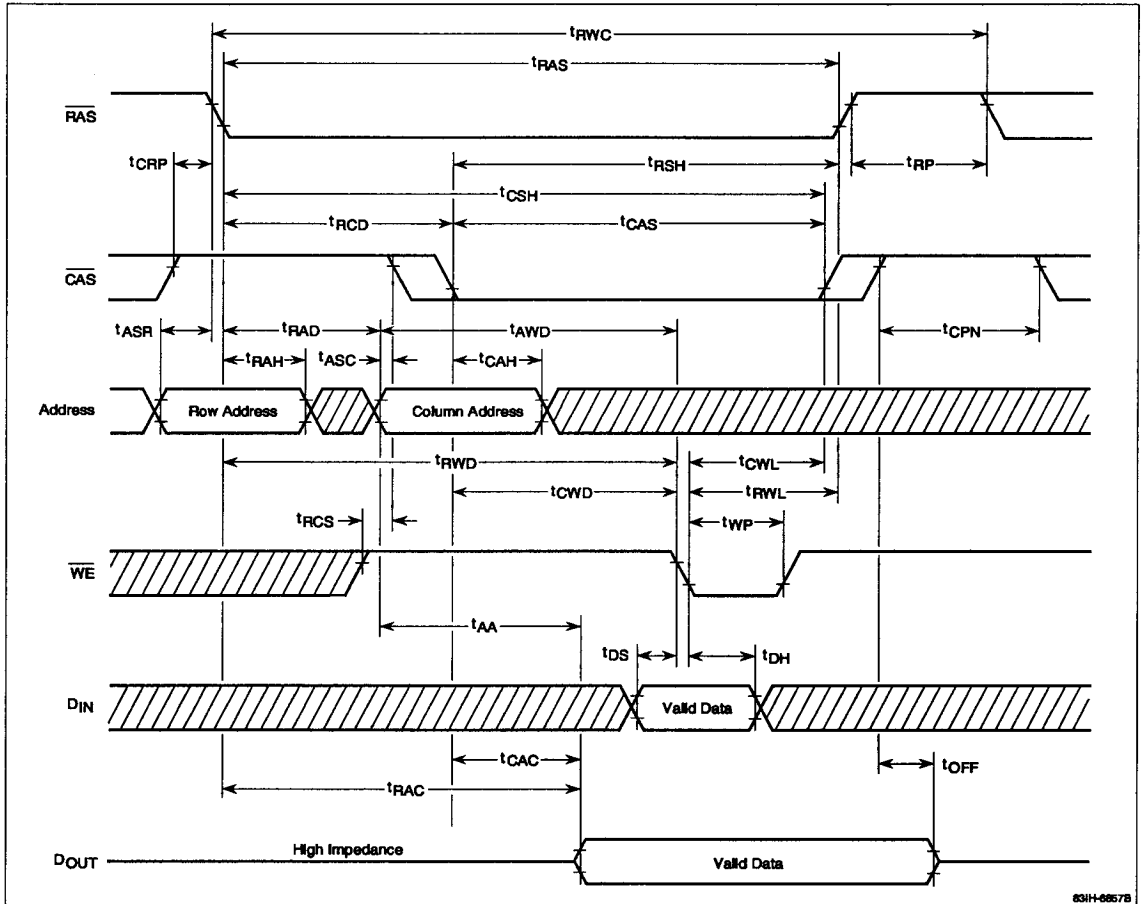
Timing Waveforms (cont)

Late Write Cycle



Timing Waveforms (cont)

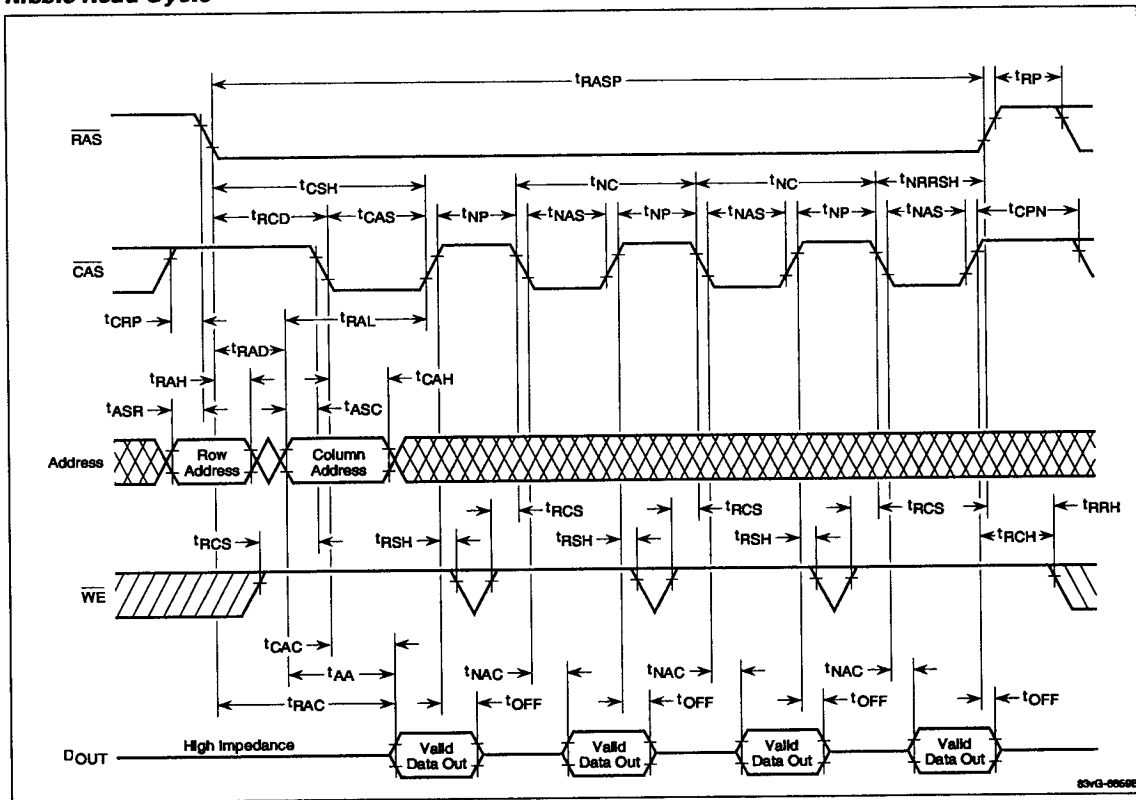
Read-Write/Read-Modify-Write Cycle



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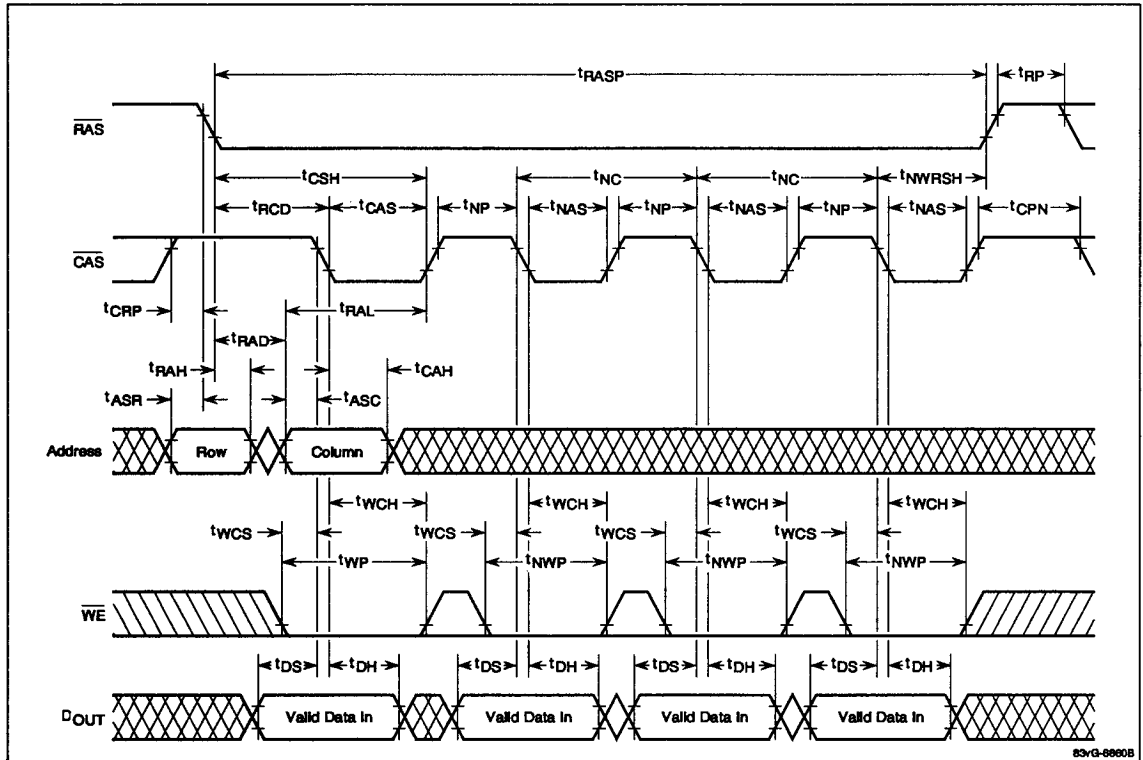
Timing Waveforms (cont)

Nibble Read Cycle



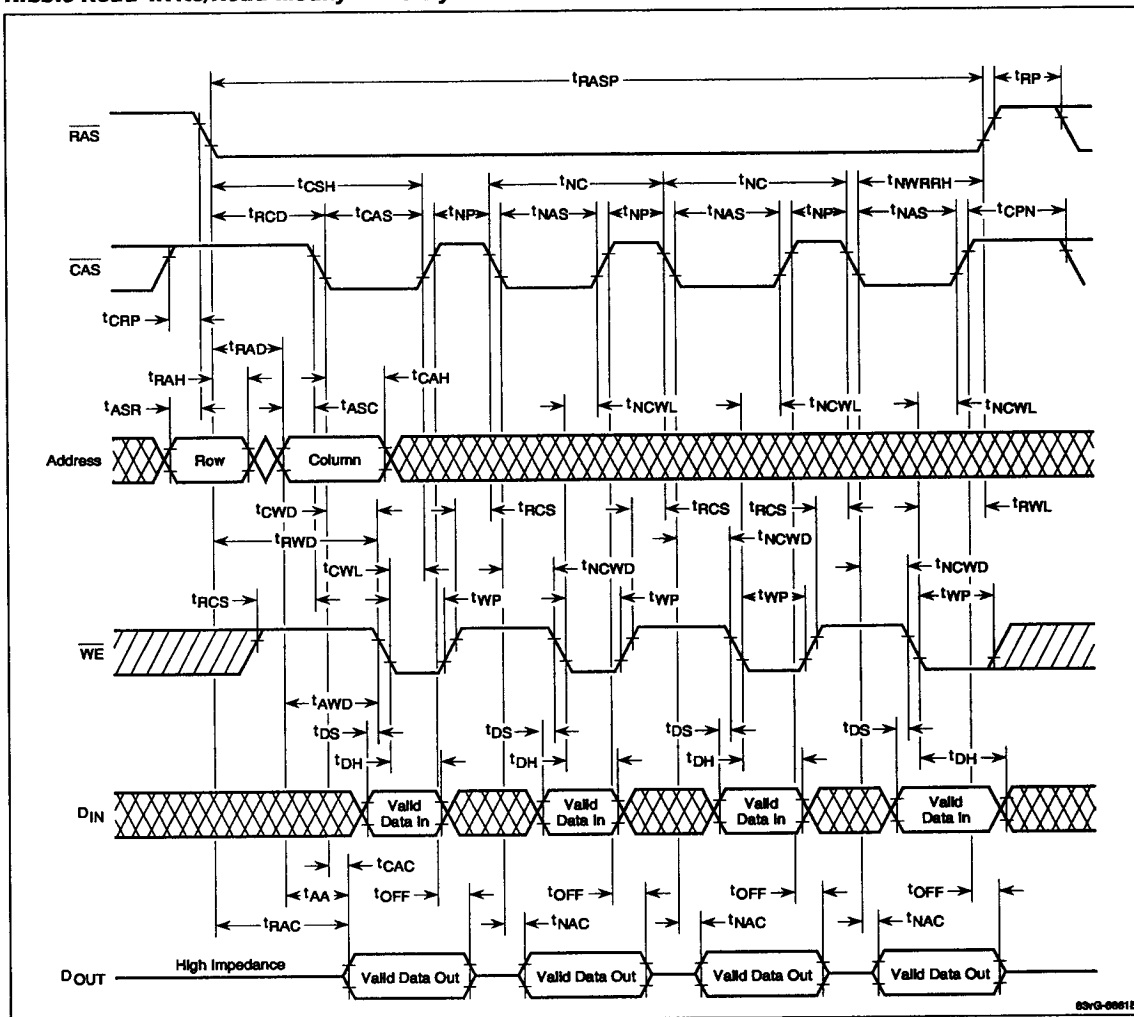
Timing Waveforms (cont)

Nibble Early Write Cycle



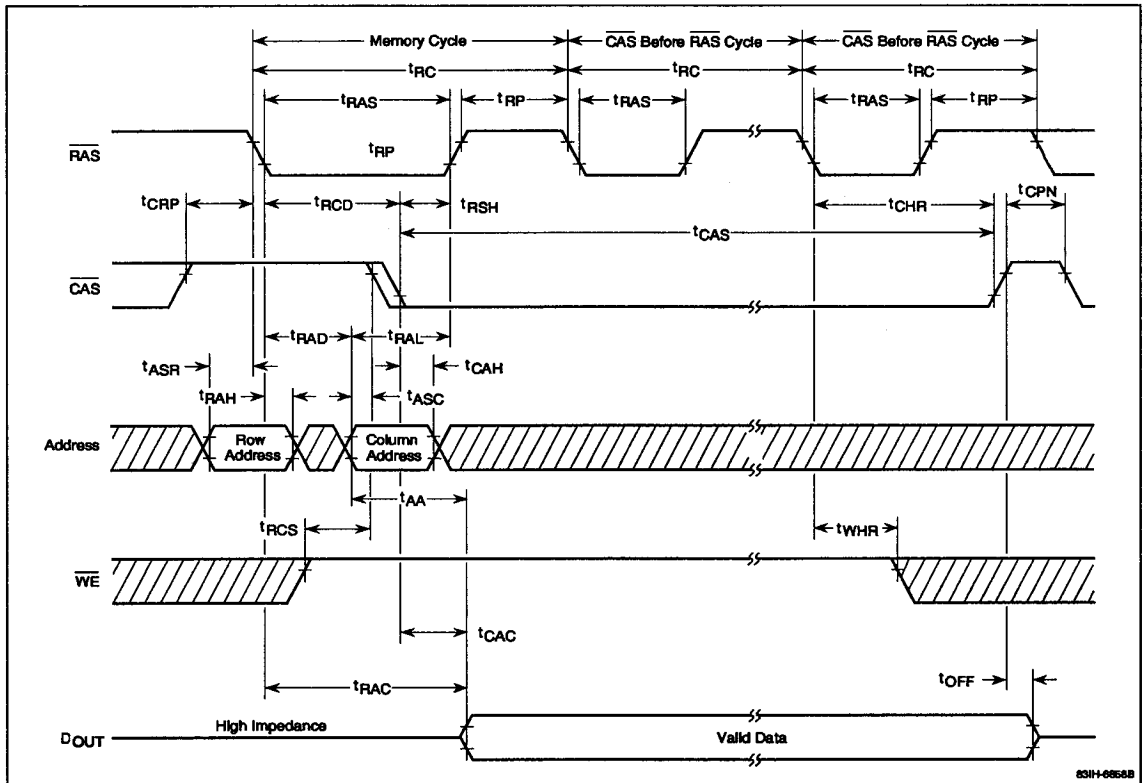
Timing Waveforms (cont)

Nibble Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

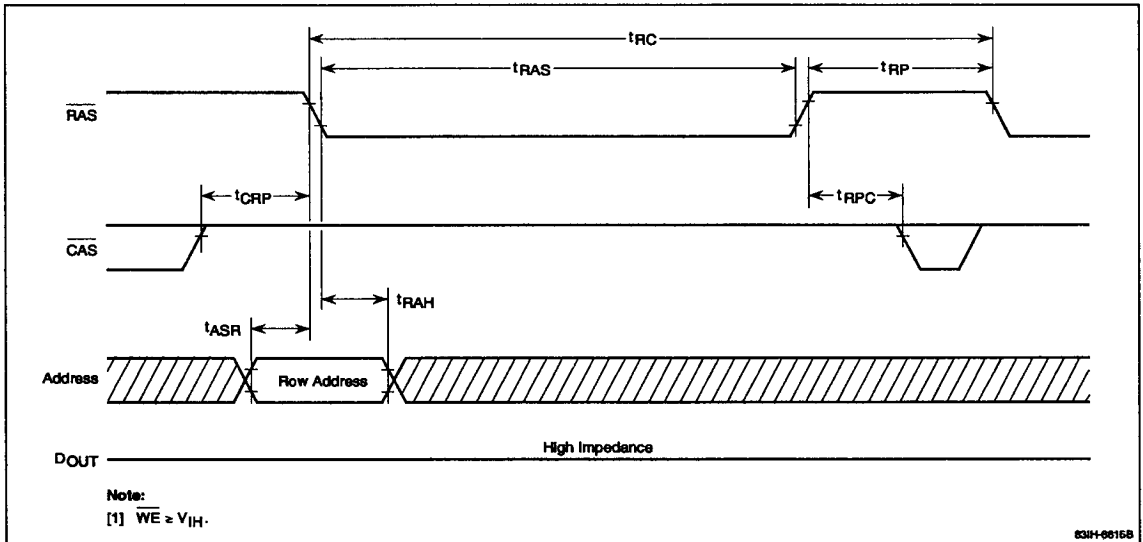
Hidden Refresh Cycle



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Timing Waveforms (cont)

RAS-Only Refresh Cycle



CAS Before RAS Refresh Cycle

