NEC

MOS INTEGRATED CIRCUIT

μPD431009

1M-BIT CMOS FAST STATIC RAM
128K-WORD BY 9-BIT

Description

The μPD431009 is a high speed, low power, 1 179 072 bits (131 072 words by 9 bits) CMOS static RAM.
The μPD431009 is packed in 36-pin plastic SOJ.

Feature

- 131 072 words by 9 bits organization
- Fast access time 15, 17, 20 ns (MAX.)
- Output buffers control: $\overline{OE}$
- Common I/O using three state outputs
- Fully static operation: no clock or refreshing to operate
- TTL compatible: all inputs and outputs
- Single +5 V power supply

Ordering Information

Part number	Package	Access time ns (MAX.)	Operating supply current mA (MAX.)	Standby supply current mA (MAX.)	Quality grade
μPD431009LE-15	36-pin plastic SOJ (400 mil)	15	160	10	Standard
μPD431009LE-17		17	150		
μPD431009LE-20		20	140		

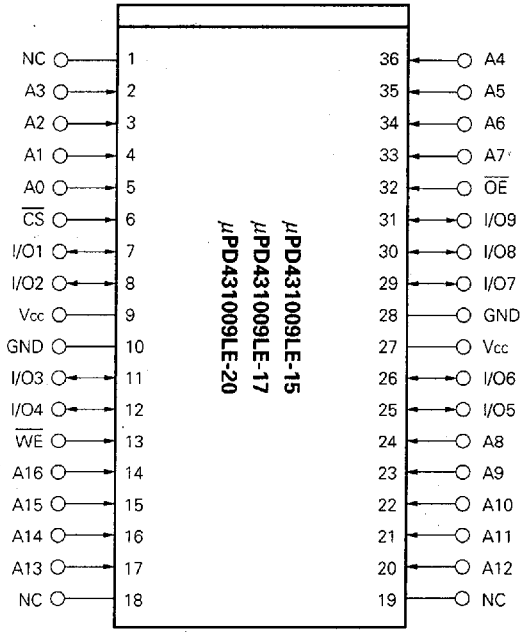
Remark Operating supply current is 120 mA (MAX.) when this product is used at 50ns cycle time.

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Document No. IC-3237

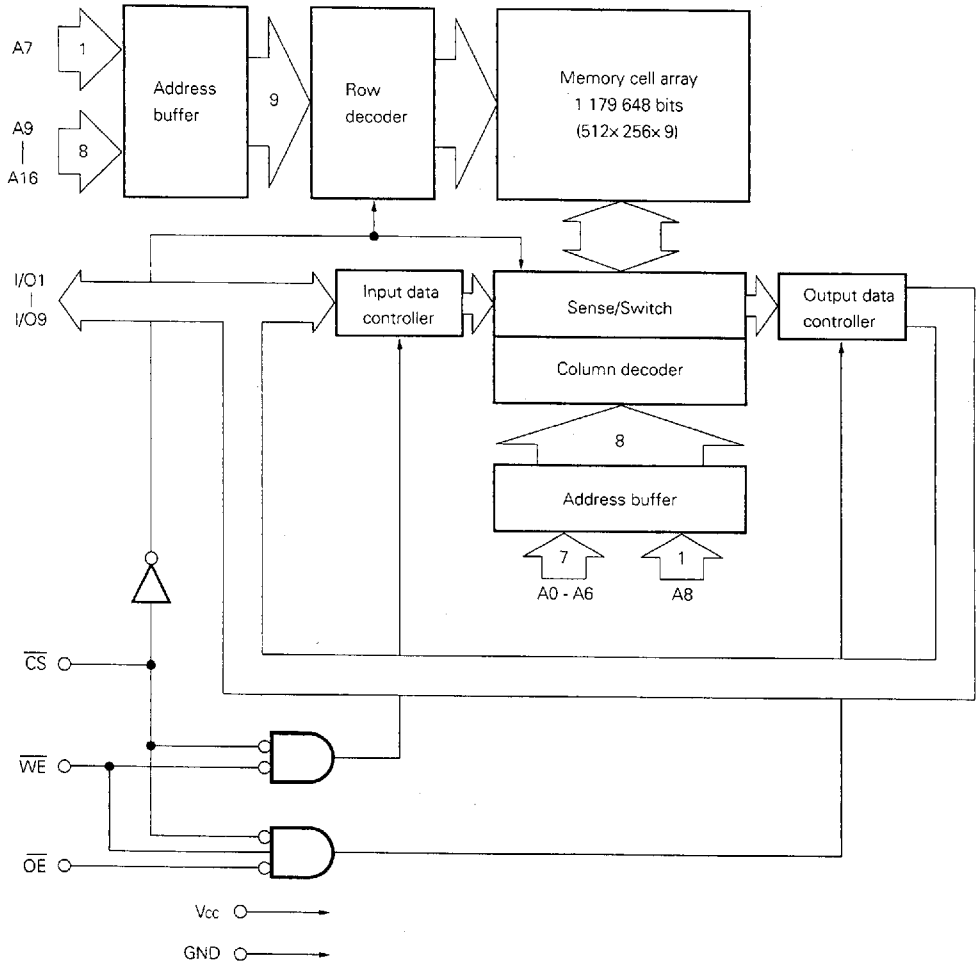
Pin Configuration (Marking Side)

36-Pin Plastic SOJ (400 mil)



A0 to A16	:	Address Inputs
I/O1 to I/O9	:	Data Inputs/Outputs
$\overline{CS}$	:	Chip Select
$\overline{WE}$	:	Write Enable
$\overline{OE}$	:	Output Enable
Vcc	:	Power Supply
GND	:	Ground
NC	:	No Connection

Block Diagram



Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Supply current
H	×	×	Not selected	Hi-Z	I_{SB}
L	L	H	Read	D_{OUT}	I_{CC}
L	×	L	Write	D_{IN}	
L	H	H	Output disable	Hi-Z	

Remark × : Don't care

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.5[Note] to +7.0	V
Input/Output voltage	V_T	−0.5 [Note] to V_{CC} +0.5	V
Operating temperature	T_{opt}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C

Note −3.0 V (MIN.) (Pulse width: 10 ns)

Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
High level input voltage	V_{IH}	2.2		V_{CC} +0.5	V
Low level input voltage	V_{IL}	−0.5[Note]		+0.8	V
Ambient temperature	T_a	0		+70	°C

Note −3.0 V (MIN.) (Pulse width: 10 ns)

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}		−2		+2	μA
Output leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC}, $\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}		−2		+2	μA
Operating supply current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA	Cycle time: 15 ns			160	mA
			Cycle time: 17 ns			150	
			Cycle time: 20 ns			140	
			Cycle time: 50 ns			120	
Standby supply current	I_{SB}	$\overline{CS}$ = V_{IH}; V_{IN} = V_{IH} or V_{IL}				30	mA
	I_{SB1}	V_{CC} − 0.2 V ≦ $\overline{CS}$, V_{IN} ≦ 0.2 V or V_{CC} − 0.2 V ≦ V_{IN}				10	
High level output voltage	V_{OH}	I_{OH} = −4.0 mA		2.4			V
Low level output voltage	V_{OL}	I_{OL} = 8 mA				0.4	V

Remark V_{IN}: Input voltage

Capacitance (T_a = +25 °C, f = 1 MHz)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V			6	pF
Input/Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			8	pF

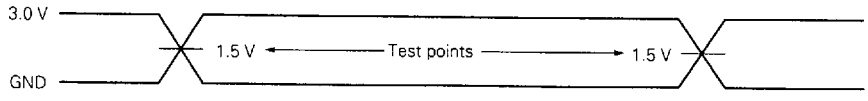
Remark 1. V_{IN}: Input voltage

2. These parameters are periodically sampled and not 100 % tested.

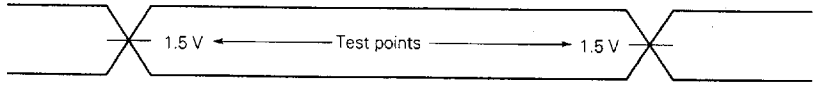
AC Characteristics (Recommended operating conditions unless otherwise noted)

AC Test Conditions

Input waveform (Rise/fall time ≦ 3 ns)



Output waveform



Output load

AC Characteristics directed with the note should be measured with the output load shown in **Fig. 1** or **Fig. 2.**

Fig. 1
(For t_{AA}, t_{ACS}, t_{OE}, t_{OH})

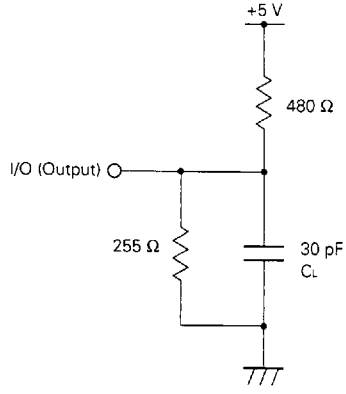
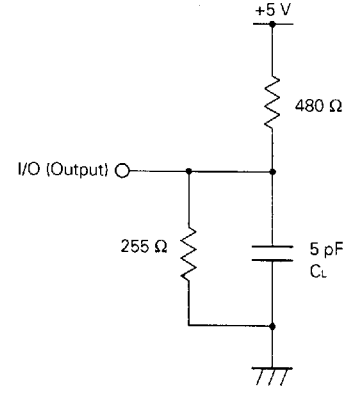


Fig. 2
(For t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ}, t_{OW})



Remark C_L includes capacitances of the probe and jig, and stray capacitances.

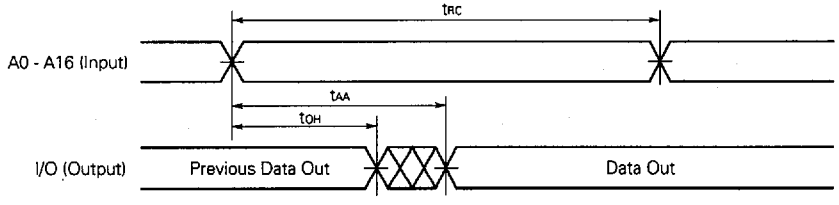
Read Cycle

Parameter	Symbol	μPD431009LE-15		μPD431009LE-17		μPD431009LE-20		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	15		17		20		ns	
Address access time	t_{AA}		15		17		20	ns	Note 1.
$\overline{CS}$ access time	t_{ACS}		15		17		20	ns	
$\overline{OE}$ access time	t_{OE}		8		9		10	ns	
Output hold from address change	t_{OH}	5		5		5		ns	
$\overline{CS}$ to output in low-Z	t_{CLZ}	5		5		5		ns	Note 2.
$\overline{OE}$ to output in low-Z	t_{OLZ}	1		1		1		ns	
$\overline{CS}$ to output in high-Z	t_{CHZ}		7		7		7	ns	
$\overline{OE}$ to output in high-Z	t_{OHZ}		7		7		7	ns	

Note 1. See the output load shown in **Fig. 1.**

2. See the output load shown in **Fig. 2.**

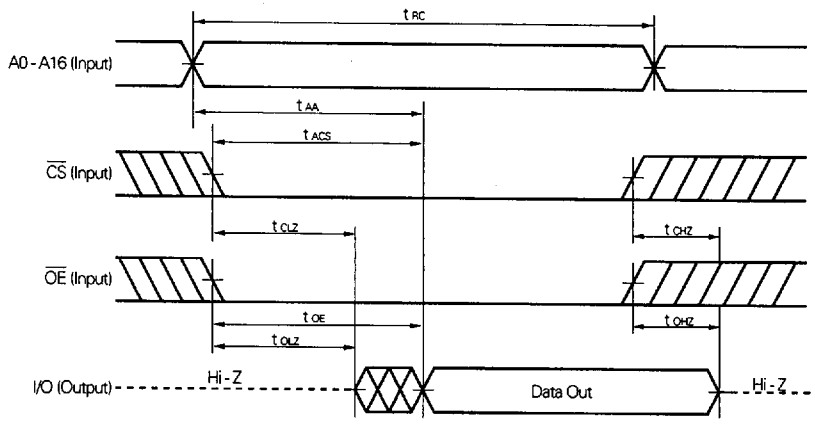
Read Cycle Timing Chart 1 (Address Access)



Remark 1. In read cycle, $\overline{WE}$ should be fixed to high level.

2. $\overline{CS} = \overline{OE} = V_{IL}$

Read Cycle Timing Chart 2 ($\overline{CS}$ Access)



Caution Address valid prior to or coincident with $\overline{CS}$ low level input.

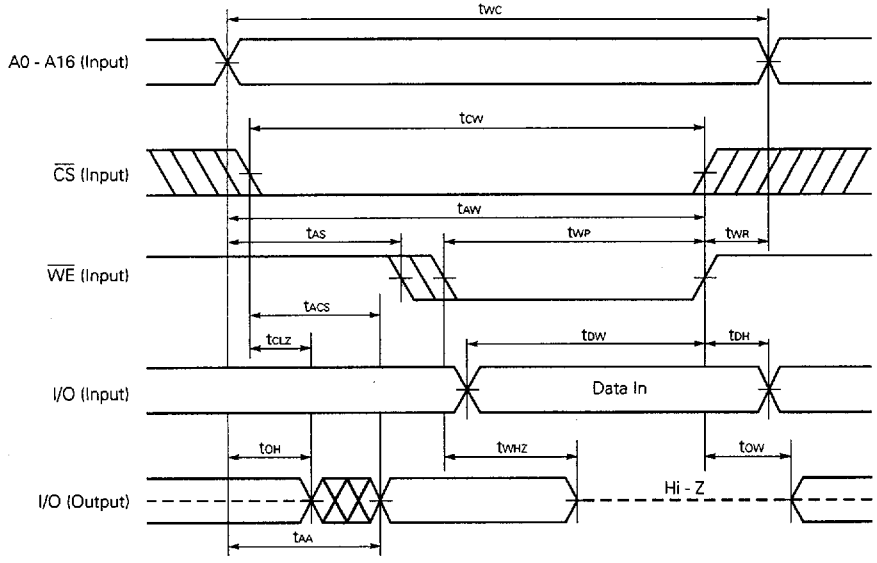
Remark In read cycle, $\overline{WE}$ should be fixed to high level.

Write Cycle

Parameter	Symbol	μPD431009LE-15		μPD431009LE-17		μPD431009LE-20		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	15		17		20		ns	
$\overline{CS}$ to end of write	t_{CW}	10		11		12		ns	
Address valid to end of write	t_{AW}	9		11		12		ns	
Write pulse width	t_{WP}	9		10		10		ns	
Data valid to end of write	t_{DW}	8		9		10		ns	
Data hold time	t_{DH}	0		0		0		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write recovery time	t_{WR}	0		0		0		ns	
$\overline{WE}$ to output in high-Z	t_{WHZ}		7		7		7	ns	Note
Output active from end of write	t_{OW}	3		3		3		ns	

Note See the output load shown in **Fig. 2.**

Write Cycle Timing Chart 1 ($\overline{WE}$ Controlled)



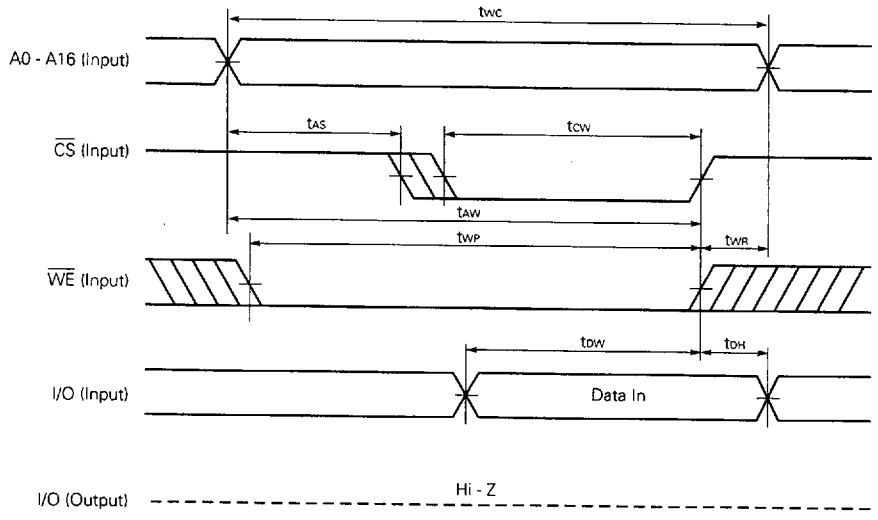
Caution $\overline{CS}$ or $\overline{WE}$ should be fixed to high level during address transition.

Remark 1. Write operation is done during the overlap time of a low level $\overline{CS}$ and a low level $\overline{WE}$.

2. During t_{WHZ}, I/O pins are in the output state, therefore the input signals of opposite phase to the output must not be applied.

3. When $\overline{WE}$ is at low level, the output state is always Hi-Z. When $\overline{WE}$ is at high level, read operation is executed. Therefore $\overline{OE}$ should be at high level to make the output state Hi-Z.

Write Cycle Timing Chart 2 ($\overline{CS}$ Controlled)

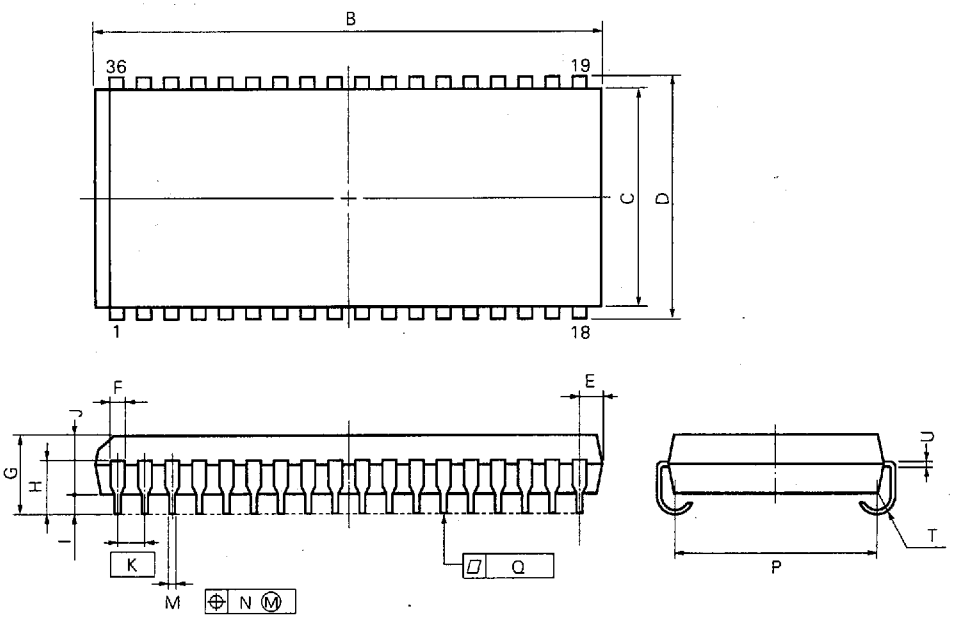


Caution $\overline{CS}$ or $\overline{WE}$ should be fixed to high level during address transition.

Remark Write operation is done during the overlap time of a low level $\overline{CS}$ and a low level $\overline{WE}$.

Package Drawing

36 PIN PLASTIC SOJ (400 mil)



P36LE-400A

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	23.6±0.2	0.929±0.008
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.005 ± 0.1	$0.040^{+0.004}_{-0.005}$
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.1	0.004
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

RECOMMENDED SOLDERING CONDITIONS

Please consult with our sales offices for soldering conditions of the μPD431009.

TYPE OF SURFACE MOUNT DEVICE

μPD431009LE: 36-pin plastic SOJ (400 mil)