

**1M-BIT CMOS FAST STATIC RAM
64K-WORD BY 16-BIT**

Description

The μ PD431016 is a high speed, low power, 1 048 576 bits (65 536 words by 16 bits) CMOS static RAM.
The μ PD431016 are packed in 44-pin plastic SOJ.

Feature

- 65 536 words by 16 bits organization
- Fast access time 15, 17, 20 ns (MAX.)
- Output buffers control: $\overline{OE}$
- Byte data control: $\overline{LB}$ (I/O1 to I/O8), $\overline{UB}$ (I/O9 to I/O16)
- Common I/O using three state output
- Fully static operation: no clock or refreshing to operate
- TTL compatible: all inputs and outputs
- Single +5 V power supply

Ordering Information

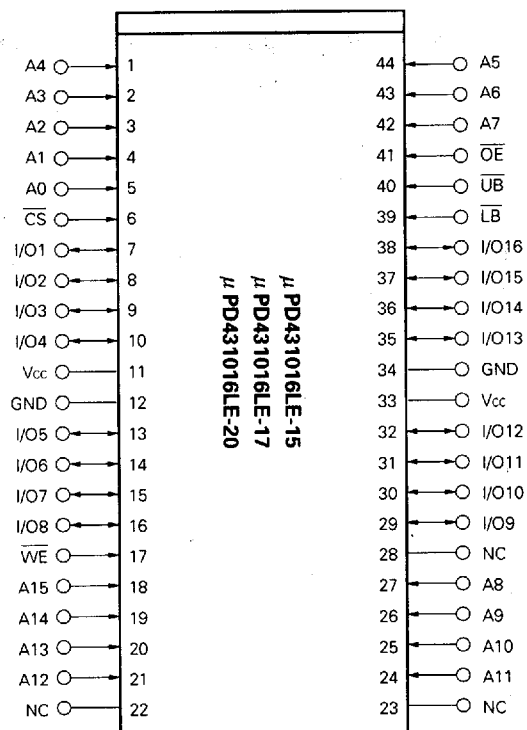
Part number	Package	Access time ns (MAX.)	Operating supply current mA (MAX.)	Standby supply current mA (MAX.)	Quality grade
μ PD431016LE-15	44-pin plastic SOJ (400 mil)	15	240	10	Standard
μ PD431016LE-17		17	230		
μ PD431016LE-20		20	220		

Remark Operating supply current is 180 mA (MAX.) when this product is used at 50 ns cycle time.

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

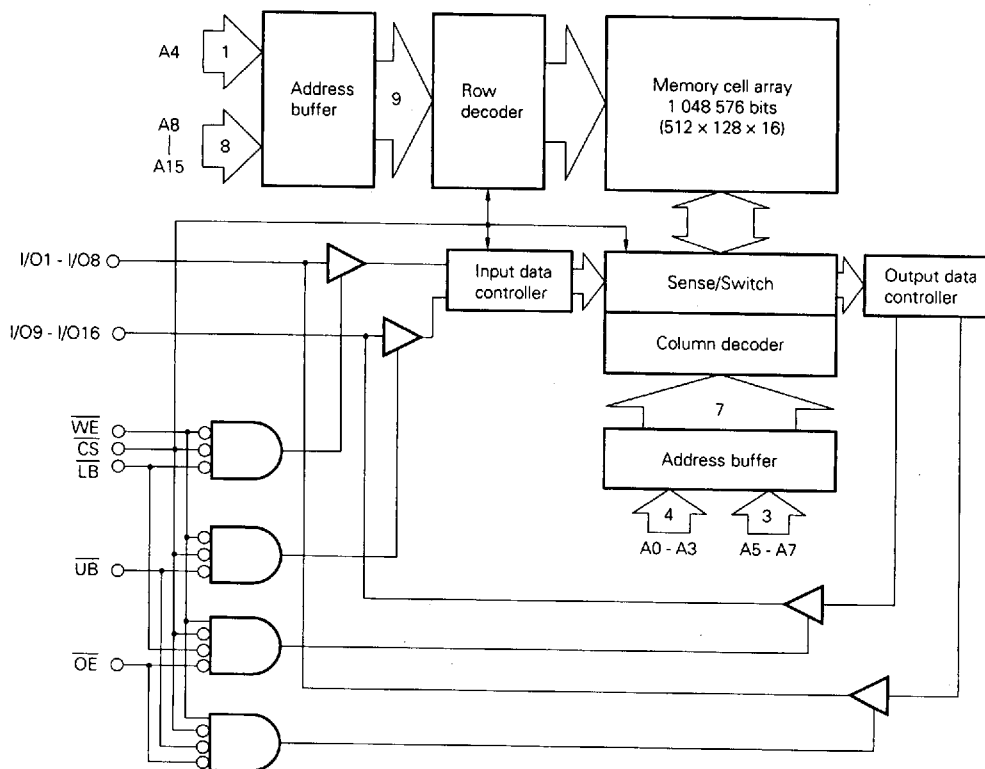
Pin Configuration (Marking Side)

44-Pin Plastic SOJ (400 mil)



A0 to A15 : Address Inputs
I/O1 to I/O16 : Data Inputs/Outputs
 $\overline{CS}$: Chip Select
 $\overline{WE}$: Write Enable
 $\overline{OE}$: Output Enable
 $\overline{LB}$, $\overline{UB}$: Byte data select
Vcc : Power supply
GND : Ground
NC : No Connection

Block Diagram



Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O		Supply current
						I/O1 - I/O8	I/O9 - I/O16	
H	X	X	X	X	Not selected	Hi-Z	Hi-Z	I_{sb}
L	L	H	L	L	Read	D _{OUT}	D _{OUT}	I_{cc}
			L	H		D _{OUT}	Hi-Z	
			H	L		Hi-Z	D _{OUT}	
L	X	L	L	L	Write	D _{IN}	D _{IN}	
			L	H		D _{IN}	Hi-Z	
			H	L		Hi-Z	D _{IN}	
L	H	H	X	X	Output disable	Hi-Z	Hi-Z	
L	X	X	H	H		Hi-Z	Hi-Z	

Remark X : Don't care

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 ^{Note} to +7.0	V
Input/Output voltage	V _I	-0.5 ^{Note} to V _{CC} +0.5	V
Operating temperature	T _{opt}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +125	°C

Note -3.0 V (MIN.) (Pulse width: 10 ns)

Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
High level input voltage	V _{IH}	2.2		V _{CC} +0.5	V
Low level input voltage	V _{IL}	-0.5 ^{Note}		+0.8	V
Ambient temperature	T _a	0		+70	°C

Note -3.0 V (MIN.) (Pulse width: 10 ns)

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input leakage current	I _{LI}	V _{IN} = 0 V to V _{CC}	-2		+2	μA
Output leakage current	I _{LO}	V _{I/O} = 0 V to V _{CC} , $\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{LB} = V_{IH}$ or $\overline{UB} = V_{IH}$	-2		+2	μA
Operating supply current	I _{CC}	$\overline{CS} = V_{IL}$, I _{I/O} = 0 mA	Cycle time: 15 ns		240	mA
			Cycle time: 17 ns		230	
			Cycle time: 20 ns		220	
			Cycle time: 50 ns		180	
Standby supply current	I _{SB}	$\overline{CS} = V_{IH}$, V _{IN} = V _{IH} or V _{IL}			30	mA
	I _{SB1}	V _{CC} - 0.2 V ≤ $\overline{CS}$, V _{IN} ≤ 0.2 V or V _{CC} - 0.2 V ≤ V _{IN}			10	
High level output voltage	V _{OH}	I _{OH} = -4.0 mA	2.4			V
Low level output voltage	V _{OL}	I _{OL} = 8 mA			0.4	V

Remark V_{IN}: Input voltage

Capacitance (T_a = +25 °C, f = 1 MHz)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C _{IN}	V _{IN} = 0 V			6	pF
Input/Output capacitance	C _{I/O}	V _{I/O} = 0 V			8	pF

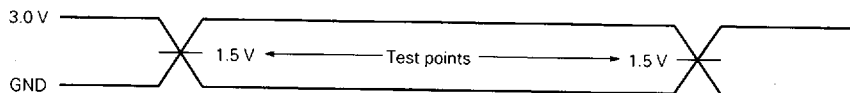
Remark 1. V_{IN}: Input voltage

2. These parameters are periodically sampled and not 100 % tested.

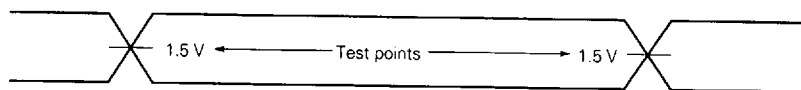
AC Characteristics (Recommended operating conditions unless otherwise noted)

AC Test Conditions

Input waveform (Rise/fall time ≤ 3 ns)



Output waveform



Output load

AC Characteristics directed with the note should be measured with the output load shown in Fig. 1 or Fig. 2.

Fig. 1

(For tAA, tACS, tOE, tADB, tOH)

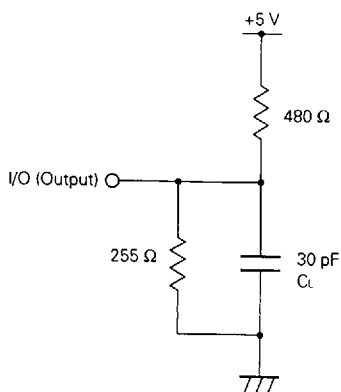
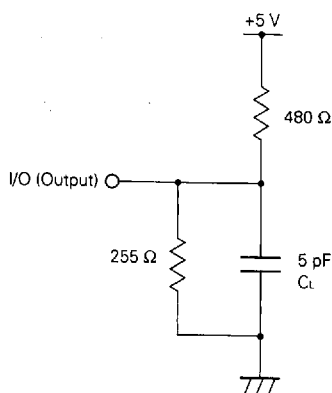


Fig. 2

(For tCLZ, tOLZ, tBLZ, tCHZ, tBHZ, tWHZ, tOW)



Remark CL includes capacitances of the probe and jig, and stray capacitances.

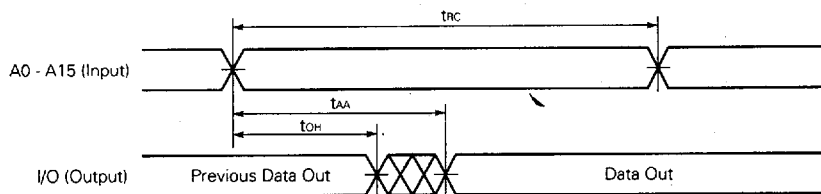
Read Cycle

Parameter	Symbol	μ PD431016LE-15		μ PD431016LE-17		μ PD431016LE-20		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	15		17		20		ns	
Address access time	t_{AA}		15		17		20	ns	Note 1.
$\overline{CS}$ access time	t_{ACS}		15		17		20	ns	
$\overline{OE}$ access time	t_{OE}		8		9		10	ns	
$\overline{LB}$, $\overline{UB}$ access time	t_{ABD}		8		9		10	ns	
Output hold from address change	t_{OH}	5		5		5		ns	
$\overline{CS}$ to output in low-Z	t_{CLZ}	5		5		5		ns	Note 2.
$\overline{OE}$ to output in low-Z	t_{OLZ}	1		1		1		ns	
$\overline{LB}$, $\overline{UB}$ to output in low-Z	t_{BLZ}	1		1		1		ns	
$\overline{CS}$ to output in high-Z	t_{CHZ}		7		7		7	ns	
$\overline{OE}$ to output hold in high-Z	t_{OHZ}		7		7		7	ns	
$\overline{LB}$, $\overline{UB}$ to output hold in high-Z	t_{BHZ}		7		7		7	ns	

Note 1. See the output load shown in Fig. 1.

2. See the output load shown in Fig. 2.

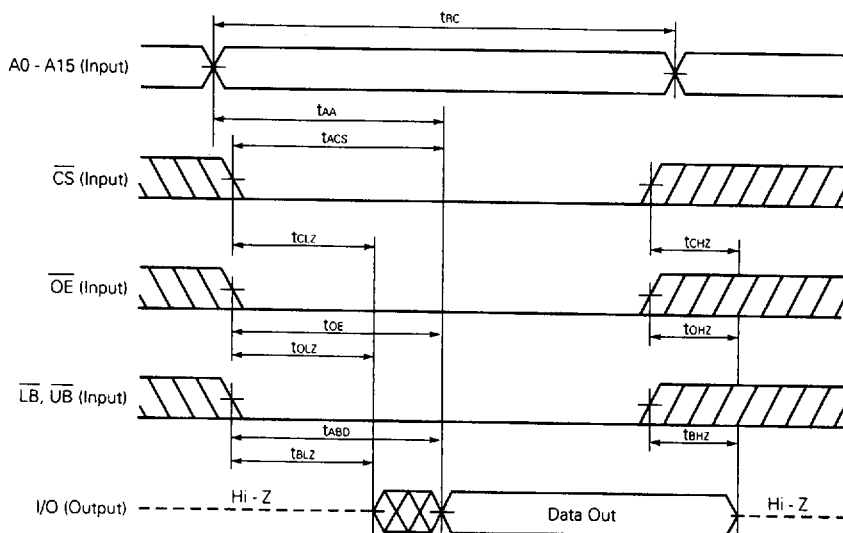
Read Cycle Timing Chart 1 (Address Access)



Remark 1. In read cycle, $\overline{WE}$ should be fixed to high level.

2. $\overline{CS} = \overline{OE} = \overline{LB}$ (or $\overline{UB}$) = V_{IL}

Read Cycle Timing Chart 2 ($\overline{\text{CS}}$ Access)



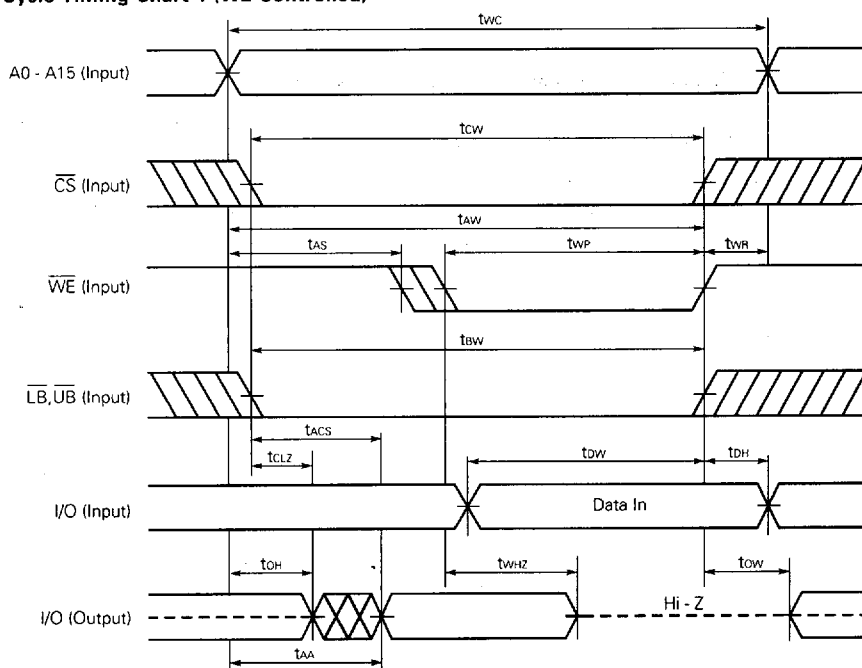
Caution Address valid prior to or coincident with $\overline{\text{CS}}$ low level input.

Remark In read cycle, $\overline{\text{WE}}$ should be fixed to high level.

Write Cycle

Parameter	Symbol	μ PD431016LE-15		μ PD431016LE-17		μ PD431016LE-20		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t _{wc}	15		17		20		ns	
$\overline{\text{CS}}$ to end of write	t _{cw}	10		11		12		ns	
Address valid to end of write	t _{aw}	9		11		12		ns	
Write pulse width	t _{wp}	9		10		10		ns	
$\overline{\text{LB}}, \overline{\text{UB}}$ to end of write	t _{bw}	9		11		12		ns	
Data valid to end of write	t _{dww}	8		9		10		ns	
Data hold time	t _{dH}	0		0		0		ns	
Address setup time	t _{as}	0		0		0		ns	
Write recovery time	t _{wr}	0		0		0		ns	
$\overline{\text{WE}}$ to output in high-Z	t _{whz}		7		7		7	ns	Note
Output active from end of write	t _{ow}	3		3		3		ns	

Note See the output load shown in Fig. 2.

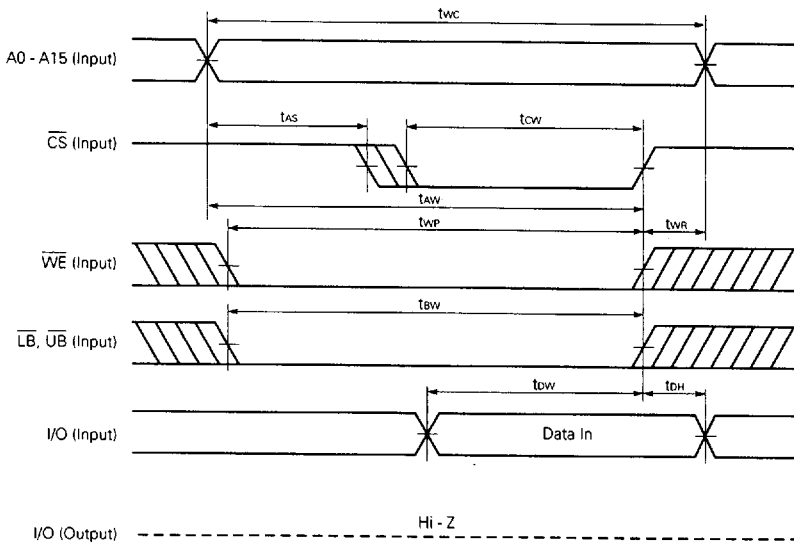
Write Cycle Timing Chart 1 ($\overline{\text{WE}}$ Controlled)

Caution $\overline{\text{CS}}$ or $\overline{\text{WE}}$ should be fixed to high level during address transition.

Remark 1. Write operation is done during the overlap time of low level $\overline{\text{CS}}$, low level $\overline{\text{WE}}$ and low level $\overline{\text{LB}}$ (or low level $\overline{\text{UB}}$).

- During t_{whz}, I/O pins are in the output state, therefore the input signals of opposite phase to the output must not be applied.
- When $\overline{\text{WE}}$ is at low level, the I/O pins are always Hi-Z. When $\overline{\text{WE}}$ is at high level, read operation is executed. Therefore $\overline{\text{OE}}$ should be at high level to make the I/O pins Hi-Z.

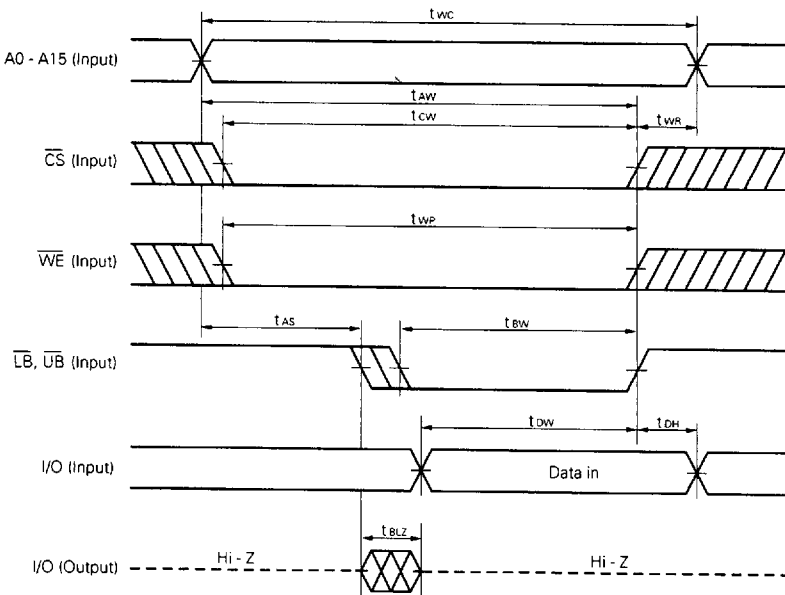
Write Cycle Timing Chart 2 ($\overline{CS}$ Controlled)



Caution $\overline{CS}$ or $\overline{WE}$ should be fixed to high level during address transition.

Remark Write operation is done during the overlap time of a low level $\overline{CS}$, low level $\overline{WE}$ and low level $\overline{LB}$ (or low level $\overline{UB}$).

Write Cycle Timing Chart 3 ($\overline{LB}, \overline{UB}$ Controlled)

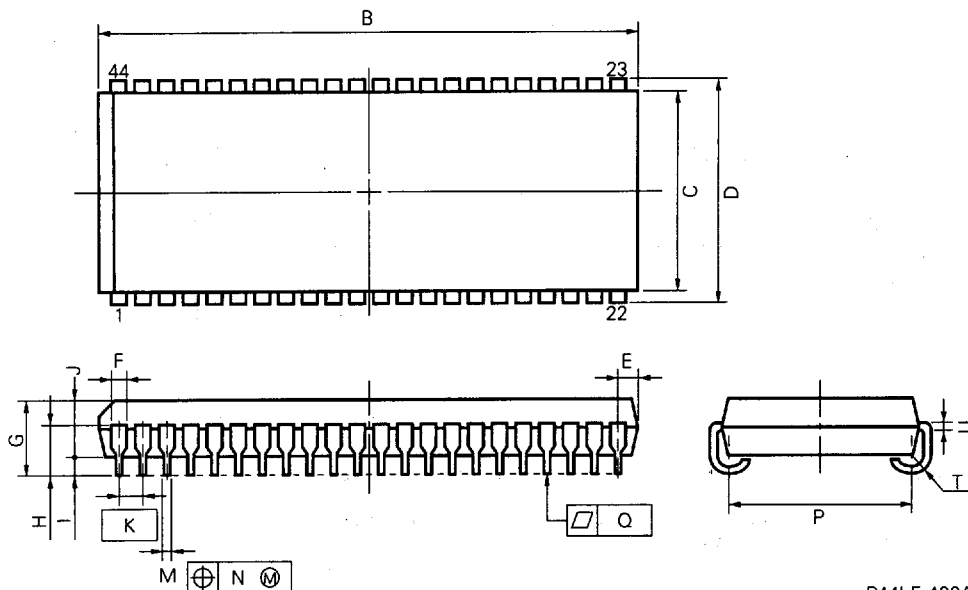


Caution $\overline{CS}$ or $\overline{WE}$ should be fixed to high level during address transition.

Remark Write operation is done during the overlap time of a low level $\overline{CS}$, low level $\overline{WE}$ and low level $\overline{LB}$ (or low level $\overline{UB}$).

Package Drawing

44 PIN PLASTIC SOJ (400 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P44LE-400A

ITEM	MILLIMETERS	INCHES
B	28.73 ^{+0.2} _{-0.35}	1.131 ^{+0.008} _{-0.014}
C	10.16	0.400
D	11.18±0.20	0.440±0.008
E	1.03±0.15	0.041 ^{+0.006} _{-0.007}
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.3±0.2	0.091 ^{+0.008} _{-0.009}
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.10	0.004
T	R 0.85	R 0.033
U	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}

RECOMMENDED SOLDERING CONDITIONS

Please consult with our sales offices for soldering conditions of the μ PD431016.

TYPE OF SURFACE MOUNT DEVICE

μ PD431016LE: 44-pin plastic SOJ (400 mil)