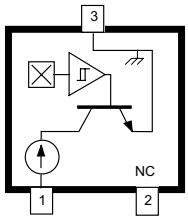
Preliminary Data Sheet
Subject to Change Without Notice
August 9, 2004

A1185 and A1186

Ultrasensitive Two-Wire Field-Programmable Chopper-Stabilized Unipolar Hall-Effect Switches

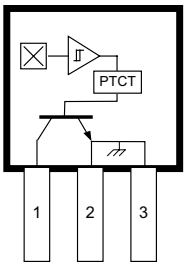
Package LH, 3-pin SOT

1. VCC
2. No connection
3. GND



Package UA, 3-pin SIP

1. VCC
2. GND
3. GND



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	**28 V**
Reverse-Supply Voltage, V_{RCC}	**–18 V**
Magnetic Flux Density, B	**Unlimited**
Operating Temperature	
Ambient, T_A, Range E	**–40°C to 85°C**
Ambient, T_A, Range L	**–40°C to 150°C**
Maximum Junction, $T_{J(max)}$	**165°C**
Storage Temperature, T_S	**–65°C to 170°C**

The A1185 and A1186 devices are ultrasensitive, two-wire, unipolar, Hall effect switches. The operate point, B_{OP}, can be field-programmed, after final packaging of the sensor and placement into the application. This advanced feature allows the optimization of the sensor switching performance, by effectively accounting for variations caused by mounting tolerances for the device and the target magnet.

This family of devices are produced on the Allegro MicroSystems advanced BiCMOS wafer fabrication process, which implements a patented, high-frequency, chopper-stabilization technique that achieves magnetic stability and eliminates the offsets that are inherent in single-element devices exposed to harsh application environments. Commonly found in a number of automotive applications, the A1185 and A1186 devices are utilized to sense: seat track position, seat belt buckle presence, hood/trunk latching, and shift selector position.

Two-wire unipolar switches are particularly advantageous in price-sensitive applications, because they require one less wire than the more traditional open-collector output switches. Additionally, the system designer gains inherent diagnostics because output current normally flows in either of two narrowly-specified ranges. Any output current level outside of these two ranges is a fault condition. The A1185 and A1186 devices also features on-chip transient protection, and a Zener clamp to protect against overvoltage conditions on the supply line.

The output current of the A1186 switches HIGH in the presence of a south polarity magnetic field of sufficient strength; and switches LOW otherwise, including when there is no significant magnetic field present. The A1185 has an inverted output current level: switching LOW in the presence of a south polarity magnetic field of sufficient strength, and HIGH otherwise.

All family members are offered in two package styles: SOT-23W, a miniature low-profile package for surface-mount applications (suffix *–LH*), and TO-92, three-lead ultra-mini Single Inline Package (SIP) for through-hole mounting (suffix *–UA*).

Factory-programmed versions are also available. Refer to: A1145 and A1146.

Features and Benefits

- Chopper stabilization
  - Low switchpoint drift over operating temperature range
  - Low stress sensitivity
- Field-programmable for optimized switchpoints
- On-chip protection
  - Supply transient protection
  - Reverse-battery protection
  - On-board voltage regulator
  - 3.5 V to 24 V operation

Engineering samples available on a limited basis. Contact your local sales or applications support office for additional information.

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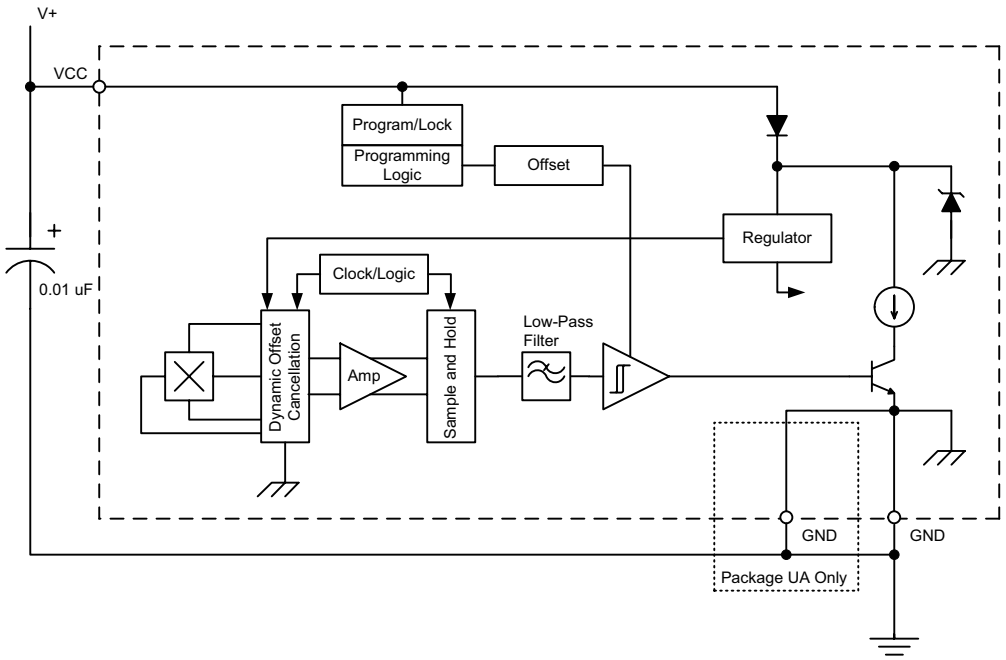
Functional Block Diagram



Product Selection Guide

Use the complete part numbers when ordering

Part Number	Package	T_A (°C)	Supply Current at Low Output, $I_{CC(L)}$ (mA)	Output	
				South (+) Field[1]	Other Field[2]
A1185ELH A1185EUA	Surface Mount SIP	–40 to 85	5 to 6.9	Low	High
A1185LLH A1185LUA	Surface Mount SIP	–40 to 150			
A1186ELH A1186EUA	Surface Mount SIP	–40 to 85	5 to 6.9	High	Low
A1186LLH A1186LUA	Surface Mount SIP	–40 to 150			

[1]South (+) magnetic fields must be of sufficient strength.

[2]Includes north (–) magnetic fields of sufficient strength, and weak fields of either polarity.

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ELECTRICAL CHARACTERISTICS over the operating voltage and temperature range, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{CC}	Device powered on	3.5	–	24	V
Supply Current[1]	$I_{CC(L)}$	B >B_{OP} for A1185; B <B_{RP} for A1186	5	–	6.9	mA
	$I_{CC(H)}$	B >B_{OP} for A1186; B <B_{RP} for A1185	12	–	17	mA
Zener Clamp Supply Voltage	$V_{Z(supply)}$	I_{CC} = $I_{CC(max)}$ + 3 mA; T_A = 25°C	28	–	40	V
Zener Clamp Supply Current[2]	$I_{Z(supply)}$	$V_{Z(supply)}$ = 28 V	–	–	10	mA
Output Slew Rate[3]	di/dt	No bypass capacitor; capacitance of the oscilloscope performing the measurement = 20 pF	–	36	–	mA/µs
Chopping Frequency	f_C		–	400	–	kHz
Power-On Time[4]	t_{on}	After factory trimming; with and without bypass capacitor (C_{BYP} = 0.01 µF)	–	–	25	µs
Power-On State[5]	POS	t_{on} ≤ $t_{on(max)}$; V_{CC} slew rate ≥ 25 mV/µs	–	HIGH	–	–

[1]Relative values of B use the algebraic convention, where positive values indicate south magnetic polarity, and negative values indicate north magnetic polarity; therefore greater B values indicate a stronger south polarity field (or a weaker north polarity field, if present).
[2]The maximum value for $I_{Z(supply)}$ is equal to $I_{CC(L)MAX}$ + 3 mA.
[3]The value of di is the difference between 90% of $I_{CC(H)}$ and 10% of $I_{CC(L)}$, and the value of dt is time period between those two points. The value of di/dt depends on the value of the bypass capacitor, if one is used, with greater capacitances resulting in lower rates of change.
[4]The value of t_{on} depends on the value of the bypass capacitor, if one is used, with greater capacitances resulting in longer t_{on}.
[5]A V_{CC} slew rate less than 25 mV/µs affects device performance, both while powering-on and while running. For t_{on} > $t_{on(max)}$, and B_{RP} < B < B_{OP}, POS is undefined.

MAGNETIC CHARACTERISTICS[1] over the operating voltage and temperature range, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Programmable Operate Point Range	$B_{OPrange}$	I_{CC} = $I_{CC(L)}$ for A1185 I_{CC} = $I_{CC(H)}$ for A1186	10	–	60	G
Switchpoint Step Size	B_{RES}	V_{CC} = 5 V, T_A = 25°C	2	4	6	G
Number of Programming Bits	–	Switchpoint setting	–	5	–	Bit
		Programming locking	–	1	–	Bit
Termperature Drift of B_{OP}	ΔB_{OP}		–	–	±20	G
Hysteresis	B_{HYS}	B_{HYS} = B_{OP} – B_{RP}	5	15	30	G

[1]Relative values of B use the algebraic convention, where positive values indicate south magnetic polarity, and negative values indicate north magnetic polarity; therefore greater B values indicate a stronger south polarity field (or a weaker north polarity field, if present).
[2]The range of values specified for B_{RES} is a maximum, derived from the cumulative programming bit errors.

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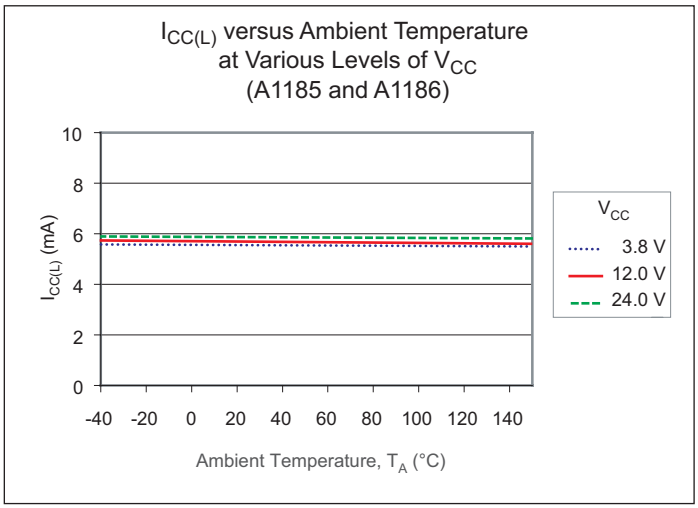
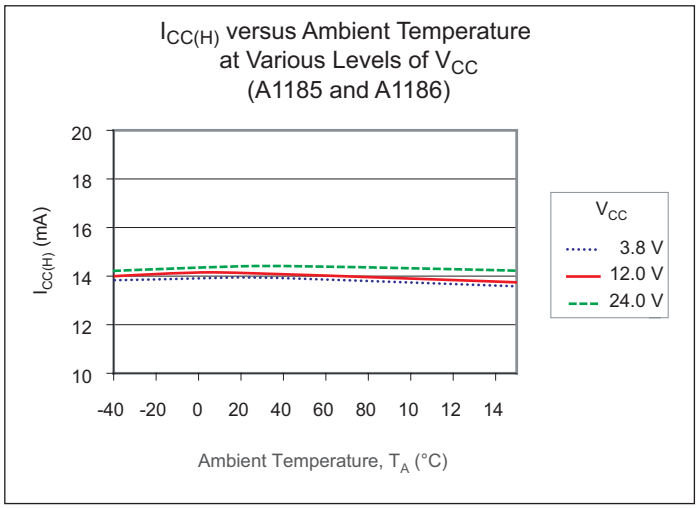
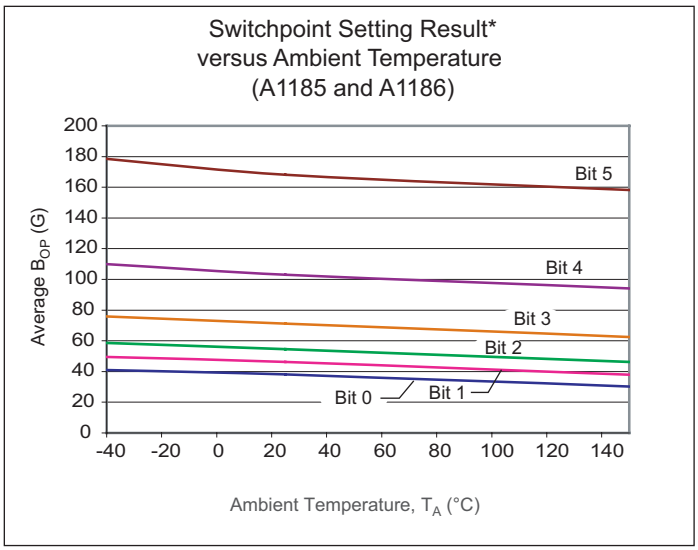
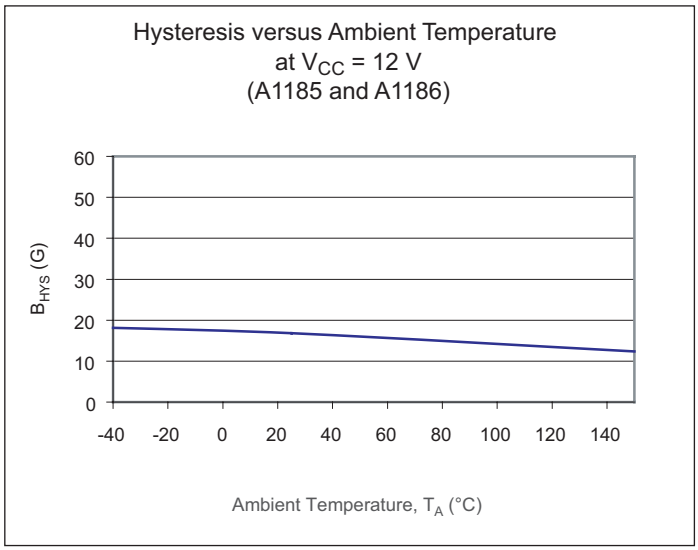
Characteristic Data









* Factory default setting is Bit 0.

Device Qualification Program

Contact Allegro MicroSystems for information.

EMC (Electromagnetic Compatibility) Requirements

Contact your local representative for EMC results.

Test Name	Reference Specification
ESD – Human Body Model	AEC-Q100-002
ESD – Machine Model	AEC-Q100-003
Conducted Transients	ISO 7637-1
Direct RF Injection	ISO 11852-7
Bulk Current Injection	ISO 11852-4
TEM Cell	ISO 11852-3

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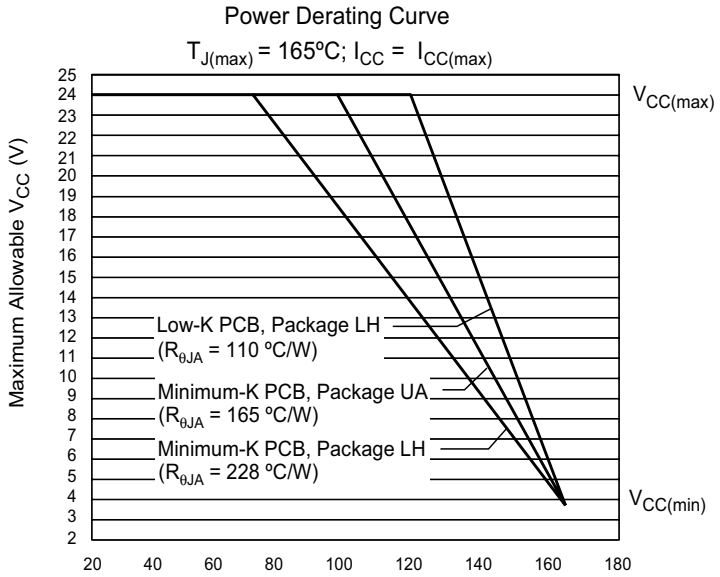
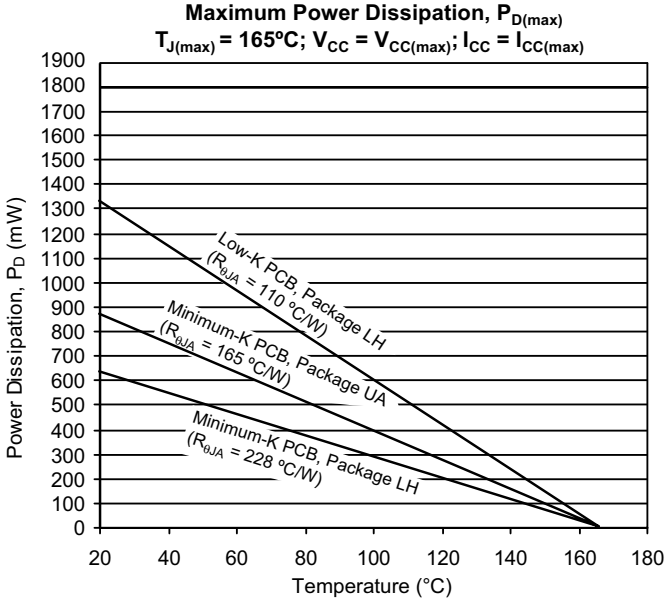
THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max	Units
Package Thermal Resistance	$R_{\theta JA}$	Package LH, minimum-K PCB (single-sided with copper limited to solder pads)	110	–	–	ºC/W
		Package LH, low-K PCB (double-sided with 0.926 in^2 copper area)	228	–	–	ºC/W
		Package UA, minimum-K PCB (single-sided with copper limited to solder pads)	165	–	–	ºC/W





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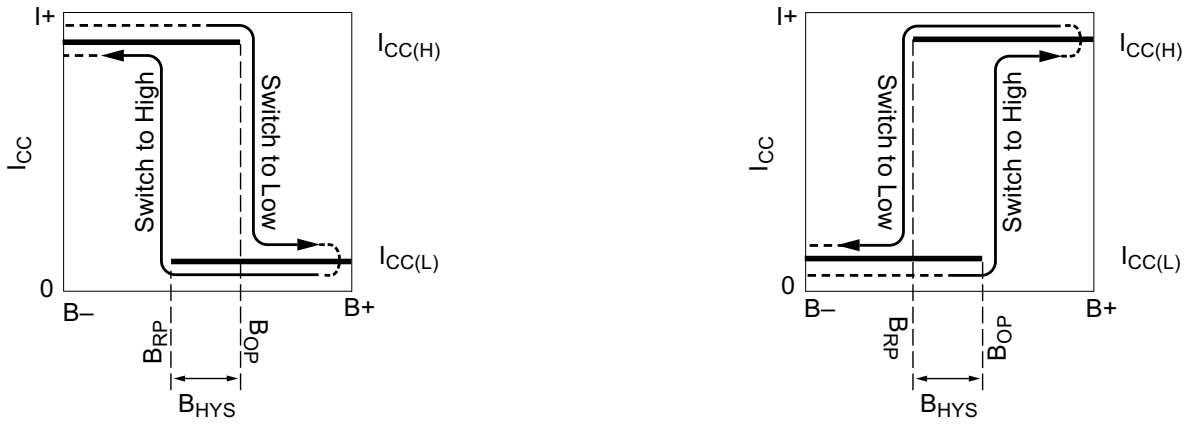
Functional Description

Operation

The output, I_{CC}, of the A1185 switches low after the magnetic field at the Hall sensor exceeds the operate point threshold, B_{OP}. When the magnetic field is reduced to below the release point threshold, B_{RP}, the device output goes high. The differences between the magnetic operate and release point is called the hysteresis of the device, B_{HYS}. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise. The A1186 device switches with opposite polarity for similar B_{OP} and B_{RP} values, in comparison to the A1185 (see figure 1).



(A) A1185 (B) A1186

Figure 1. Alternative switching behaviors are available in the A118x device family. On the horizontal axis, the B+ direction indicates increasing south polarity magnetic field strength, and the B– direction indicates decreasing south polarity field strength (including the case of increasing north polarity).

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Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switch-point accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall sensor. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges.

Chopper stabilization is a unique approach used to minimize Hall offset on the chip. The patented Allegro technique, namely dynamic quadrature offset cancellation, removes key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at baseband, while the dc offset becomes a high-frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated dc offset is suppressed.

The chopper stabilization technique uses a 200 kHz high frequency clock. The chopping occurs on each clock edge, resulting in a 400 kHz chop frequency. This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling.

This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits. This process is illustrated in figure 2.

The repeatability of magnetic field-induced switching is affected slightly by a chopper technique. However, the Allegro high-frequency chopping approach minimizes the affect of jitter and makes it imperceptible in most applications. Applications that are more likely to be sensitive to such degradation are those requiring precise sensing of alternating magnetic fields; for example, speed sensing of ring-magnet targets. For such applications, Allegro recommends its digital sensor families with lower sensitivity to jitter. For more information on those devices, contact your Allegro sales representative.

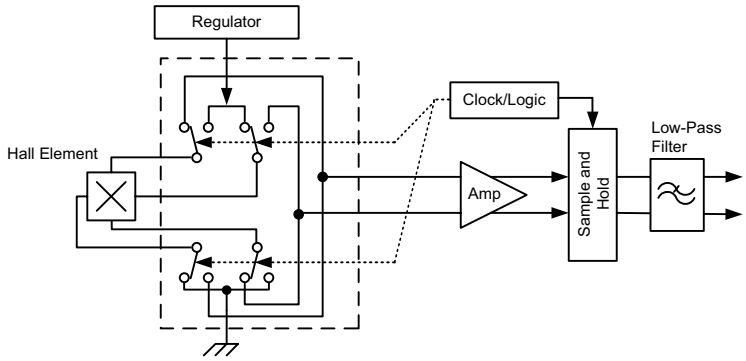

Figure 2. Chopper stabilization circuit (dynamic quadrature offset cancellation)

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Application Information

For additional general application information, visit the Allegro MicroSystems Web site at www. allegromicro.com.

Typical Application Circuit

The A118x family of devices must be protected by an external bypass capacitor, C_{BYP}, connected between the supply, VCC, and the ground, GND, of the device. C_{BYP} reduces both external noise and the noise generated by the chopper-stabilization function. As shown in figure 3, a 0.01 µF capacitor is typical.

Installation of C_{BYP} must ensure that the traces that connect it to the A118x pins are no greater than 5 mm in length.

All high-frequency interferences conducted along the supply lines are passed directly to the load through C_{BYP}, and it serves only to protect the A118x internal circuitry. As a result, the load ECU (electronic control unit) must have sufficient protection, other than C_{BYP}, installed in parallel with the A118x.

A series resistor on the supply side, R_S (not shown), in combination with C_{BYP}, creates a filter for EMI pulses. (Additional information on EMC is provided on the Allegro MicroSystems Web site.)

When determining the minimum V_{CC} requirement of the A118x device, the voltage drops across R_S and the ECU sense resistor, R_{SENSE}, must be taken into consideration. The typical value for R_{SENSE} is approximately 100 Ω.

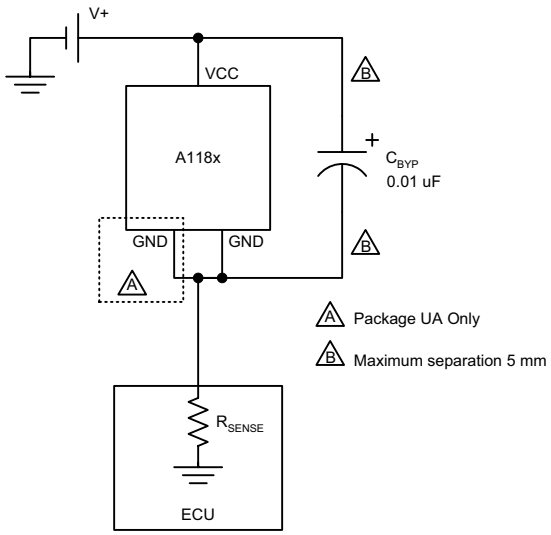

Figure 3. Typical application circuit

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Power Derating

The device must be operated below the maximum junction temperature of the device, $T_{J(max)}$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems Web site.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \qquad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \qquad (2)$$

$$T_J = T_A + \Delta T \qquad (3)$$

For example, given common conditions such as: T_A= 25°C, V_{CC} = 12 V, I_{CC} = 4 mA, and $R_{\theta JA}$ = 140 °C/W, then:

$$P_D = V_{CC} \times I_{CC} = 12\ V \times 4\ mA = 48\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 48\ mW \times 140\ °C/W = 7°C$$

$$T_J = T_A + \Delta T = 25°C + 7°C = 32°C$$

A worst-case estimate, $P_{D(max)}$, represents the maximum allowable power level ($V_{CC(max)}$, $I_{CC(max)}$), without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at T_A=150°C, package UA, using minimum-K PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$=165°C/W, $T_{J(max)}$=165°C, $V_{CC(max)}$= 24 V, and $I_{CC(max)}$ = 17 mA.

Calculate the maximum allowable power level, $P_{D(max)}$. First, invert equation 3:

$$\Delta T_{max} = T_{J(max)} - T_A = 165\,°C - 150\,°C = 15\,°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15°C \div 165\ °C/W = 91\ mW$$

Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_{D(max)} \div I_{CC(max)} = 91\ mW \div 17\ mA = 5\ V$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages ≤$V_{CC(est)}$.

Compare $V_{CC(est)}$ to $V_{CC(max)}$. If $V_{CC(est)} \leq V_{CC(max)}$, then reliable operation between $V_{CC(est)}$ and $V_{CC(max)}$ requires enhanced $R_{\theta JA}$. If $V_{CC(est)} \geq V_{CC(max)}$, then operation between $V_{CC(est)}$ and $V_{CC(max)}$ is reliable under these conditions.

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Programming Protocol

The magnetic operate point, B_{OP}, is adjustable using 5 bits, allowing 31 addresses. The 31 addresses correspond to increments between $B_{OP(min)}$ and $B_{OP(max)}$, with step sizes corresponding to B_{RES}. Note that the difference between B_{OP} and the magnetic release point, B_{RP}, referred to as the hysteresis, B_{HYS}, is constant and identical for all addresses.

The B_{OP} is programmed by serially addressing the device by digital pulsing through the supply terminal, VCC. Programming is accomplished by permanently blowing fuses in the device. After setting the required fuses, a locking fuse is blown to prevent any further programming of the device. The pulse values are shown in the Programming Protocol Characteristics table and in figure 4.

Additional information on device programming and programming products is available on www. allegromicro.com. Programming hardware is available for purchase, and programming software is available free of charge.

Enabling Addressing Mode. The first segment of code is a keying sequence used to enable the addressing mode. As shown in figure 5, this sequence consists of one VPP pulse, one VPH pulse, and one VPP pulse, with no supply interruptions. This sequence is designed to prevent the device from being programmed accidentally, such as by noise on the supply line.

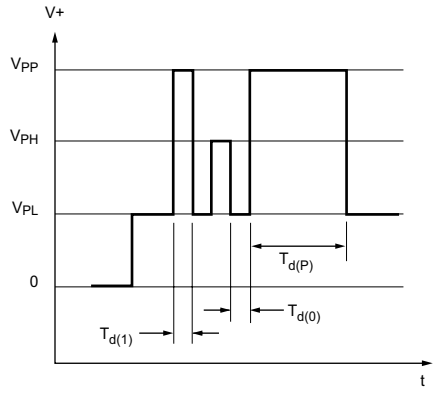

Figure 4. Pulse amplitudes and durations

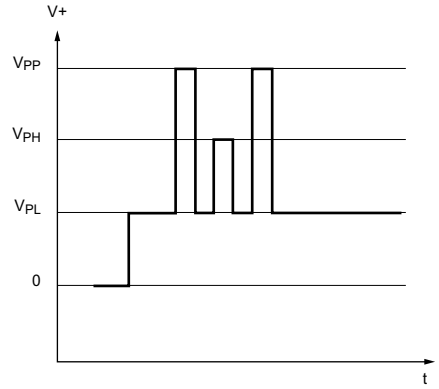

Figure 5. Addressing mode enable pulse sequence

PROGRAMMING PROTOCOL CHARACTERISTICS, over operating temperature range, unless otherwise noted

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Programming Voltage[1]	V_{PL}	Minimum voltage range during programming	4.5	5.0	5.5	V
	V_{PH}		11.5	12.5	13.5	V
	V_{PP}		25.0	26.0	27.0	V
Programming Current[2]	I_{PP}	t_r = 11 µs; 5 V → 26 V; C_{BYP} = 0.1 µF	-	190	-	mA
Pulse Width	$t_{d(0)}$	OFF time between programming bits	20	-	-	µs
	$t_{d(1)}$	Pulse duration for enable and addressing sequences	20	-	-	µs
	$t_{d(P)}$	Pulse duration for fuse blowing	100	300	-	µs
Pulse Rise Time	t_r	0 to V_{PL}; V_{PL} to V_{PH}; V_{PH} to V_{PP}	5	-	20	µs
Pulse Fall Time	t_f	V_{PH} to V_{PL}; V_{PP} to V_{PL}	5	-	100	µs

[1]Programming voltages are measured at the VCC pin.
[2]A bypass capacitor with a minimum capacitance of 0.1 µF must be connected from VCC to the GND pin of the A118x device in order to provide the current necessary to blow the fuse.

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Address Selection. Addresses are set bit by bit, and therefore are expressed in binary notation for programming. For example, with the five bits available for addressing, the fifth address location is expressed as 00101 (binary 5). Of those binary digits, each that is equal to 1 must be set.

In the programming sequence for each digit, an address selection sequence is required to indicate which bit is to be set. As shown in figure 6, an address selection sequence is a series of V_{PH} pulses. The quantity of pulses for a particular binary digit is equal to the decimal value of the binary digit (from 1 to 31 pulses, bits with the value 0 are not set). For example, to set the third binary digit (bit) to 1, four pulses are sent (corresponding to the value of binary 100, which is four in decimal).

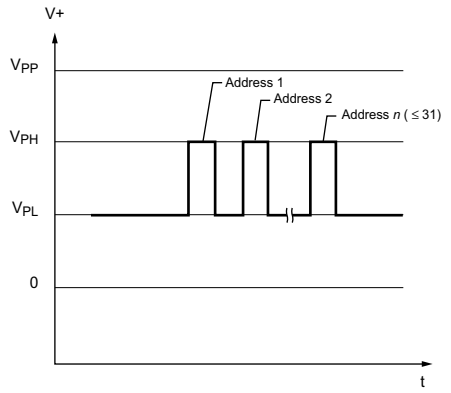

Figure 6. Pulse sequence to select addresses

Code Programming. To program each binary digit in the target address, the following elements are required:

1. an addressing mode enable sequence
2. an address selection sequence
3. a fuse blowing pulse (Note: Blown bit fuses cannot be reset.)

Blowing a bit fuse is accomplished by applying a wide V_{PP} pulse.

Blowing a bit fuse sets that bit to 1. Bits that are not set represent a 0. A sequence for programming address 5 (binary 101) is shown in figure 4. Bit 3 is set to 1 (binary 100, decimal 4) by blowing its fuse, then bit 1 is set to 1 by blowing its fuse. Bit 2 remains 0 because its fuse is left intact.

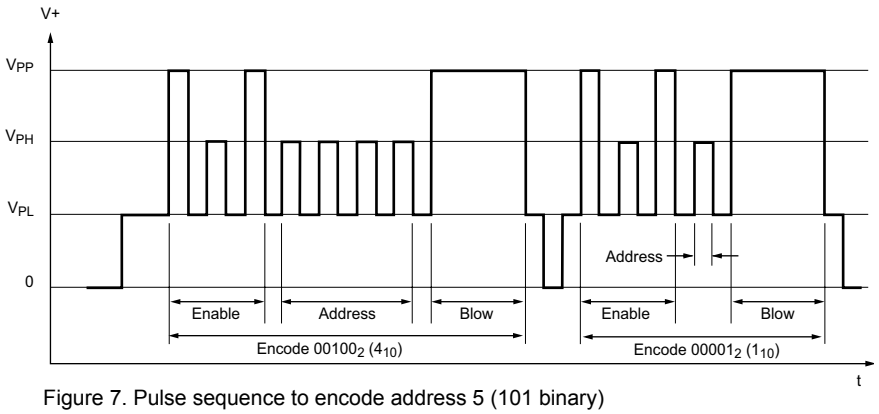

Figure 7. Pulse sequence to encode address 5 (101 binary)

Lock Bit Programming. After the desired B_{OP} address is programmed, the lock bit (address 32) should be encoded (its fuse blown) to prevent further programming of the device. This is done in the same manner as the other address bits, and immediately after the B_{OP} address bits, as shown in figure 8.

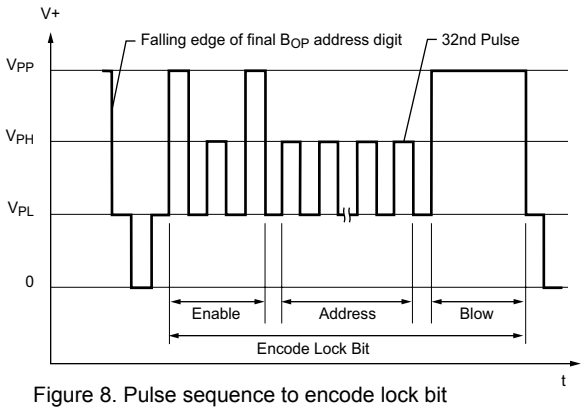

Figure 8. Pulse sequence to encode lock bit

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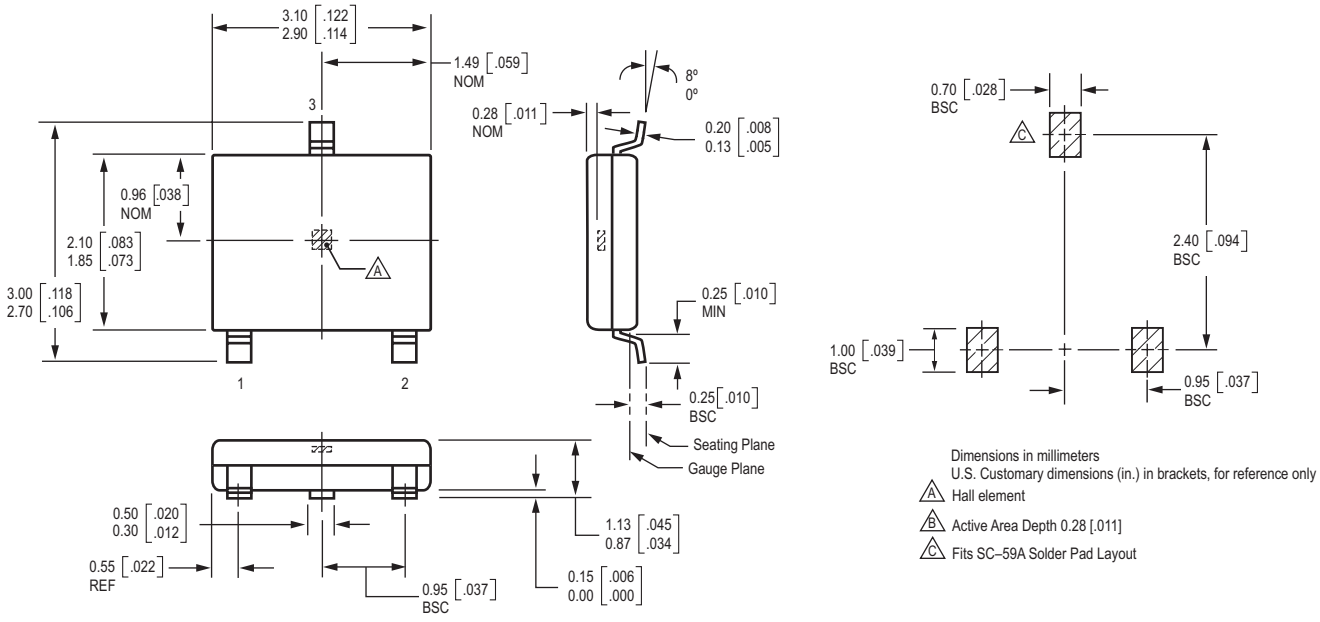
Worcester, Massachusetts 01615-0036 (508) 853-5000
www.allegromicro.com

Package LH, 3-Pin; (SOT-23W)



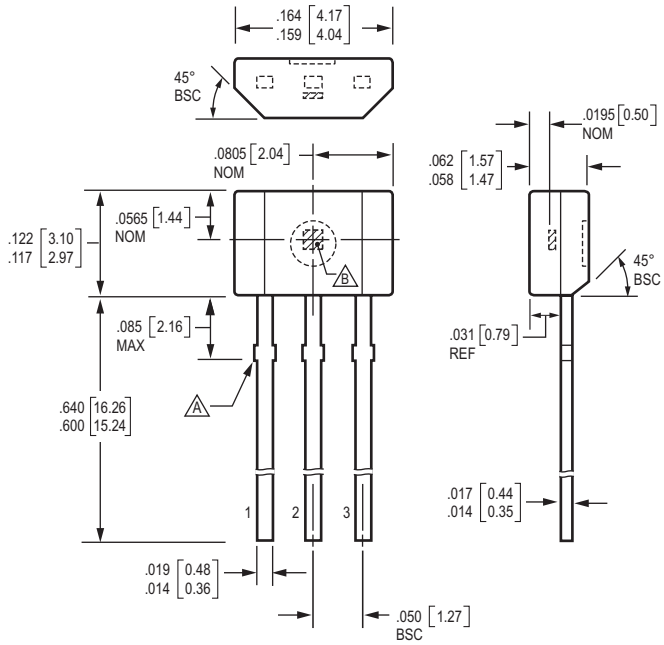
Dimensions in millimeters
U.S. Customary dimensions (in.) in brackets, for reference only

A Hall element

B Active Area Depth 0.28 [.011]

C Fits SC–59A Solder Pad Layout

Package UA, 3-Pin; (TO-92)



Dimensions in inches
Metric dimensions (mm) in brackets, for reference only

A Dambar removal protrusion

B Hall element

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The products described herein are manufactured under one or more of the following U.S. patents: 5,045,920; 5,264,783; 5,442,283; 5,389,889; 5,581,179; 5,517,112; 5,619,137; 5,621,319; 5,650,719; 5,686,894; 5,694,038; 5,729,130; 5,917,320; and other patents pending.

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