DATA SHEET

PCF8548
65 × 102 pixels matrix LCD driver

Product specification
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Philips Semiconductors

PHILIPS

CONTENTS

1 FEATURES

- Single-chip LCD controller/driver
- 65 row and 102 column outputs
- Display data RAM 65 × 102 bits
- On-chip:
  - Configurable 5 (4, 3 and 2) × voltage multiplier generating V_{LCD} (external V_{LCD} also possible)
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible).
- 400 kbits/s fast I^2C-bus interface
- CMOS compatible inputs
- Mux rate: 1 : 65
- Logic supply voltage range V_{DD1} to V_{SS}:
  - 1.9 to 5.5 V.
- High voltage generator supply voltage range V_{DD2} to V_{SS} and V_{DD3} to V_{SS}:
  - 2.4 to 4.5 V with LCD voltage internally generated (voltage generator enabled).
- Display supply voltage range V_{LCD} to V_{SS}:
  - 4.5 to 9.0 V
- Low power consumption, suitable for battery operated systems
- Temperature compensation of V_{LCD}
- Slim chip layout, suitable for Chip-On-Glass (COG) applications
- Programmable bottom row pads mirroring and top row pads mirroring, for compatibility with both Tape Carrier Package (TCP) and COG applications.

2 APPLICATIONS

- Telecom equipment
- Portable instruments
- Point of sale terminals.

3 GENERAL DESCRIPTION

The PCF8548 is a low power CMOS LCD controller driver, designed to drive a graphic display of 65 rows and 102 columns. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD supply and bias voltages, resulting in a minimum of external components and low power consumption.
The PCF8548 interfaces to most microcontrollers via an I^2C-bus interface.

3.1 Packages

The PCF8548 is available as chip with bumps in tray; tape carrier package is available on request.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8548U/2	Tray	chip with bumps in tray	–
PCF8548U/9	Bumped wafer	quarter wafer	–

5 BLOCK DIAGRAM

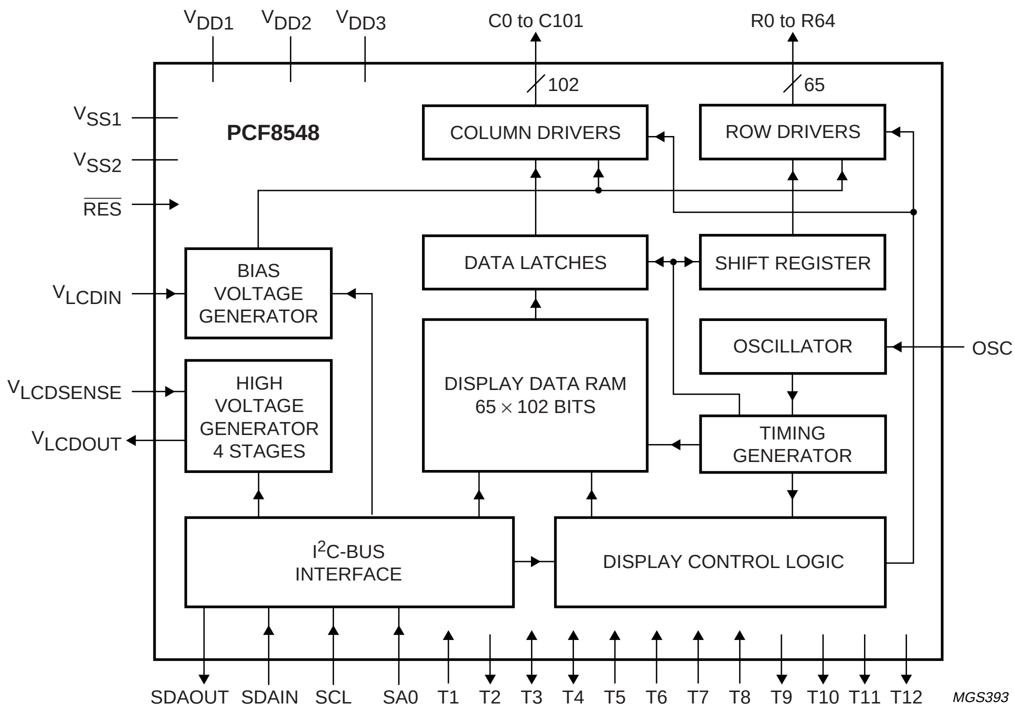


Fig.1 Block diagram.

6 PINNING

SYMBOL	PAD	DESCRIPTION
$\overline{RES}$	1	external reset input (active LOW)
SDAOUT	2	I^2C-bus data output
SDAIN	3 and 4	I^2C-bus data input
SCL	5 and 6	I^2C-bus clock input
T2	7	test 2 output
SA0	8	least significant bit of slave address
T7 to T5	9 to 11	test inputs
T4 and T3	12 and 13	test input/output
T1	14	test input
V_{SS1}	15 to 20	negative power supply 1
V_{SS2}	21 to 26	negative power supply 2
V_{LCDOUT}	28 to 33	voltage multiplier output
$V_{LCDSENSE}$	34	voltage multiplier regulation input (V_{LCD})

SYMBOL	PAD	DESCRIPTION
V_{LCDIN}	35 to 40	LCD supply voltage
R32 to R19	41 to 54	LCD row driver outputs
R0 to R18	57 to 75	LCD row driver outputs
C0 to C101	76 to 177	LCD column driver outputs
R50 to R33	178 to 195	LCD row driver outputs
R51 to R64	198 to 211	LCD row driver outputs
T12 to T9	212 to 215	test outputs
OSC	216	oscillator
T8	217	test input
V_{DD1}	218 to 223	supply voltage 1
V_{DD3}	224 to 226	supply voltage 3
V_{DD2}	227 to 233	supply voltage 2
	27, 55, 56, 196 and 197	dummy pads

7 PIN FUNCTIONS

7.1 R0 to R64: row driver outputs

These pads output the row signals.

7.2 C0 to C101: column driver outputs

These pads output the column signals.

7.3 V_{SS1} and V_{SS2}: negative power supply rails

V_{SS2} is related to V_{DD2} and V_{DD3} and V_{SS1} is related to V_{DD1}.

7.4 V_{DD1} to V_{DD3}: positive power supply rails

V_{DD2} and V_{DD3} are the supply voltages for the internal voltage generator. Both have to be at the same voltage and must be connected together outside of the chip. If the internal voltage generator is not used, they should both be connected to power or to the V_{DD1} pad.

V_{DD1} is used as the power supply for the rest of the chip. This voltage can be a different voltage than V_{DD2} and V_{DD3}.

7.5 V_{LCDIN}: LCD power supply

Internally generated positive power supply for the liquid crystal display. An external LCD supply voltage can be supplied using the V_{LCDIN} pad. In this case, V_{LCDOUT} has to be connected to ground, and the internal voltage generator has to be programmed to zero. If the PCF8548 is in power-down mode, the external LCD supply voltage must be switched off.

7.6 V_{LCDOUT}: LCD power supply

Positive power supply for the liquid crystal display. If the internal voltage generator is used, the two supply rails V_{LCDIN} and V_{LCDOUT} must be connected together and an external capacitor must be connected (see Fig.19).

7.7 $V_{LCDSENSE}$: voltage multiplier regulation input (V_{LCD})

$V_{LCDSENSE}$ is the input voltage for the internal voltage multiplier regulation.

If the internal voltage generator is used then $V_{LCDSENSE}$ must be connected to V_{LCDOUT}. If an external supply voltage is used then $V_{LCDSENSE}$ must be connected to ground.

7.8 T1 to T12: test pads

T1 and T3 to T7 must be connected to V_{SS1}. T8 must be connected to V_{DD1}. T2 and T9 to T12 must be left open-circuit; not accessible to user.

7.9 SDAIN and SDAOUT: I²C-bus data lines

Serial data and acknowledge lines for the I²C-bus.
By connecting SDAIN to SDAOUT, the SDA line becomes fully I²C-bus compatible. Having the acknowledge output (SDAOUT) separated from the serial data line is advantageous in Chip-On-Glass (COG) applications.
In COG applications where the track resistance from the SDAOUT pad to the system SDA line can be significant, a potential divider is generated by the bus pull-up resistor and the Indium Tin Oxide (ITO) track resistance. It is possible that during the acknowledge cycle the PCF8548 will not be able to create a valid logic 0 level. By splitting the SDA input from the output the device could be used in a mode that ignores the acknowledge bit. In COG applications where the acknowledge cycle is required, it is necessary to minimize the track resistance from the SDACK pad to the system SDA line to guarantee a valid LOW level.

7.10 SCL: I²C-bus clock signal

I²C-bus serial clock signal input.

7.11 SA0: slave address

Two different slave addresses can be selected using the SA0 pad. This allows two PCF8548 LCD drivers to be connected to the same I²C-bus.

7.12 OSC: oscillator

When the on-chip oscillator is used this input must be connected to V_{DD1}. An external clock signal, if used, is connected to this input.

7.13 $\overline{\text{RES}}$: reset

This signal is used to reset the device. The signal is active LOW.

8 BLOCK DIAGRAM FUNCTIONS

8.1 Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and the OSC input must be connected to V_{DD1}. An external clock signal (if used), is connected to this input.

8.2 I²C-bus interface

The I²C-bus interface receives and executes the commands sent via the I²C-bus. It also receives RAM data and sends it to the RAM.

8.3 Display control logic

The display control logic generates the control signals to read from the RAM via the 102 bits parallel port. It also generates the control signals for the row and column drivers.

8.4 Display Data RAM (DDRAM)

The PCF8548 contains a 65 × 102 bit static RAM which stores the display data. The RAM is divided into 8 banks of 102 bytes and 1 bank of 102 bits [(8 × 8 + 1) × 102 bits]. During RAM access, data is transferred to the RAM via the I²C-bus interface. There is a direct correspondence between the X address and column output number.

8.5 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not disturbed by operations on the I²C-bus.

8.6 LCD row and column drivers

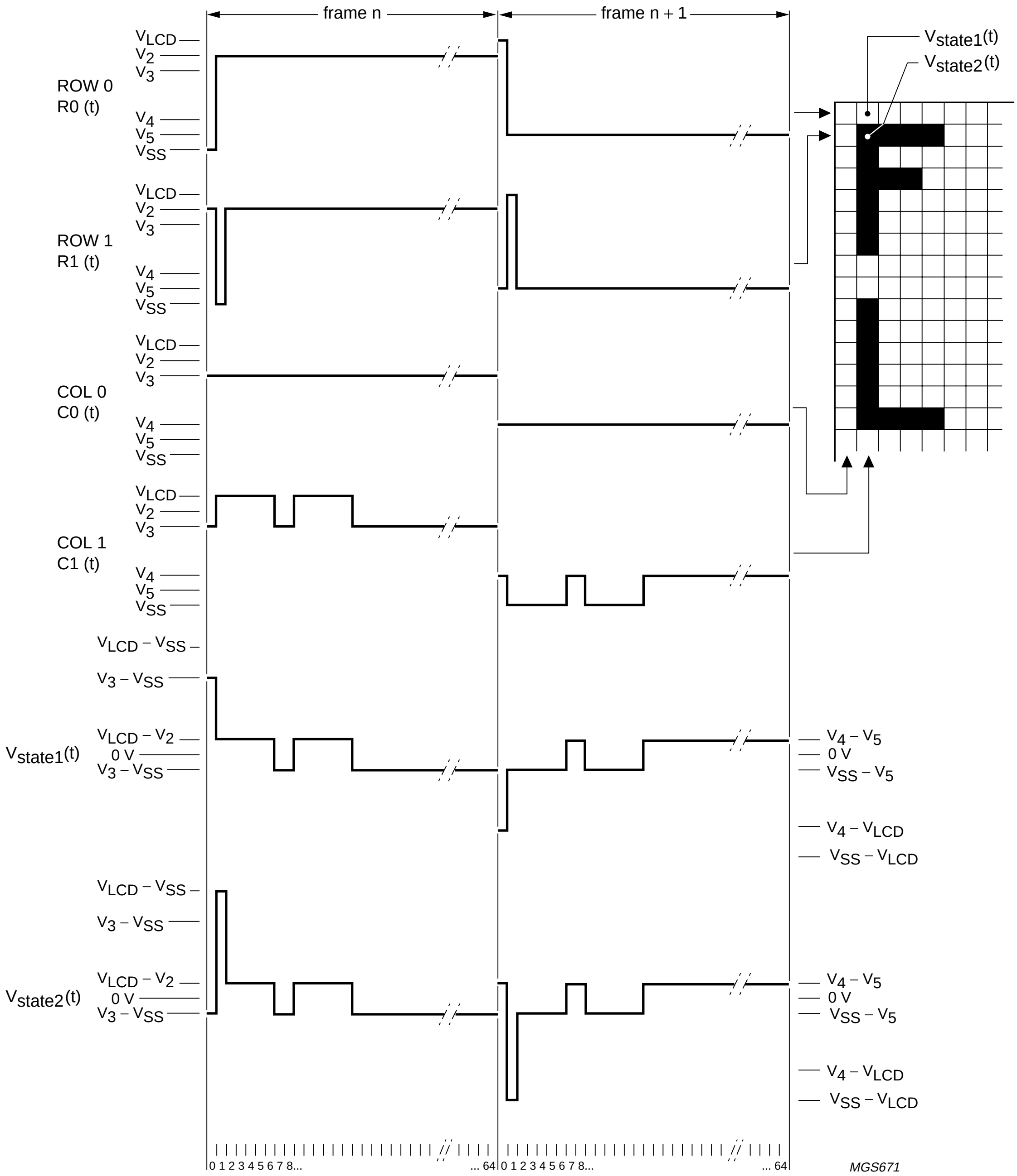
The PCF8548 contains 65 row and 102 column drivers, which connect the appropriate LCD bias voltages to the display in accordance with the data to be displayed. Figure 2 shows typical waveforms. Unused outputs should be left unconnected.

9 INITIALIZATION

Immediately following Power-on, all internal registers and the RAM content are undefined. A reset pulse must first be applied.

Reset is accomplished by applying an external $\overline{RES}$ pulse (active LOW). When reset occurs within the specified time all internal registers are initialized, however the RAM is still undefined. The state after reset is described in Section 12.1.

The $\overline{RES}$ input must be ≤0.3 V_{DD} when V_{DD} reaches $V_{DD(min)}$ (or higher) within a maximum time t_{VHRL} after V_{DD} goes HIGH (see Fig.17).



$V_{state1}(t) = C1(t) - R0(t)$.

$V_{state2}(t) = C1(t) - R1(t)$.

Fig.2 Typical LCD driver waveforms.

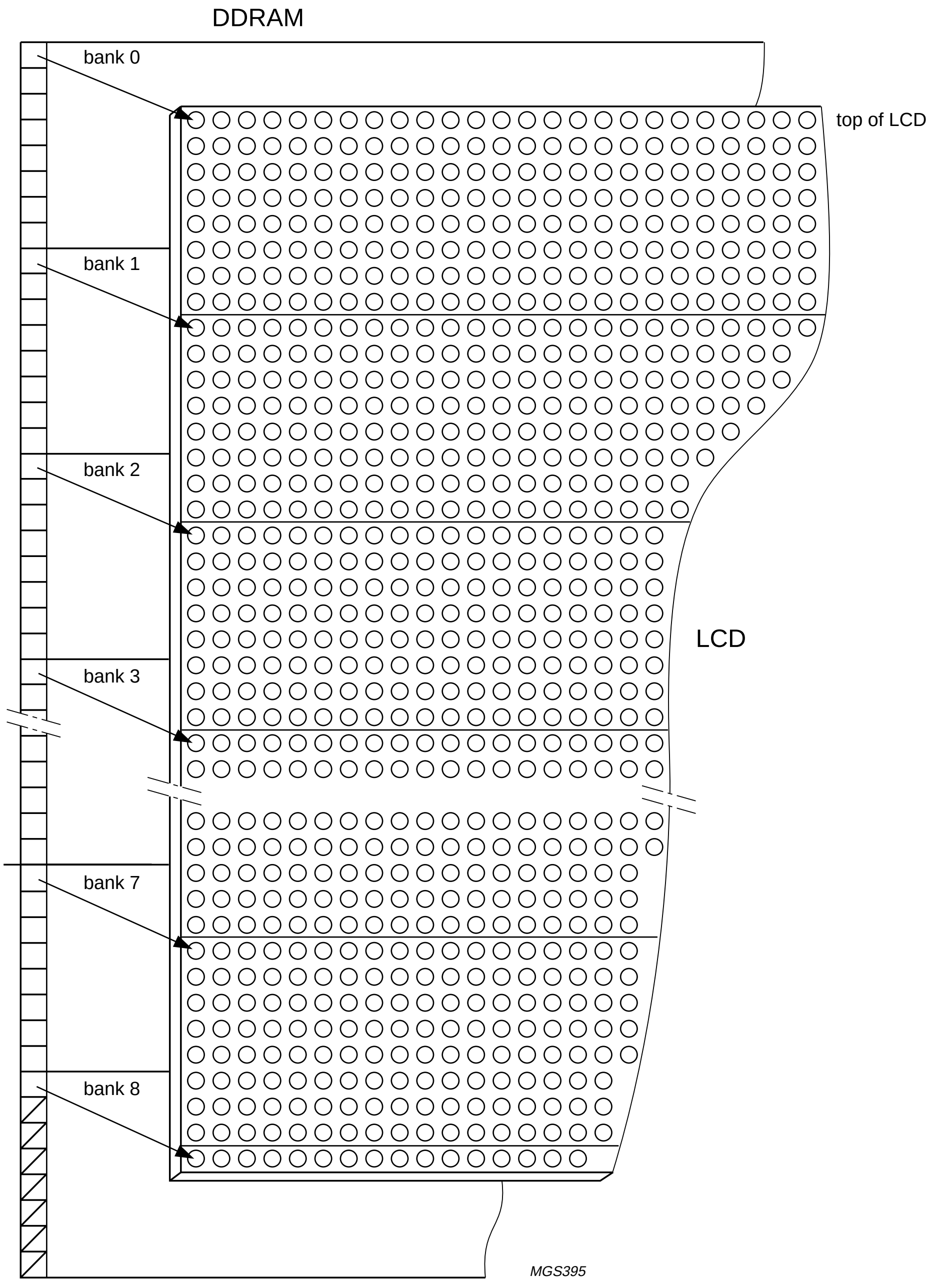


Fig.3 DDRAM to display mapping.

10 ADDRESSING

The Display Data RAM (DDRAM) of the PCF8548 is accessed as indicated in Figs 3, 6, 7, 8 and 9. The DDRAM has a matrix of 65 × 102 bits. The RAM cells are addressed by the X and Y address pointers. The address ranges are X0 to X101 (1100101b) and Y0 to Y8 (1000b). Addresses outside of these ranges are not allowed. In vertical addressing mode (V = 1) the Y address increments after each byte (see Fig.5). After the last Y address (Y = 8), Y wraps around to 0 and X increments to address the next column. In the horizontal addressing mode (V = 0) the X address increments after each byte (see Fig.4). After the last X address (X = 101), X wraps around to 0 and Y increments to address the next row. After the very last address (X = 101 and Y = 8) the address pointers wrap around to address X = 0 and Y = 0.

10.1 Display data RAM structure

Fig.4 Sequence of writing data bytes into RAM with horizontal addressing (V = 0).

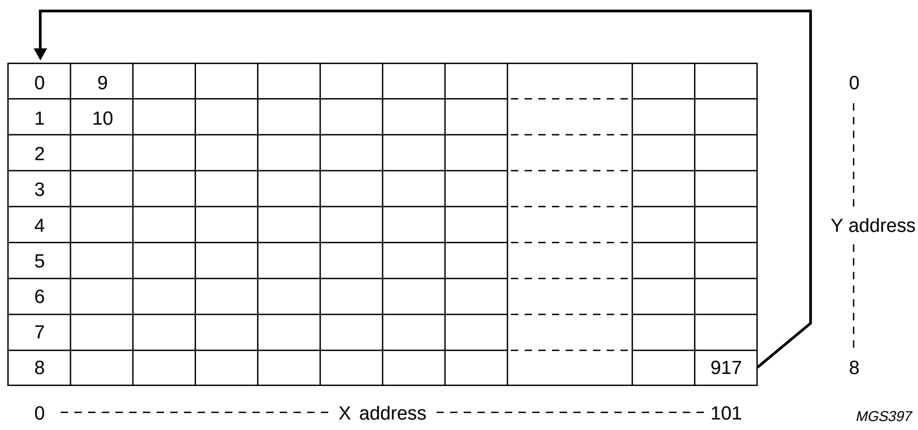


Fig.5 Sequence of writing data bytes into RAM with vertical addressing (V = 1).

The DO bit defines the bit order (MSB on top or MSB on bottom) for writing to the RAM (see Figs 6 and 7).

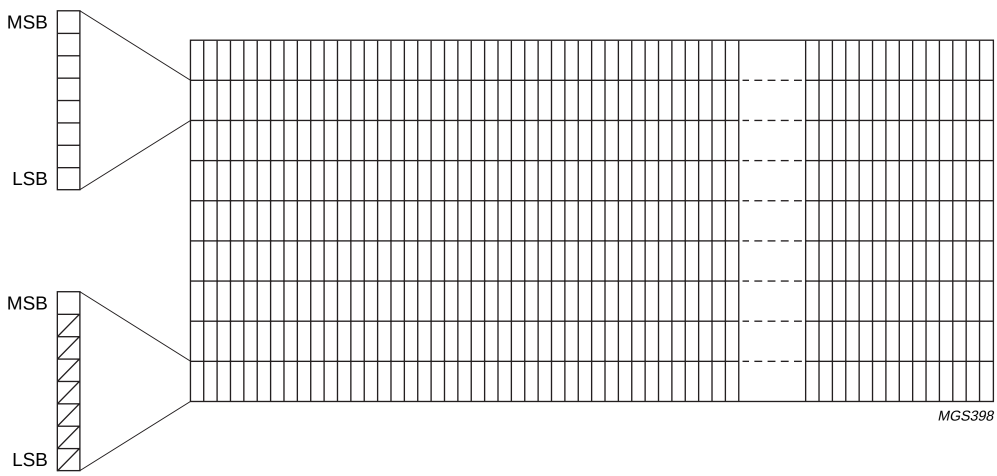


Fig.6 RAM byte organization, if DO = 0.

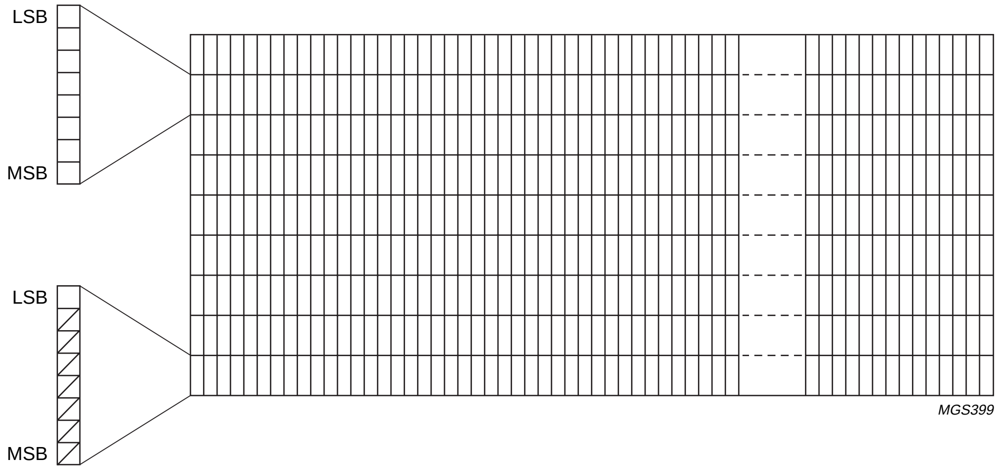


Fig.7 RAM byte organization, if DO = 1.

The MX bit allows a horizontal mirroring; when MX = 1, the X address space is mirrored. The address X = 0 is then located at the right side (column 101) of the display (see Fig.9). When MX = 0 the mirroring is disabled and the address X = 0 is located at the left side (column 0) of the display (see Fig.8).

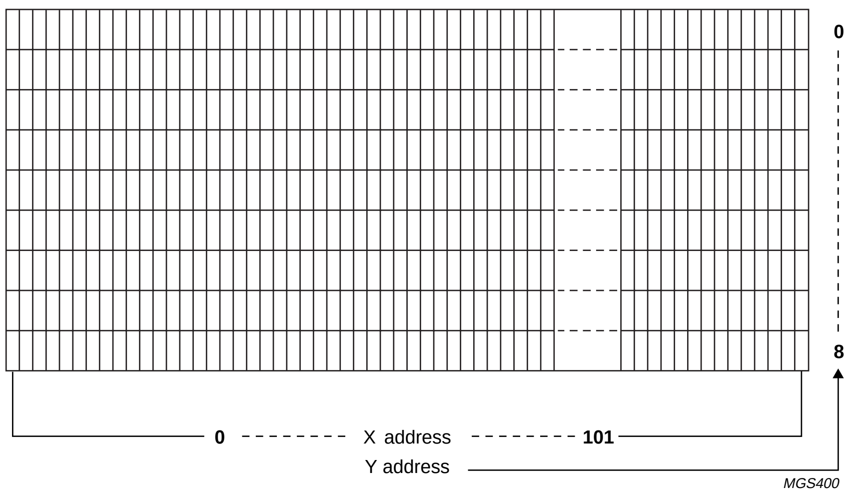


Fig.8 RAM format addressing (MX = 0).

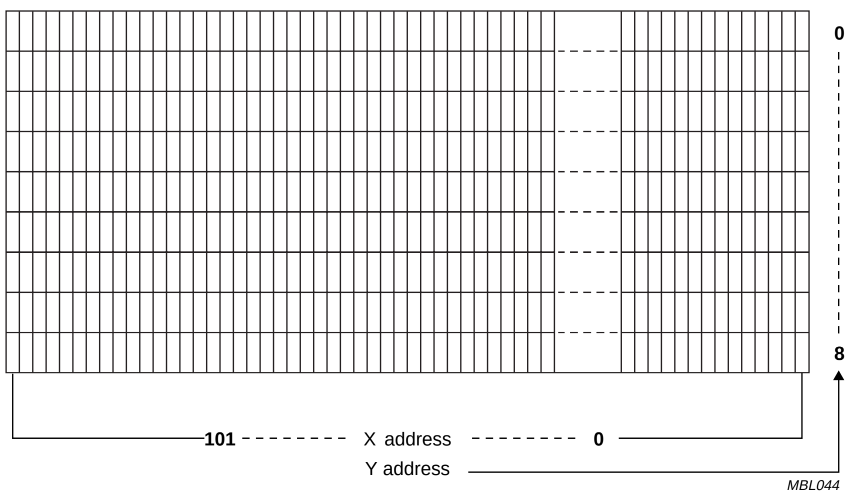


Fig.9 RAM format addressing (MX = 1).

10.2 RAM access

If the D/$\overline{C}$ bit is logic 1 the RAM can be written to. The data is written to the RAM during the acknowledge cycle.

11 I^{2}C-BUS INTERFACE

11.1 Characteristics of the I^{2}C-bus

The I^{2}C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

11.1.1 BIT TRANSFER

One data bit is transferred during each clock pulse.
The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Fig.10.

11.1.2 START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S).
A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig.11.

11.1.3 SYSTEM CONFIGURATION

The system configuration is illustrated in Fig.12.

- Transmitter: the device which sends the data to the bus
- Receiver: the device which receives the data from the bus
- Master: the device which initiates a transfer, generates clock signals and terminates a transfer
- Slave: the device addressed by a master
- Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronization: procedure to synchronize the clock signals of two or more devices.

11.1.4 ACKNOWLEDGE

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. A master receiver must also generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I^{2}C-bus is illustrated in Fig.13.

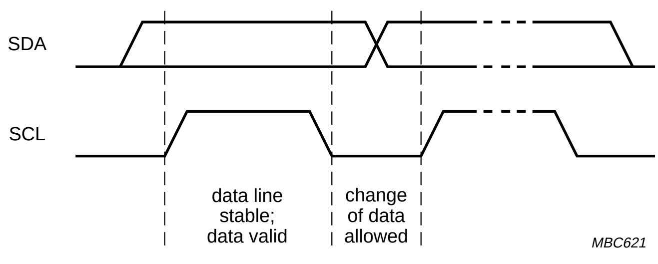


Fig.10 Bit transfer.

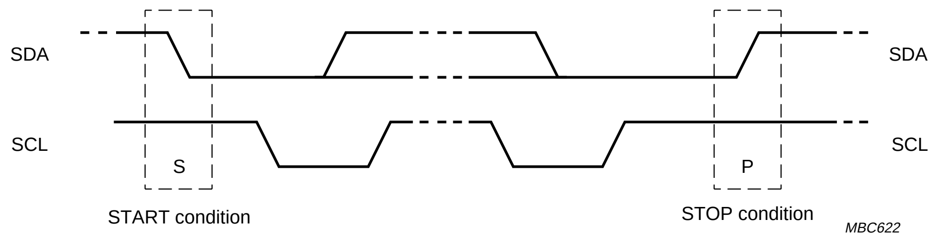


Fig.11 Definition of START and STOP conditions.

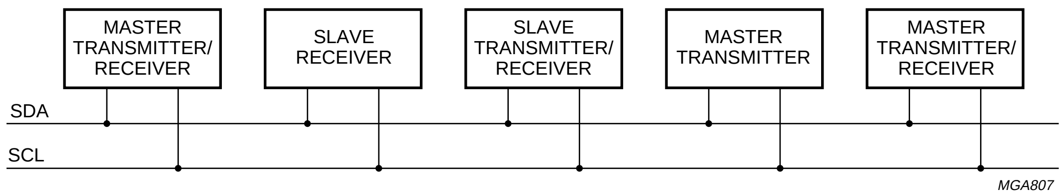


Fig.12 System configuration.

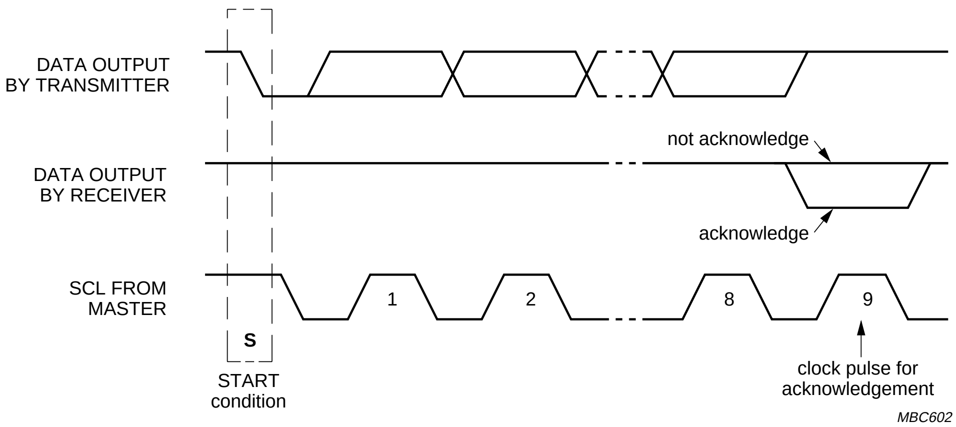


Fig.13 Acknowledgement on the I²C-bus.

11.2 I²C-bus protocol

The PCF8548 supports command, data write and status read access.

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. Two 7-bit slave addresses (0111100 and 0111101) are reserved for the PCF8548. The least significant bit of the slave address is set by connecting the input SA0 to either logic 0 (V_{SS1}) or logic 1 (V_{DD1}).

The I²C-bus protocol is illustrated in Fig.14.

The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C-bus transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves.
A command word consists of a control byte, which defines Co and D/$\overline{C}$, plus a data byte (see Fig.14 and Table 1).

The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data bytes will follow. The state of the D/$\overline{C}$ bit defines whether the data byte is interpreted as a command or as RAM data.

The control and data bytes are also acknowledged by all addressed slaves on the bus.

After the last control byte, depending on the D/$\overline{C}$ bit setting, either a series of display data bytes or command data bytes may follow. If the D/$\overline{C}$ bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended PCF8548 device. If the D/$\overline{C}$ bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. The acknowledgement after each byte is made only by the addressed slave. At the end of the transmission the I²C-bus master issues a STOP condition (P).

If the R/$\overline{W}$ bit is set to logic 1 the chip will output data immediately after the slave address if the D/$\overline{C}$ bit, which was sent during the last write access, is set to logic 0. If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

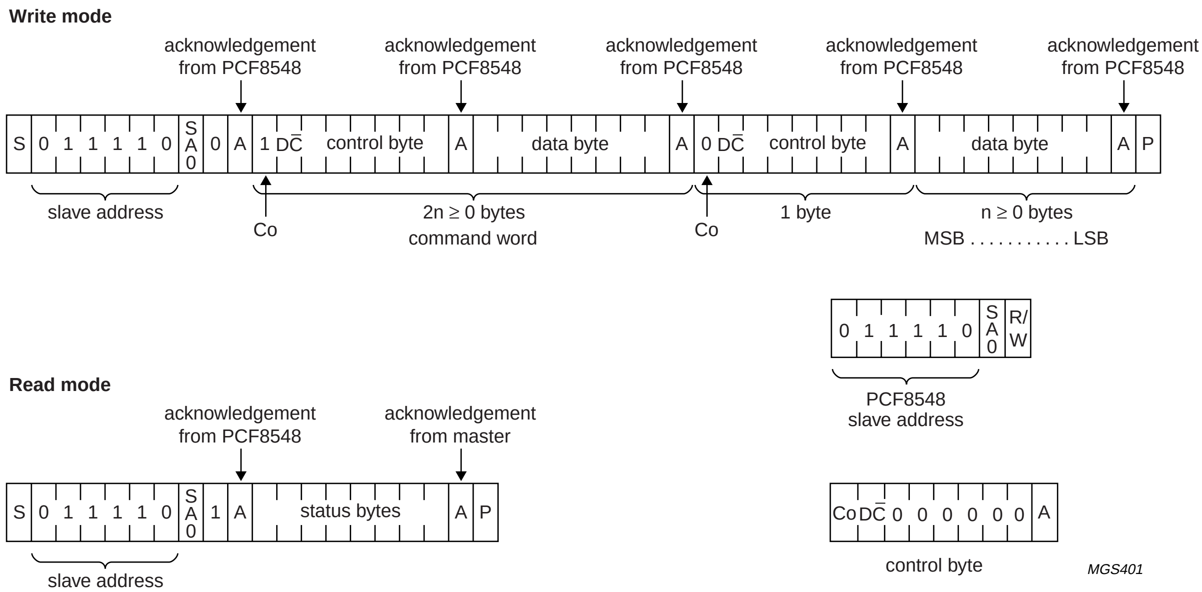


Fig.14 I²C-bus protocol.

12 INSTRUCTIONS

The instruction format is divided into two modes:

1. If $D/\overline{C}$ is set LOW, commands can be sent to the chip.
2. If $D/\overline{C}$ is set HIGH, the DDRAM will be accessed.

Every instruction can be sent in any order to the PCF8548.

Table 1 Instruction set

INSTRUCTION	$D/\overline{C}$	$R/\overline{W}$	COMMAND BYTE								DESCRIPTION
			B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
H = 0 or 1											
NOP	0	0	0	0	0	0	0	0	0	0	no operation
Reserved	0	0	0	0	0	0	0	0	0	1	do not use
Function set	0	0	0	0	1	MX	MY	PD	V	H	Power-down control; entry mode; extended instruction set control (H)
Read status byte	0	1	PD	TRS	BRS	D	E	MX	MY	DO	read status byte
Write data	1	0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	writes data to RAM
H = 0											
Reserved	0	0	0	0	0	0	0	0	1	X	do not use
Set V_{LCD} range	0	0	0	0	0	0	0	1	0	PRS	V_{LCD} programming range select
Display control	0	0	0	0	0	0	1	D	0	E	sets display configuration
Set HV-gen stages	0	0	0	0	0	1	0	0	S1	S0	# of HV-gen voltage multiplication
Set Y address of RAM	0	0	0	1	0	0	Y_3	Y_2	Y_1	Y_0	sets Y address of RAM: $0 \leq Y \leq 8$
Set X address of RAM	0	0	1	X_6	X_5	X_4	X_3	X_2	X_1	X_0	sets X address of RAM: $0 \leq X \leq 101$
H = 1											
Reserved	0	0	0	0	0	0	0	0	1	X	do not use
Temperature control	0	0	0	0	0	0	0	1	TC_1	TC_0	set temperature coefficient (TCx)
Display configuration	0	0	0	0	0	0	1	DO	TRS	BRS	top/bottom row mode set data order
Bias system	0	0	0	0	0	1	0	BS_2	BS_1	BS_0	set bias system (BSx)
Reserved	0	0	0	1	X	X	X	X	X	X	do not use (reserved for test)
Set V_{OP}	0	0	1	V_{OP6}	V_{OP5}	V_{OP4}	V_{OP3}	V_{OP2}	V_{OP1}	V_{OP0}	write V_{OP} to register

Table 2 Explanations of symbols in Table 1

BIT		0	1	RESET STATE
PD		chip is active	chip is in Power-down mode	1
V		horizontal addressing	vertical addressing	0
H		use basic instruction set	use extended instruction set	0
MX		normal X addressing	X address is mirrored	0
MY		display is not vertically mirrored	display is vertically mirrored	0
TRS		top rows are not mirrored	top rows are mirrored	0
BRS		bottom rows are not mirrored	bottom rows are mirrored	0
DO		MSB is on top	LSB is on top	0
PRS		V_{LCD} programming range LOW	V_{LCD} programming range HIGH	0
D and E	00	display blank		D = 0 E = 0
	10	normal mode		
	01	all display segments on		
	11	inverse video mode		
TC[1:0]	00	V_{LCD} temperature coefficient 0		TC[1:0] = 00
	01	V_{LCD} temperature coefficient 1		
	10	V_{LCD} temperature coefficient 2		
	11	V_{LCD} temperature coefficient 3		
S[1:0]	00	2 × voltage multiplier		S[1:0] = 00
	01	3 × voltage multiplier		
	10	4 × voltage multiplier		
	11	5 × voltage multiplier		
BS[2:0]		bias system		BS[2:0] = 000
V_{op}[6:0]		V_{LCD} programming		V_{op}[6:0] = 0000000

12.1 External reset ($\overline{RES}$)

After power-on a reset pulse must be applied immediately to the chip, as it is in an undefined state. A reset of the chip can be achieved using the external reset pad. After the reset the LCD driver is set to the following states:

- Power-down mode (PD = 1)
- All LCD outputs at V_{SS} (display off)
- Horizontal addressing (V = 0)
- Normal instruction set (H = 0)
- Normal display (MX = MY = TRS = BRS = 0)
- Display blank (E = D = 0)
- Address counter X[6:0] = 0 and Y[3:0] = 0
- Temperature coefficient (TC[1:0] = 0)
- Bias system (BS[2:0] = 0)
- V_{LCD} is equal to 0, the HV generator is switched off (V_{op}[6:0] = 0 and PRS = 0)
- After power-on (RAM data is undefined), the reset signal does not change the content of the RAM.

12.2 Function set

12.2.1 POWER-DOWN (PD)

- All LCD outputs at V_{SS} (display off)
- Bias generator and V_{LCD} generator off
- Oscillator off (external clock possible)
- V_{LCD} can be disconnected
- RAM contents not cleared (RAM data can be written)
- V_{LCD} output is discharged to V_{SS}.

12.2.2 V

When V = 0, the horizontal addressing is selected. The data is written to the RAM as shown in Fig.4. When V = 1, the vertical addressing is selected. The data is written to the RAM as shown in Fig.5.

12.2.3 H

When H = 0 the commands ‘display control’, ‘set HV-gen stages’, ‘set Y address’ and ‘set X address’ can be performed. When H = 1 the other commands can be executed. The commands ‘write data’ and ‘function set’ can be executed in both cases.

12.2.4 MX

When MX = 0, the display RAM is written from left to right (X = 0 is on the left side of the display, X = 100 is on the right side of the display). When MX = 1 the display RAM is written from right to left (X = 0 is on the right side of the display, X = 100 is on the left side of the display).

Thus, if a horizontally mirroring of the display is desired the RAM must first be rewritten.

12.2.5 MY

When MY = 1, the display is mirrored vertically.

A change of this bit has an immediate effect on the display.

12.3 Display control

12.3.1 D AND E

The bits D and E select the display mode (see Table 2).

12.4 Display configuration

12.4.1 TRS

Bit TRS enables the top row pad blocks to be mirrored. This is used to enable flexibility in the wiring of the row lines from the PCF8548 to the LCD cell (e.g. COG or TCP wiring). When TRS = 0 rows 19 to 32 and rows 51 to 64 are organized as illustrated in Fig.22. When TRS = 1 rows 19 to 32 and rows 51 to 64 are mirrored and organized as illustrated in Fig.23.

12.4.2 BRS

Bit BRS enables the bottom row pad blocks to be mirrored. This is used to enable flexibility in the wiring of the row lines from the PCF8548 to the LCD cell (e.g. COG or TCP wiring). When BRS = 0 rows 0 to 18 and rows 33 to 50 are organized as illustrated in Fig.22. When BRS = 1 rows 0 to 18 and rows 33 to 50 are mirrored and organized as illustrated in Fig.23.

12.5 Set Y address of RAM

Y[3 : 0] defines the Y address vector address of the RAM.

Table 3 X and Y address ranges

Y_3	Y_2	Y_1	Y_0	CONTENT	ALLOWED X RANGE
0	0	0	0	bank 0 (display RAM)	0 to 101
0	0	0	1	bank 1 (display RAM)	0 to 101
0	0	1	0	bank 2 (display RAM)	0 to 101
0	0	1	1	bank 3 (display RAM)	0 to 101
0	1	0	0	bank 4 (display RAM)	0 to 101
0	1	0	1	bank 5 (display RAM)	0 to 101
0	1	1	0	bank 6 (display RAM)	0 to 101
0	1	1	1	bank 7 (display RAM)	0 to 101
1	0	0	0	bank 8 (display RAM); note 1	0 to 101

Note

1. In bank 8 only the MSB is accessed.

12.6 Set X address of RAM

The X address points to the columns. The range of X is 0 to 101 (65H).

12.7 Set HV generator stages

12.7.1 S[1:0]

The PCF8548 incorporates a software configurable voltage multiplier. After reset the voltage multiplier is set to $2 \times V_{DD2}$. Other voltage multiplier factors are set via the command 'set HV-gen stages' (see Tables 1 and 2).

12.8 Temperature control

Due to the temperature dependency of the liquid crystals viscosity, the LCD controlling voltage V_{LCD} must be increased with lower temperature to maintain optimum contrast.

There are 4 different temperature coefficients available in the PCF8548 (see Fig.15). The coefficients are selected by the two bits TC[1:0]. Table 6 shows the typical values of the different temperature coefficients. The coefficients are proportional to the programmed V_{LCD}.

12.9 Bias system

The Bias voltage levels are set in the ratio

of R – R – nR – R – R giving a $\frac{1}{n+4}$ bias system.

The resulting bias levels are shown in Table 5.

Different multiplex rates require different factors n (see Table 4); this is programmed by BS[2 : 0]. For Mux 1 : 65 the optimum bias value n is given by:

$n = \sqrt{m} - 3 = \sqrt{65} - 3 = 5.06 = 5$ resulting in $\frac{1}{9}$bias.

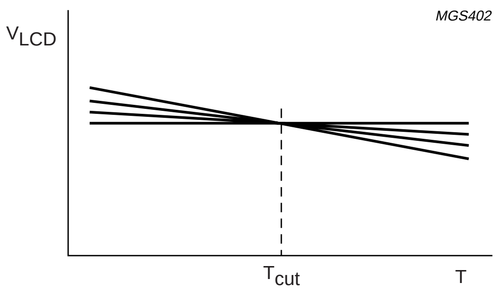


Fig.15 Temperature coefficients.

Table 4 Programming the required bias system

BS[2]	BS[1]	BS[0]	n	RECOMMENDED MUX RATE
0	0	0	7	1 : 100
0	0	1	6	1 : 81
0	1	0	5	1 : 64
0	1	1	4	1 : 49
1	0	0	3	1 : 36
1	0	1	2	1 : 24
1	1	0	1	1 : 16
1	1	1	0	1 : 9

Table 5 LCD bias voltage

SYMBOL	BIAS VOLTAGES	BIAS VOLTAGES FOR $\frac{1}{9}$ BIAS
V1	V_{LCD}	V_{LCD}
V2	(n + 3)/(n + 4)	$\frac{8}{9} \times V_{LCD}$
V3	(n + 2)/(n + 4)	$\frac{7}{9} \times V_{LCD}$
V4	2/(n + 4)	$\frac{2}{9} \times V_{LCD}$
V5	1/(n + 4)	$\frac{1}{9} \times V_{LCD}$
V6	V_{SS}	V_{SS}

12.10 Set V_{OP} value

The voltage at reference temperature can be calculated as: [V_{LCD} (T = T_{cut})]

$$V_{LCD_{(Tcut)}} = (a + V_{OP} \times b) \quad (1)$$

The operating voltage V_{LCD} can be set by software. The generated voltage is dependent on the temperature, programmed Temperature Coefficient (TC) and the programmed voltage at reference temperature (T_{cut}).

$$V_{LCD} = (a + V_{OP} \times b) \times [1 + (T - T_{cut}) \times TC] \quad (2)$$

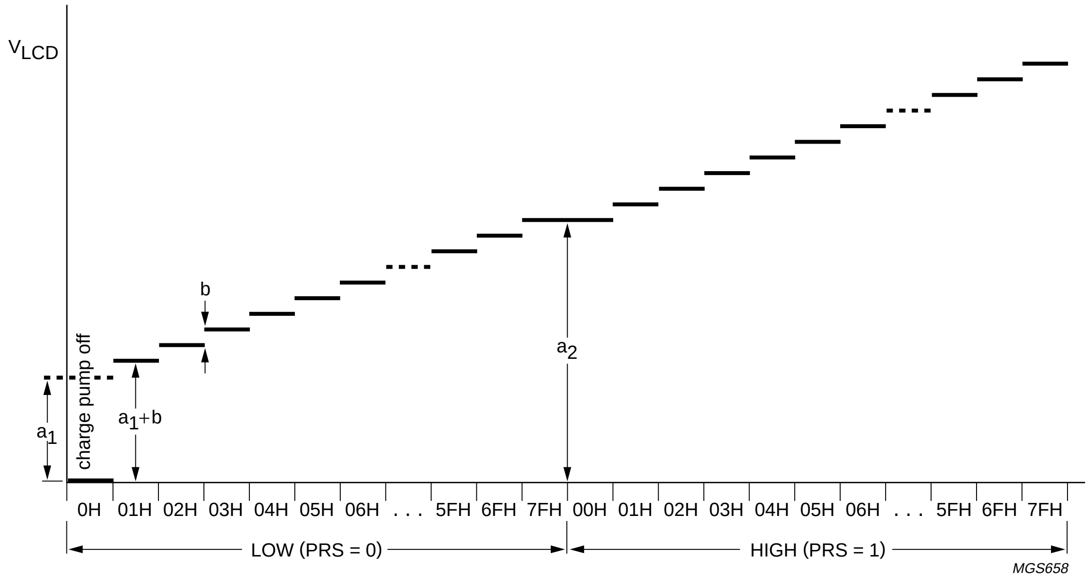
The parameters are explained in Fig.16 and Table 6. The maximum voltage that can be generated is dependent on the V_{DD2} voltage and the display load current. Two overlapping V_{LCD} ranges are selectable via the command ‘HV-gen control’. For the LOW (PRS = 0) range a = a_1 and for the HIGH (PRS = 1) range a = a_2 with steps equal to b in both ranges. It should be noted that the charge pump is turned off if V_{OP}[6;0] and bit PRS are all set to zero. For Mux 1 : 65 the optimum operation voltage of the liquid can be calculated as follows:

$$V_{LCD} = \frac{1 + \sqrt{65}}{\sqrt{2 \times \left(1 - \frac{1}{\sqrt{65}}\right)}} \times V_{th} = 6.85 \times V_{th}$$

where V_{th} is the threshold voltage of the liquid crystal material used.

Table 6 Typical values for parameters for the HV-generator programming

SYMBOL	BITS	VALUE	UNIT
a_1		2.94 (PRS = 0)	V
a_2		6.75 (PRS = 1)	V
b		0.03	V
T_{cut}		27	°C



V_{OP}[6:0] (programmed); 00H to 7FH, programme range LOW and HIGH.

Fig.16 V_{OP} programming of PCF8548.

As the programming range for the internally generated V_{LCD} allows values above the maximum allowed V_{LCD} (9.0 V) the customer must ensure while setting the V_{OP} register and selecting the temperature coefficient, under all conditions and including all tolerances V_{LCD} remains below 9.0 V.

13 LIMITING VALUES

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134); parameters are valid over operating temperature range unless otherwise specified; all voltages referenced to V_{SS} = 0 V. Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD1}	supply voltage	–0.5	+6.5	V
V_{DD2},V_{DD3}	supply voltage for internal voltage generator	–0.5	+4.5	V
V_{LCD}	supply voltage for the LCD	–0.5	+9.0	V
I_{SS}	supply current	–50	+50	mA
$V_{i(n)}$	all input voltages	–0.5	V_{DD} + 0.5	V
I_I	DC input current	–10	+10	mA
I_O	DC output current	–10	+10	mA
P_{pack}	power dissipation per package	–	300	mW
P/out	power dissipation per output	–	30	mW

14 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see “Handling MOS Devices”).

15 DC CHARACTERISTICS

V_{DD1} = 1.9 to 5.5 V; V_{DD2} and V_{DD3} = 2.4 to 4.5 V; V_{SS1} and V_{SS2} = 0 V; V_{LCD} = 4.5 to 9.0 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD1}	supply voltage		1.9	–	5.5	V
		T_{amb} = –25 to +85 °C	1.8	–	5.5	V
V_{DD2},V_{DD3}	supply voltage for internal voltage generator	LCD voltage internally generated (voltage generator enabled)	2.4	–	4.5	V
V_{LCDIN}	LCD input supply voltage	LCD voltage externally supplied (voltage generator disabled)	4.5	–	9.0	V
V_{LCDOUT}	LCD output supply voltage	LCD voltage internally generated (voltage generator enabled); note 1	4.5	–	9.0	V
I_{DD1}	supply current	V_{DD1} = 2.8 V; V_{LCD} = 7.6 V; f_{sclk} = 0; T_{amb} = 25 °C; notes 2 and 3	–	20	–	μA
I_{DD2},I_{DD3}	supply current for internal voltage generator	with external V_{LCD}	–	0.5	–	μA
		with internal V_{LCD} generation; V_{DD1} = 2.8 V; V_{LCD} = 7.6 V; f_{sclk} = 0; T_{amb} = 25 °C; no display load; 4 × charge pump; notes 2 and 3	–	180	–	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{DD(tot)}$	total supply current	with internal V_{LCD} generation; V_{DD1} = 2.8 V; V_{LCD} = 7.6 V; f_{sclk} = 0; T_{amb} = 25 °C; no display load; 4 × charge pump; notes 2 and 3	–	200	350	μA
		(Power-down mode) with internal or external V_{LCD} generation; note 4	–	1.5	10	μA
I_{LCDIN}	supply current from external V_{LCD}	V_{DD1} = 2.8 V; V_{LCD} = 7.6 V; f_{sclk} = 0; T_{amb} = 25 °C; no display load; notes 2, 3 and 5	–	30	–	μA
Logic						
V_{IL}	LOW-level input voltage		V_{SS1}	–	0.3V_{DD1}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD1}	–	V_{DD1}	V
I_L	leakage current	V_i = V_{DD1} or V_{SS1}	–1	–	+1	μA
Column and row outputs						
R_{row}	row output resistance R0 to R64	V_{DD1} to V_{DD3} = 5.0 V; V_{LCD} = 7.6 V; I_L = 10 μA; outputs tested one at a time	–	12	20	kΩ
R_{col}	column output resistance C0 to C101	V_{LCD} = 7.6 V	–	12	20	kΩ
$V_{bias(col)}$	column bias tolerance C0 to C101		–100	0	+100	mV
$V_{bias(row)}$	row bias tolerance R0 to R64		–100	0	+100	mV
LCD supply voltage generator						
V_{LCD}	V_{LCD} tolerance internally generated	V_{DD1} = 2.8 V; V_{LCD} = 7.6 V; f_{sclk} = 0; T_{amb} = 25 °C; no display load; notes 2, 3 6 and 7	–300	0	+300	mV
TC	temperature coefficient	00	–	-0.0×10^{-3}	–	1/°C
		01	–	-0.76×10^{-3}	–	1/°C
		10	–	-1.05×10^{-3}	–	1/°C
		11	–	-2.10×10^{-3}	–	1/°C

Notes

1. The maximum possible V_{LCD} voltage that can be generated is dependent on voltage, temperature and (display) load.
2. Internal clock.
3. When f_{sclk} = 0 there is no I^2C-bus clock.
4. Power-down mode. During power-down all static currents are switched off.
5. If external V_{LCD}, the display load current is not transmitted to I_{DD}.
6. Tolerance depends on the temperature; (typically zero at T_{amb} = 27 °C), maximum tolerance values are measured at the temperature range limit.
7. For TC0 to TC3.

16 AC CHARACTERISTICS

V_{DD1} = 1.9 to 5.5 V; V_{DD2} and V_{DD3} = 2.4 to 4.5 V; V_{SS1} and V_{SS2} = 0 V; V_{LCD} = 4.5 to 9 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{OSC}	oscillator frequency	V_{DD1} = 2.8 V; T_{amb} = –20 to +70 °C	20	38	70	kHz
$f_{clk(ext)}$	external clock frequency		20	38	100	kHz
f_{frame}	frame frequency	f_{OSC} or $f_{clk(ext)}$ = 38 kHz; note 1	–	73	–	Hz
t_{VHRL}	V_{DD1} to $\overline{RES}$ LOW	see Fig.17 and note 2	0	–	1	µs
$t_{W(RES)}$	$\overline{RES}$ LOW pulse width	see Fig.17 and note 3	100	–	–	ns
I²C-bus timing characteristics; see note 4						
f_{SCLK}	SCL clock frequency		0	–	400	kHz
t_{SCLL}	SCL clock LOW period		1.3	–	–	µs
t_{SCLH}	SCL clock HIGH period		0.6	–	–	µs
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	0.9	µs
t_r	SCL and SDA rise time	note 5	20 + 0.1C_b	–	300	ns
t_f	SCL and SDA fall time	note 5	20 + 0.1C_b	–	300	ns
$t_{f(SDA)(ro)}$	SDA fall time for read out	V_{DD1} = <3.6 V	20 + 0.1C_b	–	1000	ns
C_b	capacitive load represented by each bus line		–	–	400	pF
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	–	–	µs
$t_{HD;STA}$	START condition hold time		0.6	–	–	µs
$t_{SU;STO}$	set-up time for STOP condition		0.6	–	–	µs
t_{SW}	tolerable spike width on bus	note 6	–	–	50	ns
t_{BUF}	bus free time between a STOP and START condition		1.3	–	–	µs

Notes

1. $f_{frame} = \frac{f_{clk(ext)}}{520}$
2. $\overline{RES}$ may be LOW before V_{DD1} goes HIGH.
3. If $t_{W(RES)}$ is longer than 3 ns (typical) a reset may be generated.
4. All timing values are valid within the operating supply voltage and ambient temperature ranges and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
5. The rise and fall times specified here refer to the driver device (i.e. not PCF8548) and are part of the general fast I²C-bus specification. When PCF8548 asserts an acknowledge on SDA, the minimum fall time is 10 ns. C_b = capacitive load per bus line.
6. The device inputs SDA and SCL are filtered and will reject spikes on the bus lines of width <$t_{SW(max)}$.

17 RESET

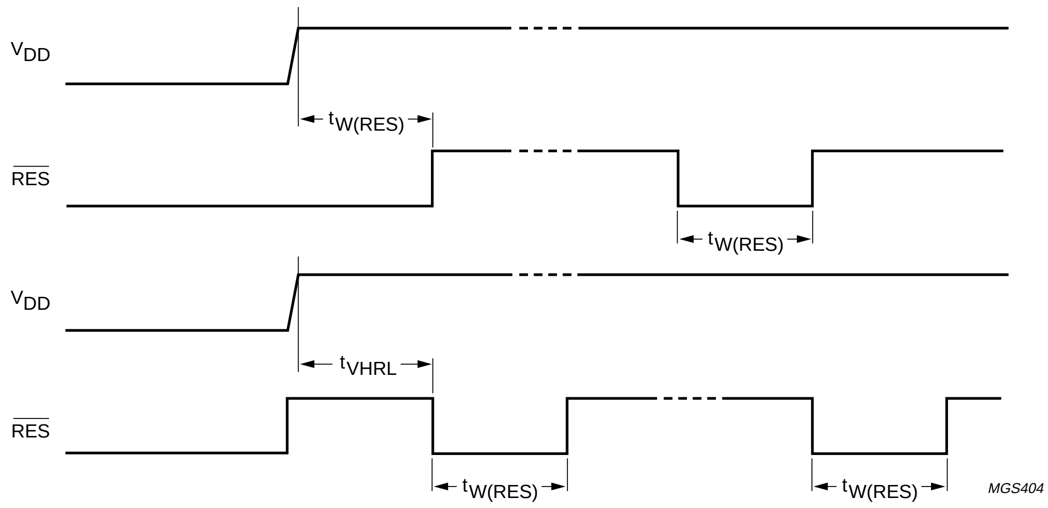
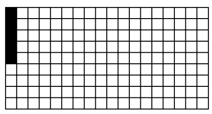
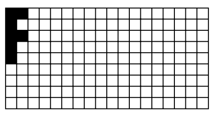
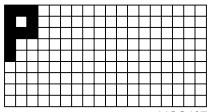
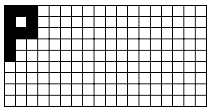
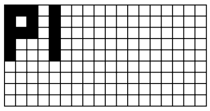
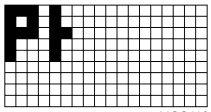
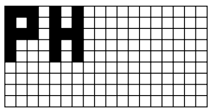
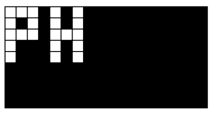
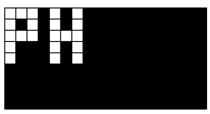


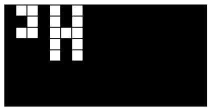
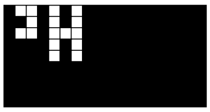
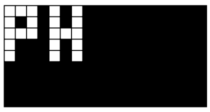
Fig.17 Reset timing.

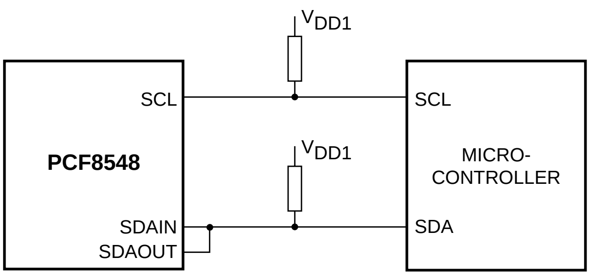
18 APPLICATION INFORMATION

Table 7 Programming example for PCF8548

STEP	BITS								DISPLAY	OPERATION
	B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**		
1	I^2C-bus start									
2	0	1	1	1	1	0	0	0		slave address for write
3	0	0	0	0	0	0	0	0		control byte with cleared Co bit and D/$\overline{C}$ set to logic 0
4	0	0	1	0	0	0	0	1		function set; PD = 0; V = 0; select extended instruction set (H = 1 mode)
5	0	0	0	1	0	0	1	0		set bias system 2; this is the recommended bias system for a multiplex rate 1 : 65
6	1	1	1	0	1	0	1	0		set V_{OP}; V_{OP} is set to a +106 × b [V]; it should be noted that the required voltage is dependent on the liquid
7	0	0	1	0	0	0	0	0		function set; PD = 0; V = 0; select normal instruction set (H = 0 mode)
8	0	0	0	0	1	1	0	0		display control; set normal mode (D = 1; E = 0)
9	I^2C-bus start									restart; to write into the display RAM the D/$\overline{C}$ must be set to logic 1; therefore a control byte is needed
10	0	1	1	1	1	0	0	0		slave address for write
11	0	1	0	0	0	0	0	0		control byte with cleared Co bit and D/$\overline{C}$ set to logic 1
12	1	1	1	1	1	0	0	0	 MGS405	data write; Y and X are initialized to 0 by default, so they are not set here
13	1	0	1	0	0	0	0	0	 MGS406	data write

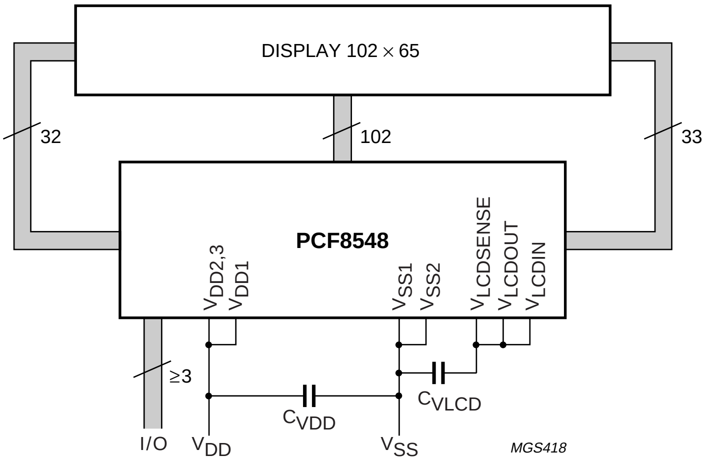
STEP	BITS								DISPLAY	OPERATION
	B7	B6	B5	B4	B3	B2	B1	B0		
14	1	1	1	0	0	0	0	0	 MGS407	data write
15	0	0	0	0	0	0	0	0	 MGS408	data write
16	1	1	1	1	1	0	0	0	 MGS409	data write
17	0	0	1	0	0	0	0	0	 MGS410	data write
18	1	1	1	1	1	0	0	0	 MGS411	data write
19	I^2C-bus start									restart
20	0	1	1	1	1	0	0	0		slave address for write
21	1	0	0	0	0	0	0	0		control byte with set Co bit and D/$\overline{C}$ set to logic 0
22	0	0	0	0	1	1	0	1	 MGS412	display control; set inverse video mode (D = 1; E = 1)
23	1	0	0	0	0	0	0	0		control byte with set Co bit and D/$\overline{C}$ set to logic 0
24	1	0	0	0	0	0	0	0	 MGS413	set X address of RAM; set address to ‘0000000’

STEP	BITS								DISPLAY	OPERATION
	B7	B6	B5	B4	B3	B2	B1	B0		
25	1	1	0	0	0	0	0	0		control byte with set Co bit and $D/\overline{C}$ set to logic 1
26	0	0	0	0	0	0	0	0	 MGS414	data write
27	0	0	0	0	0	0	0	0		control byte with cleared Co bit and $D/\overline{C}$ set to logic 0
28	1	0	0	0	0	0	0	0	 MGS415	set X address of RAM; set address to ‘0000000’
29	I²C-bus start									restart
30	0	1	1	1	1	0	0	0		slave address for write
31	1	1	0	0	0	0	0	0		control byte with set Co bit and $D/\overline{C}$ set to logic 1
32	1	1	1	1	1	0	0	0	 MGS416	write data
33	1	0	0	0	0	0	0	0		control byte with set Co bit and $D/\overline{C}$ set to logic 0



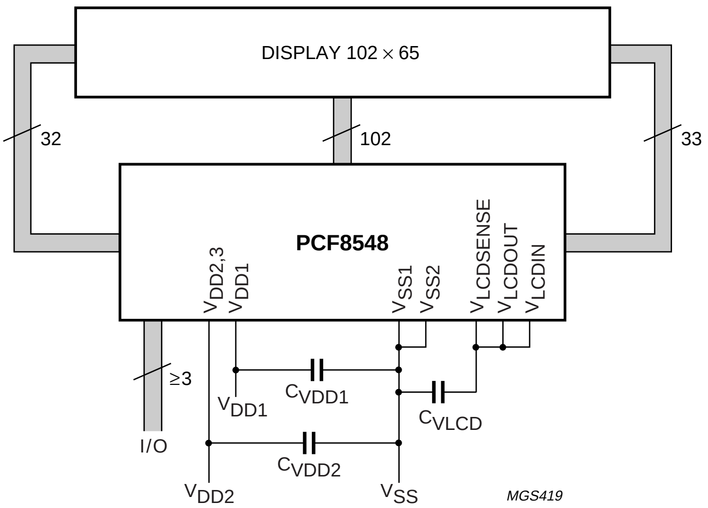
MGS417

Fig.18 Connecting the I²C-bus interface.



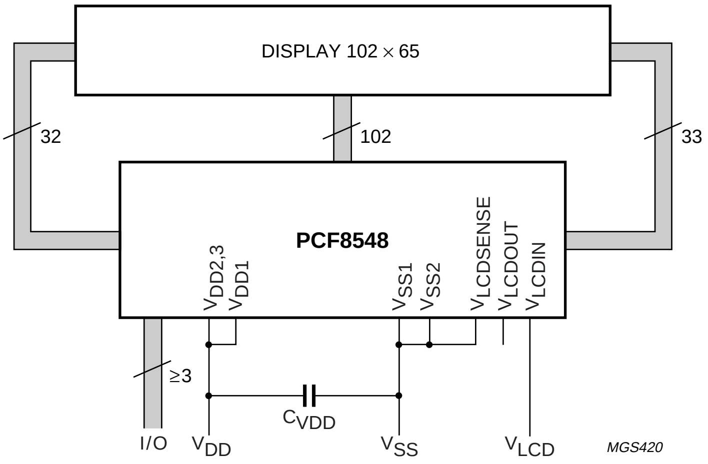
The number of I/Os depends on the application.

Fig.19 Internal charge pump is used and a single supply voltage.



The number of I/Os depends on the application.

Fig.20 Internal charge pump is used and two separate supply voltages.



The number of I/Os depends on the application.

Fig.21 External high voltage generation is used.

The pinning of the PCF8548 is optimized for single plane wiring e.g. for chip-on-glass display modules, or for TCP. Display size: 65 × 102 pixels. The required minimum value for the external capacitors in an application with the PCF8548 are: C_{VDD}, C_{VDD1}, C_{VDD2} and C_{VLCD} = 1.0 μF (min.). Higher capacitor values are recommended for ripple reduction.

To reduce the sensitivity of the reset to ESD/EMC disturbances for a COG application, it is strongly recommended to implement on the glass (ITO) a series input resistance in the reset line (The recommended minimum value is 8 kΩ).

19 CHIP INFORMATION

The PCF8548 is manufactured in n-well CMOS technology. The substrate is at V_{SS} potential.

20 PAD INFORMATION

PAD	VALUE	UNIT
Minimum bump pitch	70	μm
Pad size, alumin	62 × 100	μm
Bumps	50 (±6) × 90 (±6) × 17.5 (±5)	μm
Wafer thickness without bumps	U/2 = 381; U/9 = 525	μm

Table 8 Bonding pad location
All x and y coordinates are referenced to the centre of the chip (dimension in µm; see Fig.22).

SYMBOL	PAD	x	y
$\overline{RES}$	1	+1160	+899.4
SDAOUT	2	+840	+899.4
SDAIN	3	+600	+899.4
SDAIN	4	+520	+899.4
SCL	5	+200	+899.4
SCL	6	+120	+899.4
T2	7	–200	+899.4
SA0	8	–410	+899.4
T7	9	–620	+899.4
T6	10	–830	+899.4
T5	11	–1040	+899.4
T4	12	–1250	+899.4
T3	13	–1460	+899.4
T1	14	–1670	+899.4
V_{SS1}	15	–1750	+899.4
V_{SS1}	16	–1830	+899.4
V_{SS1}	17	–1910	+899.4
V_{SS1}	18	–1990	+899.4
V_{SS1}	19	–2070	+899.4
V_{SS1}	20	–2150	+899.4
V_{SS2}	21	–2310	+899.4
V_{SS2}	22	–2390	+899.4
V_{SS2}	23	–2470	+899.4
V_{SS2}	24	–2550	+899.4
V_{SS2}	25	–2630	+899.4
V_{SS2}	26	–2710	+899.4
dummy pad	27	–2790	+899.4
V_{LCDOUT}	28	–2950	+899.4
V_{LCDOUT}	29	–3030	+899.4
V_{LCDOUT}	30	–3110	+899.4
V_{LCDOUT}	31	–3190	+899.4
V_{LCDOUT}	32	–3270	+899.4
V_{LCDOUT}	33	–3350	+899.4
$V_{LCDSENSE}$	34	–3430	+899.4
V_{LCDIN}	35	–3510	+899.4
V_{LCDIN}	36	–3590	+899.4
V_{LCDIN}	37	–3670	+899.4
V_{LCDIN}	38	–3750	+899.4
V_{LCDIN}	39	–3830	+899.4
V_{LCDIN}	40	–3910	+899.4
R32	41	–4235	+899.4
R31	42	–4305	+899.4
R30	43	–4375	+899.4
R29	44	–4445	+899.4
R28	45	–4515	+899.4
R27	46	–4585	+899.4
R26	47	–4655	+899.4
R25	48	–4725	+899.4
R24	49	–4795	+899.4
R23	50	–4865	+899.4
R22	51	–4935	+899.4
R21	52	–5005	+899.4
R20	53	–5075	+899.4
R19	54	–5145	+899.4
dummy pad	55	–5355	+899.4
dummy pad	56	–5320	–899.4
R0	57	–5040	–899.4
R1	58	–4970	–899.4
R2	59	–4900	–899.4
R3	60	–4830	–899.4
R4	61	–4760	–899.4
R5	62	–4690	–899.4
R6	63	–4620	–899.4
R7	64	–4550	–899.4
R8	65	–4480	–899.4
R9	66	–4410	–899.4
R10	67	–4340	–899.4
R11	68	–4270	–899.4
R12	69	–4200	–899.4
R13	70	–4130	–899.4
R14	71	–4060	–899.4
R15	72	–3990	–899.4
R16	73	–3920	–899.4
R17	74	–3850	–899.4
R18	75	–3780	–899.4
C0	76	–3570	–899.4
C1	77	–3500	–899.4
C2	78	–3430	–899.4
C3	79	–3360	–899.4
C4	80	–3290	–899.4

SYMBOL	PAD	x	y
C5	81	–3220	–899.4
C6	82	–3150	–899.4
C7	83	–3080	–899.4
C8	84	–3010	–899.4
C9	85	–2940	–899.4
C10	86	–2870	–899.4
C11	87	–2800	–899.4
C12	88	–2730	–899.4
C13	89	–2660	–899.4
C14	90	–2590	–899.4
C15	91	–2520	–899.4
C16	92	–2450	–899.4
C17	93	–2380	–899.4
C18	94	–2310	–899.4
C19	95	–2240	–899.4
C20	96	–2170	–899.4
C21	97	–2100	–899.4
C22	98	–2030	–899.4
C23	99	–1960	–899.4
C24	100	–1890	–899.4
C25	101	–1750	–899.4
C26	102	–1680	–899.4
C27	103	–1610	–899.4
C28	104	–1540	–899.4
C29	105	–1470	–899.4
C30	106	–1400	–899.4
C31	107	–1330	–899.4
C32	108	–1260	–899.4
C33	109	–1190	–899.4
C34	110	–1120	–899.4
C35	111	–1050	–899.4
C36	112	–980	–899.4
C37	113	–910	–899.4
C38	114	–840	–899.4
C39	115	–770	–899.4
C40	116	–700	–899.4
C41	117	–630	–899.4
C42	118	–560	–899.4
C43	119	–490	–899.4
C44	120	–420	–899.4
C45	121	–350	–899.4
C46	122	–280	–899.4

SYMBOL	PAD	x	y
C47	123	–210	–899.4
C48	124	–140	–899.4
C49	125	–70	–899.4
C50	126	+0	–899.4
C51	127	+140	–899.4
C52	128	+210	–899.4
C53	129	+280	–899.4
C54	130	+350	–899.4
C55	131	+420	–899.4
C56	132	+490	–899.4
C57	133	+560	–899.4
C58	134	+630	–899.4
C59	135	+700	–899.4
C60	136	+770	–899.4
C61	137	+840	–899.4
C62	138	+910	–899.4
C63	139	+980	–899.4
C64	140	+1050	–899.4
C65	141	+1120	–899.4
C66	142	+1190	–899.4
C67	143	+1260	–899.4
C68	144	+1330	–899.4
C69	145	+1400	–899.4
C70	146	+1470	–899.4
C71	147	+1540	–899.4
C72	148	+1610	–899.4
C73	149	+1680	–899.4
C74	150	+1750	–899.4
C75	151	+1820	–899.4
C76	152	+1890	–899.4
C77	153	+2030	–899.4
C78	154	+2100	–899.4
C79	155	+2170	–899.4
C80	156	+2240	–899.4
C81	157	+2310	–899.4
C82	158	+2380	–899.4
C83	159	+2450	–899.4
C84	160	+2520	–899.4
C85	161	+2590	–899.4
C86	162	+2660	–899.4
C87	163	+2730	–899.4
C88	164	+2800	–899.4

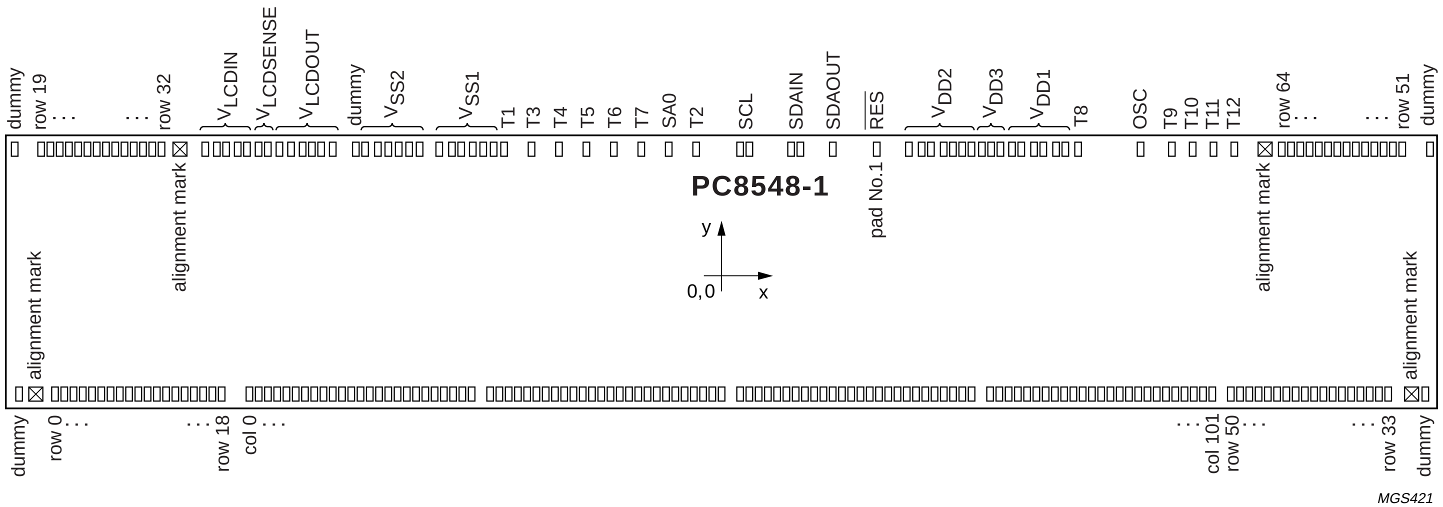
SYMBOL	PAD	x	y
C89	165	+2870	–899.4
C90	166	+2940	–899.4
C91	167	+3010	–899.4
C92	168	+3080	–899.4
C93	169	+3150	–899.4
C94	170	+3220	–899.4
C95	171	+3290	–899.4
C96	172	+3360	–899.4
C97	173	+3430	–899.4
C98	174	+3500	–899.4
C99	175	+3570	–899.4
C100	176	+3640	–899.4
C101	177	+3710	–899.4
R50	178	+3850	–899.4
R49	179	+3920	–899.4
R48	180	+3990	–899.4
R47	181	+4060	–899.4
R46	182	+4130	–899.4
R45	183	+4200	–899.4
R44	184	+4270	–899.4
R43	185	+4340	–899.4
R42	186	+4410	–899.4
R41	187	+4480	–899.4
R40	188	+4550	–899.4
R39	189	+4620	–899.4
R38	190	+4690	–899.4
R37	191	+4760	–899.4
R36	192	+4830	–899.4
R35	193	+4900	–899.4
R34	194	+4970	–899.4
R33	195	+5040	–899.4
dummy pad	196	+5320	–899.4
dummy pad	197	+5355	+899.4
R51	198	+5145	+899.4
R52	199	+5075	+899.4
R53	200	+5005	+899.4
R54	201	+4935	+899.4
R55	202	+4865	+899.4
R56	203	+4795	+899.4
R57	204	+4725	+899.4
R58	205	+4655	+899.4
R59	206	+4585	+899.4

SYMBOL	PAD	x	y
R60	207	+4515	+899.4
R61	208	+4445	+899.4
R62	209	+4375	+899.4
R63	210	+4305	+899.4
R64	211	+4235	+899.4
T12	212	+3880	+899.4
T11	213	+3720	+899.4
T10	214	+3560	+899.4
T9	215	+3400	+899.4
OSC	216	+3160	+899.4
T8	217	+2680	+899.4
V_{DD1}	218	+2600	+899.4
V_{DD1}	219	+2520	+899.4
V_{DD1}	220	+2440	+899.4
V_{DD1}	221	+2360	+899.4
V_{DD1}	222	+2280	+899.4
V_{DD1}	223	+2200	+899.4
V_{DD3}	224	+2120	+899.4
V_{DD3}	225	+2040	+899.4
V_{DD3}	226	+1960	+899.4
V_{DD2}	227	+1880	+899.4
V_{DD2}	228	+1800	+899.4
V_{DD2}	229	+1720	+899.4
V_{DD2}	230	+1640	+899.4
V_{DD2}	231	+1560	+899.4
V_{DD2}	232	+1480	+899.4
V_{DD2}	233	+1400	+899.4

Table 9 Alignment marks

x	y	MARKS
+5214	–899.4	mark 1
–5214	–899.4	mark 2
+4099	+899.4	mark 3
–4099	+899.4	mark 4

The alignment marks are circular with a diameter of 100 μm.



Maximum chip size: 2.12 mm × 10.99 mm.

Fig.22 Bonding pad location.

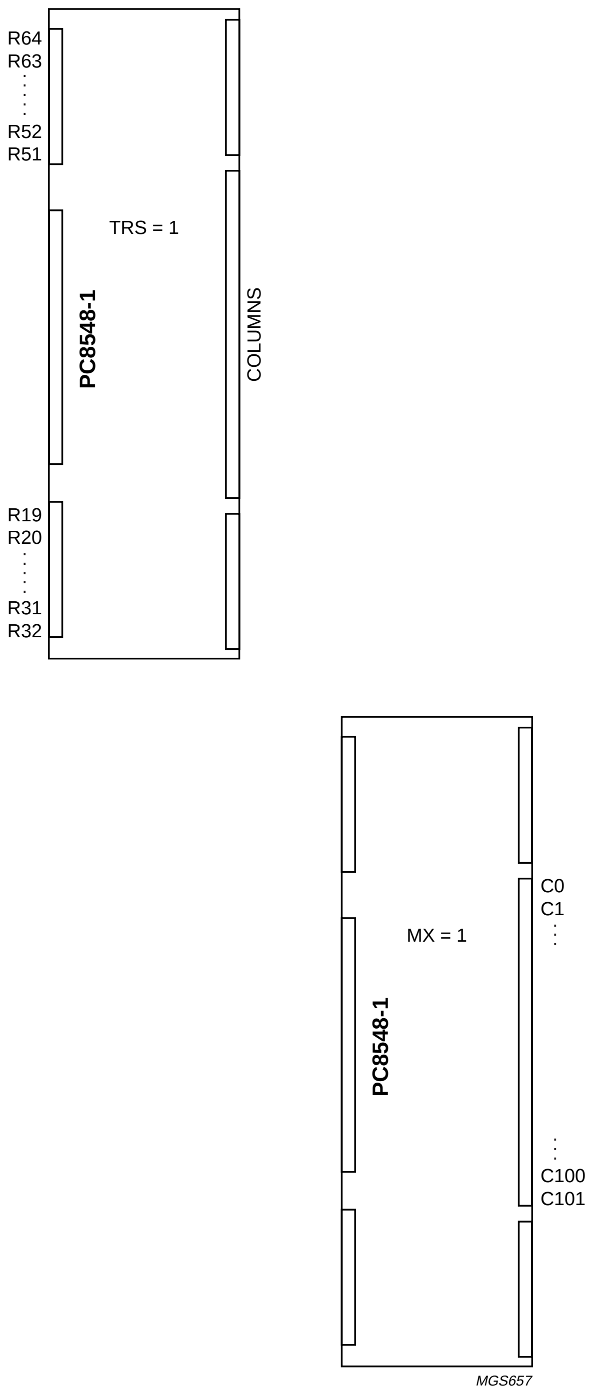


Fig.23 Pad layout for BRS, TRS and MX.

21 DEVICE PROTECTION DIAGRAM

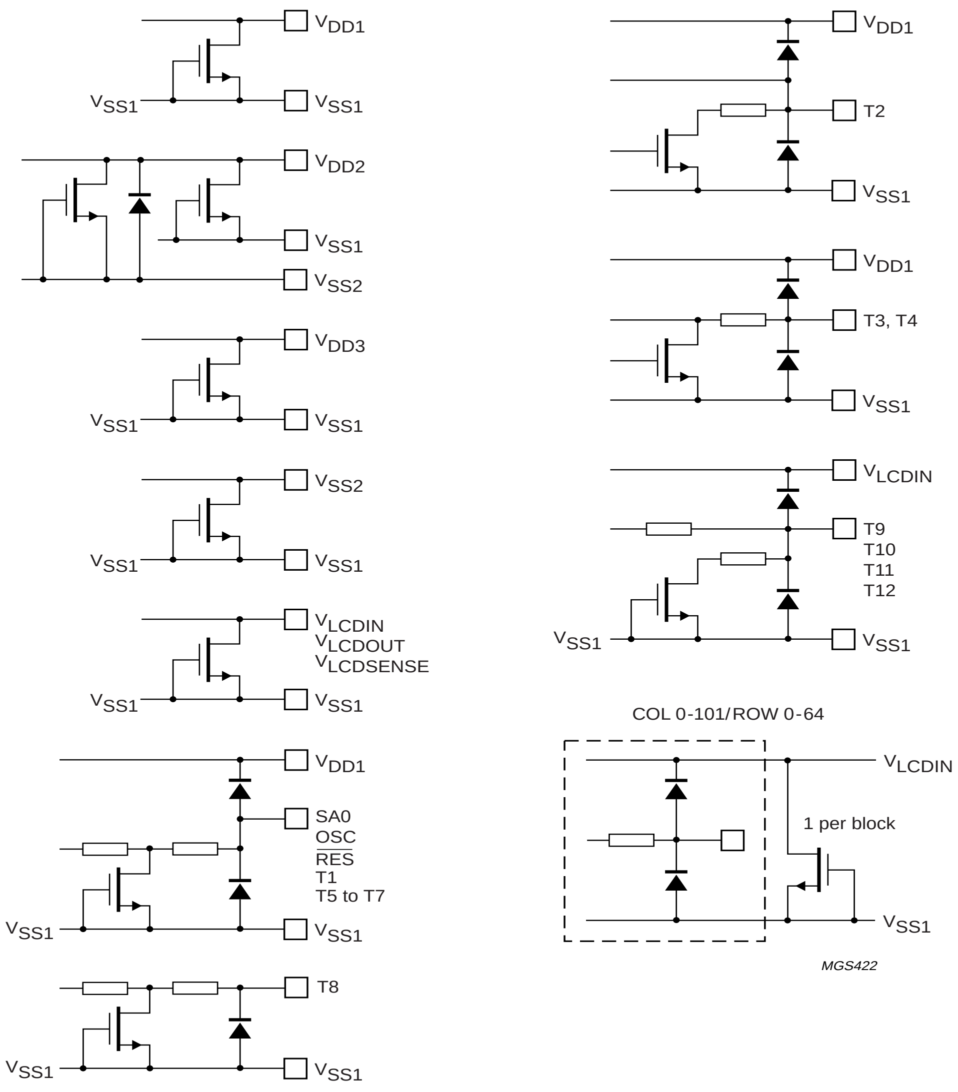
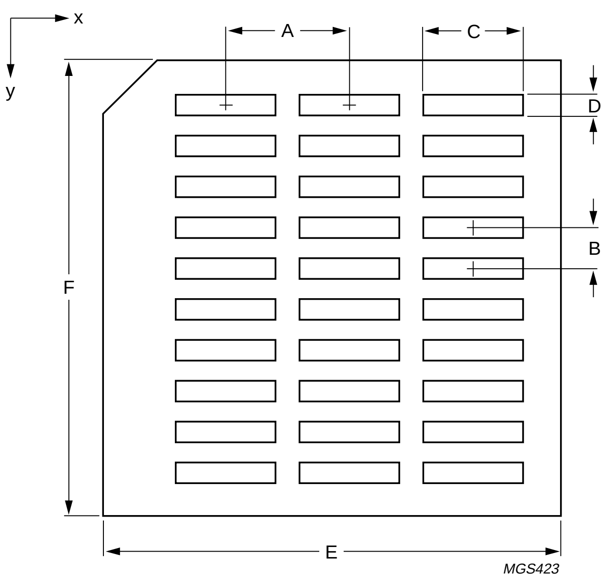


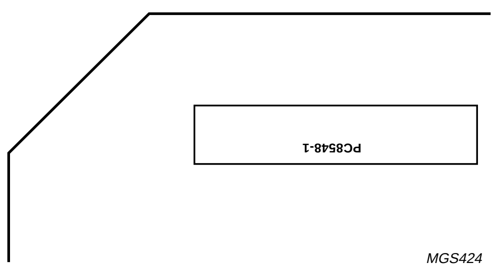
Fig.24 Device protection diagram.

22 TRAY INFORMATION



The dimensions are given in Table 10.

Fig.25 Tray details.



The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray. Refer to the bonding pad location diagram for the orientating and position of the type name on the die surface.

Fig.26 Tray alignment.

Table 10 Dimensions

DIM.	DESCRIPTION	VALUE
A	pocket pitch, x direction	13.77 mm
B	pocket pitch, y direction	4.45 mm
C	pocket width, x direction	11.09 mm
D	pocket width, y direction	2.3 mm
E	tray width, x direction	50.8 mm
F	tray width, x direction	50.8 mm
x	number of pockets in x direction	3
y	number of pockets in y direction	10

23 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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SCA67

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