PDC8RV7284D-(75/102)T-S

64MByte (8M x 72) CMOS, PC/100 Synchronous DRAM Module - ECC (Registered)

General Description

The PDC8RV7284D-(75/102)T-S is a high performance, 64-megabyte synchronous, dynamic RAM module organized as 8M words by 72 bits, in a 168-pin, dual-in-line memory module (DIMM) package.

The module utilizes nine Fujitsu MB81F64842D-(75/102)FN CMOS 8Mx8 synchronous dynamic RAMs in surface mount package (TSOP) on an epoxy laminated substrate. Each device is accompanied by a decoupling capacitor for improved noise immunity.

A 256 Byte Serial EEPROM contains the module configuration information.

Features

- High Density 64MByte
- Cycle Time (CL=3) : 7.5ns (-75), 10ns (-102)
- Cycle Time (CL=2) : 11.5ns (-75), 10ns (-102)
- Low Power: Active 6.9W(-75), 5.9W(-102)
- LVTTL-compatible inputs and outputs
- Separate power and ground planes to improve noise immunity
- Single power supply of 3.3V±0.3V
- Height: 1.500 inch

ABSOLUTE MAXIMUM RATINGS

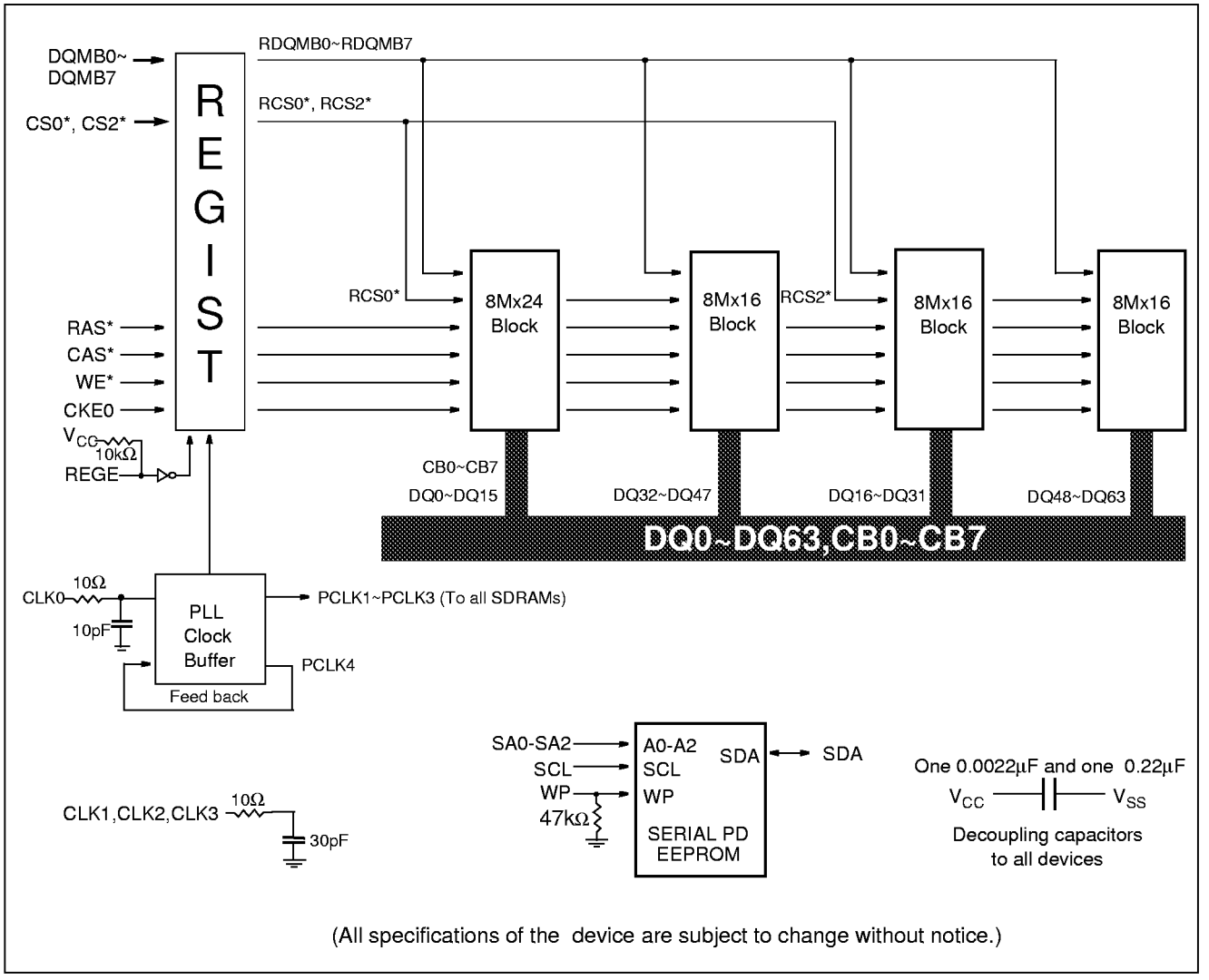
Item	Symbol	Ratings	Unit
Voltage on any pin relative to V_{SS}	V_T	-0.5 to +4.6	V
Power Dissipation	P_T	9.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperate	T_{stg}	-55 to +125	°C
Short Circuit Output Current	I_{OS}	±50	mA

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0 to +70 °C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High voltage	2.0	-	V_{CC}+0.5	V
V_{IL}	Input Low voltage	-0.5	-	0.8	V

Functional Diagram



(All specifications of the device are subject to change without notice.)

Notes:
1. A0~A11and BA0, BA1 to all SDRAMs through registers.
2. REGE, when asserted active high the buffer-register operates in register mode, when deasserted inactive low the buffer-register operates in "real time" buffer mode.
3. Each 8Mx24 Block comprises of three 8Mx8 SDRAMs and each 8Mx16 Block comprises of two 8Mx8 SDRAMs.
4. Registers Block comprises of two registers.
5. Data is terminated using 10 ohm series resistors.
6. RDQMs vs. Data I/Os: RDQMB0 controls DQ0~DQ7
   RDQMB1 controls DQ8~DQ15, CB0~CB7
   RDQMB2 controls DQ16~DQ23
   RDQMB3 controls DQ24~DQ31
   RDQMB4 controls DQ32~DQ39
   RDQMB5 controls DQ40~DQ47
   RDQMB6 controls DQ48~DQ55
   RDQMB7 controls DQ56~DQ63
7. CLK signals are terminated with series resistors and/or padding.
8. Capacitors depending on load per clock.

Pin Name

A0~A11	Addresses	CS0*, CS2*	Chip Select
BA0, BA1	Bank Select Address	WE*	Write Enable
DQ0~DQ63, C0~C7	Data Inputs/Outputs	SA0~SA2	Decode Input
CLK0~CLK3	Clock Inputs	SCL	Serial Clock
RAS*	Row Address Strobes	SDA	Serial Data Input/Output
CAS*	Column Address Strobes	WP	Write Protect
CKE0	Clock Enables	V_{CC}	Power Supply
DQMB0-DQMB7	DQ Mask Enables	V_{SS}	Ground
REGE	Register enable	NC	No Connection

Pin No.	Pin Designation	Pin No.	Pin Designation	Pin No.	Pin Designation	Pin No.	Pin Designation
1	V_{SS}	43	V_{SS}	85	V_{SS}	127	V_{SS}
2	DQ0	44	NC	86	DQ32	128	CKE0
3	DQ1	45	CS2*	87	DQ33	129	NC
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	V_{CC}	48	NC	90	V_{CC}	132	NC
7	DQ4	49	V_{CC}	91	DQ36	133	V_{CC}
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	C2	94	DQ39	136	C6
11	DQ8	53	C3	95	DQ40	137	C7
12	V_{SS}	54	V_{SS}	96	V_{SS}	138	V_{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V_{CC}	101	DQ45	143	V_{CC}
18	V_{CC}	60	DQ20	102	V_{CC}	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	C0	63	NC	105	C4	147	REGE
22	C1	64	V_{SS}	106	C5	148	V_{SS}
23	V_{SS}	65	DQ21	107	V_{SS}	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	V_{CC}	68	V_{SS}	110	V_{CC}	152	V_{SS}
27	WE*	69	DQ24	111	CAS*	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	CS0*	72	DQ27	114	NC	156	DQ59
31	NC	73	V_{CC}	115	RAS*	157	V_{CC}
32	V_{SS}	74	DQ28	116	V_{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V_{SS}	120	A7	162	V_{SS}
37	A8	79	CLK2	121	A9	163	CLK3
38	A10 / AP (Note)	80	NC	122	BA0 (Note)	164	NC
39	BA1 (Note)	81	WP	123	A11	165	SA0
40	V_{CC}	82	SDA	124	V_{CC}	166	SA1
41	V_{CC}	83	SCL	125	CLK1	167	SA2
42	CLK0	84	V_{CC}	126	NC	168	V_{CC}

Note : 1. Address A10 / AP : Initiates Auto Precharge
2. Address BA0,BA1 : Bank select within the SDRAM devices

SERIAL PD INFORMATION

		Function Supported		Hex Value	
Byte	**Function Described**	**-75**	**-102**	**-75**	**-102**
0	# Bytes Written into serial memory at module mfr	128 bytes		80h	
1	Total # bytes of SPD memory device	256 bytes		08h	
2	Fundamental memory type	SDRAM		04h	
3	# Row Address on this assembly	12		0Ch	
4	# Column Addresses on this assembly	9		09h	
5	# Module Banks on this assembly	1		01h	
6	Data Width of this assembly	72 bits		48h	
7	Data Width of this assembly (continued)			00h	
8	Voltage interface standard of this assembly	LVTTL		01h	
9	SDRAM cycle time at CL=3 (tCLK)	7.5ns	10ns	75h	A0h
10	SDRAM Access from Clock at CL=3 (tAC)	6ns		60h	
11	DIMM configuration type	ECC		02h	
12	Refresh Rate/Type	S/R, Normal 15.6 ms		80h	
13	SDRAM Width Primary DRAM	x8		08h	
14	ECC SDRAM Data Width	x8		08h	
15	Min. clock delay, Back to Back Random Column Addresses (ICCD)	1CLK		01h	
16	Burst Length Supported	1, 2, 4, 8 & Full		8Fh	
17	# Banks on each SDRAM device	4		04h	
18	CAS# Latency	2,3		06h	
19	CS# Latency	0		01h	
20	Write Latency	0		01h	
21	SDRAM Module Attribute	Registered/Buffered and PLL		1Fh	
22	SDRAM Device Attribute	Vcc, B/R, S/W, P/A, A/P		0Eh	
23	Min Clock cycle Time at CL=2 (tCLK)	11.5ns	10ns	B5h	A0h
24	Max. Data Access Time from clock at CL=2 (tAC)	7ns	6ns	70h	60h
25	Min Clock cycle Time at CL=1 (tCLK)	N/A		00h	
26	Max. Data Access Time from clock at CL=1 (tAC)	N/A		00h	
27	Min. Row Precharge Time (tRP)	22.5ns	20ns	17h	14h
28	Min. Row Active Delay (tRRD)	15ns	20ns	0Fh	14h
29	Min. RAS to CAS Delay (tRCD)	22.5ns	20ns	17h	14h
30	Min. RAS Pulse Width (tRAS)	45ns	50ns	2Dh	32h
31	Module Bank Density	64MB		10h	
32	Add. & CMD Input Setup Time (tSI)	2ns		20h	
33	Add. & CMD Input Hold Time (tHI)	1ns		10h	
34	Data Input Setup Time (tSI)	2ns		20h	
35	Data Input Hold Time (tHI)	1ns		10h	
36-61	Superset Information			00h	
62	SPD Revision	Rev. 1.2		12h	
63	Checksum for bytes 0-62	JEDEC Calculation		JEDEC Calculation	

SERIAL PD INFORMATION (CONTINUED)

		Function Supported		Hex Value	
Byte	**Function Described**	**-75**	**-102**	**-75**	**-102**
64	Manufacturers JEDEC ID code per JEP-106E	Continuation code		7Fh	
65	Manufacturers JEDEC ID code per JEP-106E	SMART's ID		94h	
66-71	Manufacturers JEDEC ID code per JEP-106E	None		FFh	
72	Manufacturing location	Mfr Specific Data			
73	Manufacturer's Part Number	P		50h	
74	Manufacturer's Part Number	D		44h	
75	Manufacturer's Part Number	C		43h	
76	Manufacturer's Part Number	8		38h	
77	Manufacturer's Part Number	R		52h	
78	Manufacturer's Part Number	V		56h	
79	Manufacturer's Part Number	7		37h	
80	Manufacturer's Part Number	2		32h	
81	Manufacturer's Part Number	8		38h	
82	Manufacturer's Part Number	4		34h	
83	Manufacturer's Part Number	D		44h	
84	Manufacturer's Part Number	7	1	37h	31h
85	Manufacturer's Part Number	5	0	35h	30h
86	Manufacturer's Part Number	T	2	54h	32h
87	Manufacturer's Part Number	S	T	53h	54h
88	Manufacturer's Part Number	None	S	FFh	53h
89	Manufacturer's Part Number	None		FFh	
90	Manufacturer's Part Number	None		FFh	
91	Revision Code	Mfr Specific Data		Mfr Specific Data	
92	Revision Code	None		FFh	
93	Manufacturing Date	DATE		DATE	
94	Manufacturing Date	DATE		DATE	
95-98	Assembly Serial Number	Serial Number		S.No.	
99	Manufacturer Specific Data	S		53h	
100	Manufacturer Specific Data	M		4Dh	
101	Manufacturer Specific Data	A		41h	
102	Manufacturer Specific Data	R		52h	
103	Manufacturer Specific Data	T		54h	
104	Manufacturer Specific Data	M		4Dh	
105	Manufacturer Specific Data	o		6Fh	
106	Manufacturer Specific Data	d		64h	
107	Manufacturer Specific Data	u		75h	
108	Manufacturer Specific Data	l		6Ch	
109	Manufacturer Specific Data	a		61h	
110	Manufacturer Specific Data	r		72h	
111	Manufacturer Specific Data	T		54h	
112	Manufacturer Specific Data	e		65h	
113	Manufacturer Specific Data	c		63h	
114	Manufacturer Specific Data	h		68h	
115	Manufacturer Specific Data	n		6Eh	
116	Manufacturer Specific Data	o		6Fh	
117	Manufacturer Specific Data	l		6Ch	
118	Manufacturer Specific Data	o		6Fh	
119	Manufacturer Specific Data	g		67h	
120	Manufacturer Specific Data	i		69h	
121	Manufacturer Specific Data	e		65h	
122	Manufacturer Specific Data	s		73h	
123	Manufacturer Specific Data	None		FFh	
124	Manufacturer Specific Data	None		FFh	
125	Manufacturer Specific Data	None		FFh	
126	Intel Spec Frequency	100MHz		64h	
127	Intel Spec Detail for 100MHz	1000-1101	1000-1111	8Dh	8Fh
128-255	Open for CPQ Use for Read & Write	None		FFh	

DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted) Notes 1,2

Parameter		Symbol	Conditions	Value		Unit
				Min.	Max.	
Output High Voltage		$V_{OH(DC)}$	I_{OH} = -2mA	2.4	-	V
Output Low Voltage		$V_{OL(DC)}$	I_{OL} = 2mA	-	0.4	V
Input Leakage Current (Any Input)		I_{LI}	0V ≤ V_{IN} ≤ V_{CC}; All other pins not under test = 0V	-90	90	µA
Output Leakage Current		I_{LO}	0V ≤ V_{IN} ≤ V_{CC} D_{out} = Disable	-10	10	µA
Operating Current (Average Power Supply Current)	-75	I_{CC1S}	Burst: Length=4, t_{RC} = min for BL=4, t_{CK} = min. One bank - active, Outputs open, Addresses changed up to 3-times during t_{RC} (min), 0V ≤ V_{in} ≤ V_{CC}	-	1112	mA
	-102			-	1022	
	-75	I_{CC1D}	Burst: Length=4 (each bank), t_{RC} = min for BL=4 (each bank), t_{CK} = min. 2 banks active, Output open, Addresses changed up to 3-times during t_{RC} (min), 0V ≤ V_{in} ≤ V_{CC}	-	1922	mA
	-102			-	1652	
Precharge Standby Current (Power Supply Current)		I_{CC2P}	CKE=V_{IL}, All banks idle, t_{CK}=min, Power down mode, 0V ≤ V_{in} ≤ V_{CC}	-	41	mA
		I_{CC2PS}	CKE=V_{IL}, All banks idle, CLK=H or L, Power down mode, 0V ≤ V_{in} ≤ V_{CC}	-	41	
Precharge Standby Current (Power Supply Current)	-75	I_{CC2N}	CKE=V_{IH}, All banks idle, t_{CK}=min, NOP commands only, Input signals (except to CMD) are changed one time during 3 clock cycles, 0V ≤ V_{in} ≤ V_{CC}	-	257	mA
	-102			-	212	
Precharge Standby Current (Power Supply Current)		I_{CC2NS}	CKE=V_{IH}, All banks idle, CLK=H or L, Input signals are stable, 0V ≤ V_{in} ≤ V_{CC}	-	77	

(Continued)

Parameter		Symbol	Test Condition	Value		Unit
				Min.	Max.	
Active Standby Current (Power Supply Current)		I_{CC3P}	CKE=V_{IL}, Any bank active, t_{CK}=min, 0V ≤ V_{in} ≤ V_{CC}	-	50	mA
		I_{CC3PS}	CKE=V_{IL}, Any bank active, CLK = H or L, 0V ≤ V_{in} ≤ V_{CC}	-	50	mA
Active Standby Current (Power Supply Current)		I_{CC3N}	CKE=V_{IH}, Any bank active, t_{CK}=min, NOP commands only, Input signals (except to CMD) are changed one time during 3 clock cycles, 0V ≤ V_{in} ≤ V_{CC}	-	302	mA
				-	257	
Active Standby Current (Power Supply Current)		I_{CC3NS}	CKE=V_{IH}, Any bank active, CLK = H or L, 0V ≤ V_{in} ≤ V_{CC}	-	122	mA
Burst mode Current (Average Power supply current)	-75	I_{CC4}	t_{CK}=min, Burst length=4, Outputs open, Multiple-banks active, Gapless data, 0V ≤ V_{in} ≤ V_{CC}	-	1562	mA
	-102			-	1292	
Refresh Current #1 (Average Power Supply Current)	-75	I_{CC5}	Auto-refresh; t_{CK}=min, t_{RC}=min, 0V ≤ V_{in} ≤ V_{CC}	-	1562	mA
	-102			-	1472	
Refresh Current #2 (Average Power Supply Current)		I_{CC6}	Self-refresh; t_{CK}=min, CKE ≤ 0.2V, 0V ≤ V_{in} ≤ V_{CC}	-	41	mA

†CL = CAS* Latency

Notes: 1. I_{CC} depends on the output termination or load conditions, clock cycle rate, and signal clocking rate; The specified values are obtained with the output open and no termination register.

2. An initial pause (DESL or NOP) of 200 μs is required after power-up followed by a minimum of eight Auto-refresh cycles.

CAPACITANCE

(TA =+25°C, VCC = 3.3V±0.3V)

Parameter	Symbol	Max.	Unit	Note
Input Capacitance (Address, WE*, CKE, RAS*, CAS*)	C_{I1}	18	pF	1
Input Capacitance (DQMBs)	C_{I2}	18	pF	1
Input Capacitance (CS0*)	C_{I3}	18	pF	1
Input Capacitance (CS2*)	C_{I4}	18	pF	1
Input Capacitance (CLK0)	C_{I5}	32	pF	1
Input Capacitance (CLK1~CLK3)	C_{I6}	35	pF	1
Input/Output Capacitance (DQ0~DQ63)	$C_{I/O}$	17	pF	1, 2

Notes: 1. Capacitance is measured with Boonton Meter or effective capacitance method.
2. CAS* - V_{IH} to disable D_{out}.

AC CHARACTERISTICS: MB81F64842D-(75/102)

(At recommended operating conditions unless otherwise noted) Notes 2,3,4

Parameter		Symbol	Unit	-75		-102		Notes
				Min.	Max.	Min.	Max.	
Clock Period	CAS Latency=2	t_{CK2}	ns	11.5	-	10	-	
	CAS Latency=3	t_{CK3}		7.5	-	10	-	
Clock High Time		t_{CH}	ns	2.5	-	3	-	
Clock Low Time		t_{CL}	ns	2.5	-	3	-	
Input Setup Time		t_{SI}	ns	2	-	2	-	
Input Hold Time		t_{HI}	ns	1	-	1	-	
Access time from Clock (t_{CK}=min)	CAS Latency=2	t_{AC2}	ns	-	7	-	6	5,6
	CAS Latency=3	t_{AC3}		-	6	-	6	
Output In Low-Z		t_{LZ}	ns	0	-	0	-	
Output in High-Z	CAS Latency=2	t_{HZ2}	ns	3	7	3	6	7
	CAS Latency=3	t_{HZ3}		3	6	3	6	
Output Hold Time	CAS Latency=2	t_{OH}	ns	3	-	3	-	
	CAS Latency=3			3	-	3	-	
Time between Auto-Refresh command Interval		t_{REFI}	us	-	15.6	-	15.6	
Time between Refresh		t_{REF}	ms	-	64	-	64	
Transition Time		t_T	ns	0.5	2	0.5	2	
CKE Set Up time for Power Down Exit		t_{CKSP}	ns	2.5	-	3	-	

BASE VALUES FOR CLOCK COUNT/LATENCY: MB81F64842D-(75/102)

Parameter		Symbol	Unit	-75		-102		Notes
				Min.	Max.	Min.	Max.	
$\overline{RAS}$ Cycle Time		t_{RC}	ns	67.5	-	70	-	8
$\overline{RAS}$ Precharge Time		t_{RP}	ns	22.5	-	20	-	
$\overline{RAS}$ Active Time		t_{RAS}	ns	45	110000	50	110000	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time		t_{RCD}	ns	22.5	-	20	-	9
Write Recovery Time		t_{WR}	ns	7.5	-	10	-	
Data-in to Precharge Lead Time		t_{DPL}	ns	7.5	-	10	-	
Data-in to Active/Refresh command period	CAS Latency=2	t_{DAL2}	ns	1cyc+t_{RP}	-	1cyc+t_{RP}	-	
	CAS Latency=3	t_{DAL3}		2cyc+t_{RP}	-	2cyc+t_{RP}	-	
Mode Register set cycle Time		t_{RSC}	ns	15	-	20	-	
$\overline{RAS}$ to $\overline{RAS}$ Bank Active Delay Time		t_{RRD}	ns	15	-	20	-	

CLOCK COUNT FORMULA

(Note 10)

$$\text{Clock} \geq \frac{\text{Base Value}}{\text{Clock Period}} \quad \text{(Round off a whole number)}$$

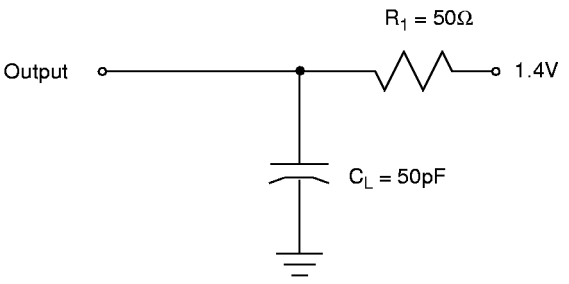
LATENCY-FIXED VALUES: MB81F64842D-(75/102)

(The latency values on these parameters are fixed regardless of clock period)

Parameter		Symbol	Unit	-75	-102	Notes
CKE to Clock Disable		I_{CKE}	cycle	1	1	
DQM to Output in High-Z		I_{DQZ}	cycle	2	2	
DQM to Input Data Delay		I_{DQD}	cycle	0	0	
Last Output to Write Command Delay		I_{OWD}	cycle	2	2	
Write Command to Input Data Delay		I_{DWD}	cycle	0	0	
Precharge to Output in High-Z Delay	CL = 2	I_{ROH2}	cycle	2	2	
	CL = 3	I_{ROH3}		3	3	
Burst Stop Command to Output in High-Z Delay	CL = 2	I_{BSH2}	cycle	2	2	
	CL = 3	I_{BSH3}		3	3	
$\overline{CAS}$ to $\overline{CAS}$ Delay (min)		I_{CCD}	cycle	1	1	
$\overline{CAS}$ Bank Delay (min)		I_{CBD}	cycle	1	1	

Notes:
1. I_{CC} depends on the output termination or load conditions, clock cycle rate, and signal clocking rate; The specified values are obtained with the output open and no termination register.
2. An initial pause (DESL or NOP) of 200 µs is required after power-up followed by a minimum of eight Auto-refresh cycles.
3. AC characteristics assume t_T = 1 ns and 50 pF of capacitive load.
4. 1.4 V is the reference level for measuring timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max).
5. Assumes t_{RCD} is satisfied.
6. t_{AC} also specifies the access time at burst mode.
7. Specified where output buffer is no longer driven.
8. Actual clock count of t_{RC} (I_{RC}) will be sum of clock count of t_{RAS} (I_{RAS}) and t_{RP} (I_{RP}).
9. Operation within the(t_{RCD}) (min) ensures that access time is determined by (t_{RCD}) (min) + (t_{AC}) (max); If t_{RCD} is greater than the specified t_{RCD} (min), access time is determined by t_{AC}.
10. All base values are measured from the clock edge at the command input to the clock edge for the next command input. All clock counts are

Fig. 4 - EXAMPLE OF AC TEST LOAD CIRCUIT

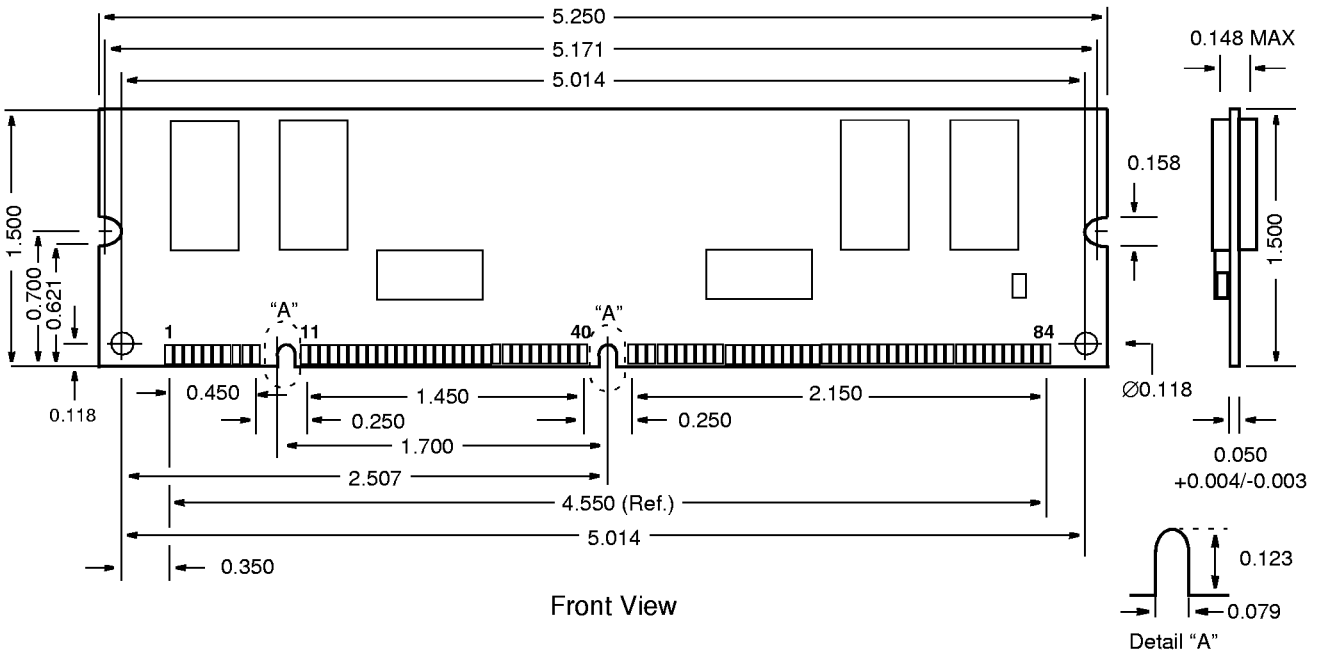


LVTTL

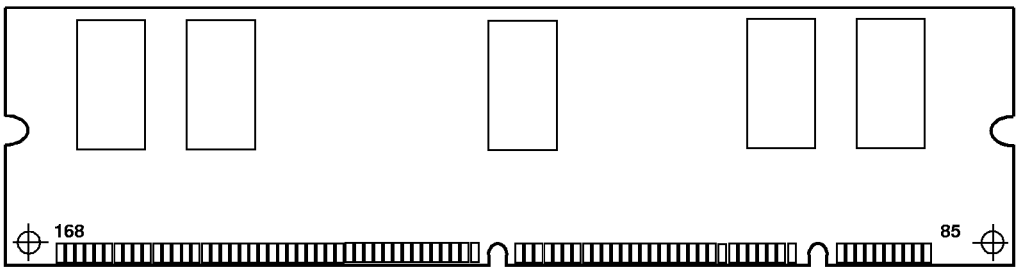
Note: AC characteristics are measured in this condition. This load circuits are not applicable for V_{OH} and V_{OL}.

Physical Dimensions

168-pin (84x2) 3.3V DIMM



Front View



Back View

Notes: 1. All dimensions are in inches.
2. Pin 85 is behind pin - on the back side.

Ordering Information

P D C 8 R V 72 8 4 D -102T -S

(1) (2) (3) (4) (5) (6) (7) (8) (9) (10) (11) (12) (13)

(1) **Memory Type**
S : SDRAM (PC/66)
G : SGRAM
P : SDRAM-Fast (PC/100)

(2) **Module Shape**
S : SIMM
D : DIMM
O : Small Outline DIMM

(3) **Module Pin Count**
A : 72-pin
B : 144-pin
C : 168-pin
D : 200-pin

(4) **Word Depth**
1 : 1M
2 : 2M
4 : 4M
8 : 8M
16 : 16M
256 : 256K
512 : 512K

(5) **Buffer Type**
B : Buffered
U : Unbuffered
R : Registered

(6) **Operating Voltage & Power Consumption**
V : 3.3V & LVTTL & Standard Power
L : 3.3V & LVTTL & Low Power
S : 3.3V & SSTL & Standard Power

(7) **Data Width**
(ex. 64=x64, 72=x72 etc.)

(8) **Device Configuration**
4 : x4
8 : x8
1 : x16
3 : x32

(9) **Refresh**
2 : 2krf
4 : 4krf
8 : 8krf

(10) **Module Revision / Applied "Standard" *1**
Blank : Rev. 0
A : Rev. 1
B : Rev. 2 (etc.)

*1 When DRAM device or PCB is revised, the revision is changed

(11) **Clock Frequency**
SDRAM
100 : 100Mhz

SDRAM-Fast (100Mhz, PC/100)
75 :133MHz (CL=3; t_{RCD}=3; t_{RP}=3)
102 : 100MHz (CL=2; t_{RCD}=2; t_{RP}=2)
103 :100MHz (CL=3; t_{RCD}=2; t_{RP}=2)
10 : 100MHz (CL=3; t_{RCD}=3; t_{RP}=3)

(12) **Package of Component**
T : TSOP

(13) **Assembly & Test Site**
S : Smart Modular Technologies

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