NEC

MOS INTEGRATED CIRCUIT
μPD4264800, 4265800

64 M-BIT DYNAMIC RAM
8 M-WORD BY 8-BIT, FAST PAGE MODE

Description

The μPD4264800, 4265800 are 8,388,608 words by 8 bits dynamic CMOS RAMs. The fast page mode capability realize high speed access and low power consumption.

These are packaged in 32-pin plastic TSOP(II) and 32-pin plastic SOJ.

Features

- 8,388,608 words by 8 bits organization
- Fast access and cycle time
- Single +3.3 V ± 0.3 V power supply

Part number	Power consumption		Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
	Active (MAX.)	Standby(MAX.)			
μPD4264800-A50	378 mW	1.80 mW (CMOS level input)	50 ns	90 ns	35 ns
μPD4265800-A50	486 mW				
μPD4264800-A60	342 mW		60 ns	110 ns	40 ns
μPD4265800-A60	414 mW				
μPD4264800-A70	306 mW		70 ns	130 ns	45 ns
μPD4265800-A70	378 mW				
μPD4264800-A80	270 mW		80 ns	150 ns	50 ns
μPD4265800-A80	342 mW				

- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh

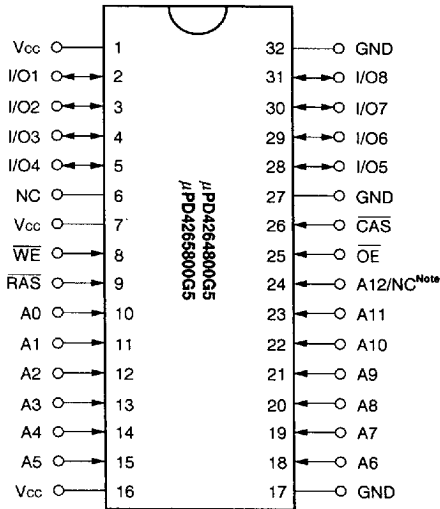| Part number	Row address	Column address	Refresh	Refresh cycle
μPD4264800	A0 - A12	A0 - A9	$\overline{RAS}$ only refresh, Normal read/write	8,192 cycles/64 ms
			$\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh	4,096 cycles/64 ms
μPD4265800	A0 - A11	A0 - A10	$\overline{RAS}$ only refresh, Normal read/write, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh	4,096 cycles/64 ms

The information in this document is subject to change without notice.

Ordering Information

Part number	Access time (MAX.)	Package	Refresh
μPD4264800G5-A50	50 ns	32-pin plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD4264800G5-A60	60 ns		
μPD4264800G5-A70	70 ns		
μPD4264800G5-A80	80 ns		
μPD4264800LE-A50	50 ns	32-pin plastic SOJ (400 mil)	
μPD4264800LE-A60	60 ns		
μPD4264800LE-A70	70 ns		
μPD4264800LE-A80	80 ns		
μPD4265800G5-A50	50 ns	32-pin plastic TSOP (II) (400 mil)	
μPD4265800G5-A60	60 ns		
μPD4265800G5-A70	70 ns		
μPD4265800G5-A80	80 ns		
μPD4265800LE-A50	50 ns	32-pin plastic SOJ (400 mil)	
μPD4265800LE-A60	60 ns		
μPD4265800LE-A70	70 ns		
μPD4265800LE-A80	80 ns		

6427525 0091423 55T

Pin Configurations (Marking Side)

32-pin Plastic TSOP (II) (400 mil)

Vcc	1	32	GND
I/O1	2	31	I/O8
I/O2	3	30	I/O7
I/O3	4	29	I/O6
I/O4	5	28	I/O5
NC	6	27	GND
Vcc	7	26	$\overline{CAS}$
$\overline{WE}$	8	25	$\overline{OE}$
$\overline{RAS}$	9	24	A12/NC[Note]
A0	10	23	A11
A1	11	22	A10
A2	12	21	A9
A3	13	20	A8
A4	14	19	A7
A5	15	18	A6
Vcc	16	17	GND

µPD4264800G5
µPD4265800G5

32-pin Plastic SOJ (400 mil)

Vcc	1	32	GND
I/O1	2	31	I/O8
I/O2	3	30	I/O7
I/O3	4	29	I/O6
I/O4	5	28	I/O5
NC	6	27	GND
Vcc	7	26	$\overline{CAS}$
$\overline{WE}$	8	25	$\overline{OE}$
$\overline{RAS}$	9	24	A12/NC[Note]
A0	10	23	A11
A1	11	22	A10
A2	12	21	A9
A3	13	20	A8
A4	14	19	A7
A5	15	18	A6
Vcc	16	17	GND

µPD4264800LE
µPD4265800LE
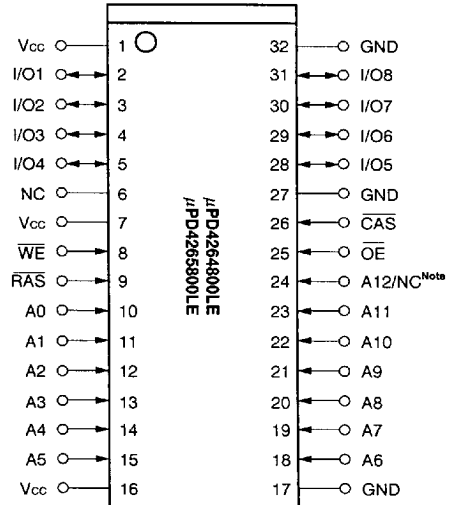
Note A12 ... µPD4264800
NC ... µPD4265800

A0 to A12	:	Address Inputs
I/O1 to I/O8	:	Data Inputs/Outputs
$\overline{RAS}$	:	Row Address Strobe
$\overline{CAS}$	:	Column Address Strobe
$\overline{WE}$	:	Write Enable
$\overline{OE}$	:	Output Enable
Vcc	:	Power Supply
GND	:	Ground
NC	:	No Connection

6427525 0091424 496

Input/Output Pin Functions

The μPD4264800, 4265800 have input pins $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, Address[Note] and input/output pins I/O1 to I/O8.

Pin name	Input/Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)	Input	$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to Ax[Note] (Address inputs)	Input	Address bus. Input total 23-bit of address signal, upper bits and lower bits[Note] in sequence (address multiplex method). Therefore, one word is selected from 8,388,608-word by 8-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O8 (Data inputs/outputs)	Input/Output	8-bit data bus. I/O1 to I/O8 are used to input/output data.

Note

Part number	Address inputs	Upper bits	Lower bits
μPD4264800	A0-A12	13	10
μPD4265800	A0-A11	12	11

6427525 0091425 322

Electrical Specifications (Preliminary)

- All voltages are referenced to GND.
- After power up(Vcc ≥ Vcc(MIN.)), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−0.5 to +4.6	V
Supply voltage	V_{CC}		−0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution **Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.**

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

6427525 0091426 269

DC Characteristics (Recommended operating conditions unless otherwise noted)

[μPD4264800]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC} = t_{RC\,(MIN.)}$ $I_O = 0$ mA	$t_{RAC} = 50$ ns		105	mA	1, 2, 3
			$t_{RAC} = 60$ ns		95		
			$t_{RAC} = 70$ ns		85		
			$t_{RAC} = 80$ ns		75		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\,(MIN.)}$, $I_O = 0$ mA			1.0	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V, $I_O = 0$ mA			0.5		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS} \geq V_{IH\,(MIN.)}$ $t_{RC} = t_{RC\,(MIN.)}$, $I_O = 0$ mA	$t_{RAC} = 50$ ns		105	mA	1, 2, 3 ,4
			$t_{RAC} = 60$ ns		95		
			$t_{RAC} = 70$ ns		85		
			$t_{RAC} = 80$ ns		75		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\,(MAX.)}$, $\overline{CAS}$ cycling $t_{PC} = t_{PC\,(MIN.)}$, $I_O = 0$ mA	$t_{RAC} = 50$ ns		85	mA	1, 2, 5
			$t_{RAC} = 60$ ns		75		
			$t_{RAC} = 70$ ns		65		
			$t_{RAC} = 80$ ns		55		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ cycling $t_{RC} = t_{RC\,(MIN.)}$ $I_O = 0$ mA	$t_{RAC} = 50$ ns		135	mA	1, 2
			$t_{RAC} = 60$ ns		115		
			$t_{RAC} = 70$ ns		105		
			$t_{RAC} = 80$ ns		95		
Input leakage current	$I_{I\,(L)}$	$V_I = 0$ to 3.6 V All other pins not under test = 0 V		−5	+5	μA	
Output leakage current	$I_{O\,(L)}$	$V_O = 0$ to 3.6 V Output is disabled (Hi-Z)		−5	+5	μA	
High level output voltage	V_{OH}	$I_O = -2.0$ mA		2.4		V	
Low level output voltage	V_{OL}	$I_O = +2.0$ mA			0.4	V	

6427525 0091427 1T5

[μPD4265800]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC} = t_{RC \, (MIN.)}$ $I_O = 0$ mA	$t_{RAC} = 50$ ns		135	mA	1, 2, 3
			$t_{RAC} = 60$ ns		115		
			$t_{RAC} = 70$ ns		105		
			$t_{RAC} = 80$ ns		95		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH \, (MIN.)}$, $I_O = 0$ mA			1.0	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V, $I_O = 0$ mA			0.5		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS} \geq V_{IH \, (MIN.)}$ $t_{RC} = t_{RC \, (MIN.)}$, $I_O = 0$ mA	$t_{RAC} = 50$ ns		135	mA	1, 2, 3 ,4
			$t_{RAC} = 60$ ns		115		
			$t_{RAC} = 70$ ns		105		
			$t_{RAC} = 80$ ns		95		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL \, (MAX.)}$, $\overline{CAS}$ cycling $t_{PC} = t_{PC \, (MIN.)}$, $I_O = 0$ mA	$t_{RAC} = 50$ ns		85	mA	1, 2, 5
			$t_{RAC} = 60$ ns		75		
			$t_{RAC} = 70$ ns		65		
			$t_{RAC} = 80$ ns		55		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ cycling $t_{RC} = t_{RC \, (MIN.)}$ $I_O = 0$ mA	$t_{RAC} = 50$ ns		135	mA	1, 2
			$t_{RAC} = 60$ ns		115		
			$t_{RAC} = 70$ ns		105		
			$t_{RAC} = 80$ ns		95		
Input leakage current	$I_{I \, (L)}$	$V_I = 0$ to 3.6 V All other pins not under test = 0 V		−5	+5	μA	
Output leakage current	$I_{O \, (L)}$	$V_O = 0$ to 3.6 V Output is disabled (Hi-Z)		−5	+5	μA	
High level output voltage	V_{OH}	$I_O = -2.0$ mA		2.4		V	
Low level output voltage	V_{OL}	$I_O = +2.0$ mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL \, (MAX.)}$ and $\overline{CAS} \geq V_{IH \, (MIN.)}$.

4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
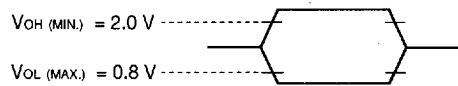
AC Characteristics (Recommended Operating Conditions unless otherwise noted)
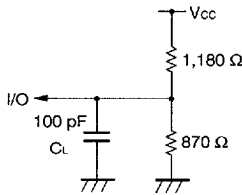
AC Characteristics Test Conditions

(1) Input timing specification

$V_{IH\ (MIN.)} = 2.0\ V$

$V_{IL\ (MAX.)} = 0.8\ V$

$t_T = 5\ ns$ $t_T = 5\ ns$
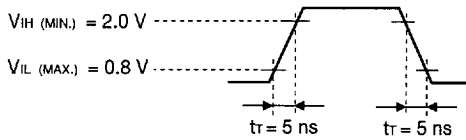
(2) Output timing specification

$V_{OH\ (MIN.)} = 2.0\ V$

$V_{OL\ (MAX.)} = 0.8\ V$

(3) Output load condition

V_{CC}

$1,180\ \Omega$

I/O

$100\ pF$
C_L

$870\ \Omega$

Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	t_{RC}	90	–	110	–	130	–	150	–	ns	
$\overline{RAS}$ precharge time	t_{RP}	30	–	40	–	50	–	60	–	ns	
$\overline{CAS}$ precharge time	t_{CPN}	8	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10,000	15	10,000	18	10,000	20	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	13	–	15	–	18	–	20	–	ns	
$\overline{CAS}$ hold time	t_{CSH}	50	–	60	–	70	–	80	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	37	20	45	20	52	25	60	ns	1
$\overline{RAS}$ to column address delay time	t_{RAD}	13	25	15	30	15	35	17	40	ns	1
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	5	–	ns	2
Row address setup time	t_{ASR}	0	–	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	8	–	10	–	10	–	12	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	13	–	15	–	15	–	15	–	ns	
$\overline{OE}$ lead time referenced to $\overline{RAS}$	t_{OES}	0	–	0	–	0	–	0	–	ns	
$\overline{CAS}$ to data setup time	t_{CLZ}	0	–	0	–	0	–	0	–	ns	
$\overline{OE}$ to data setup time	t_{OLZ}	0	–	0	–	0	–	0	–	ns	
$\overline{OE}$ to data delay time	t_{OED}	10	–	13	–	15	–	15	–	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	ns	
Refresh time	t_{REF}	–	64	–	64	–	64	–	64	ms	

6427525 0091429 T78

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\,(MAX.)}$ and $t_{RCD} \leq t_{RCD\,(MAX.)}$	$t_{RAC\,(MAX.)}$	$t_{RAC\,(MAX.)}$
$t_{RAD} > t_{RAD\,(MAX.)}$ and $t_{RCD} \leq t_{RCD\,(MAX.)}$	$t_{AA\,(MAX.)}$	$t_{RAD} + t_{AA\,(MAX.)}$
$t_{RCD} > t_{RCD\,(MAX.)}$	$t_{CAC\,(MAX.)}$	$t_{RCD} + t_{CAC\,(MAX.)}$

$t_{RAD\,(MAX.)}$ and $t_{RCD\,(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\,(MAX.)}$ and $t_{RCD} \geq t_{RCD\,(MAX.)}$ will not cause any operation problems.

2. $t_{CRP\,(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{RAS}$	t_{RAC}	–	50	–	60	–	70	–	80	ns	1
Access time from $\overline{CAS}$	t_{CAC}	–	13	–	15	–	18	–	20	ns	1
Access time from column address	t_{AA}	–	25	–	30	–	35	–	40	ns	1
Access time from $\overline{OE}$	t_{OEA}	–	13	–	15	–	18	–	20	ns	
Column address lead time referenced to $\overline{RAS}$	t_{RAL}	25	–	30	–	35	–	40	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	0	– ,	0	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	0	–	ns	2
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	10	0	13	0	15	0	15	ns	3
Output buffer turn-off delay time from $\overline{CAS}$	t_{OFF}	0	10	0	13	0	15	0	15	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\,(MAX.)}$ and $t_{RCD} \leq t_{RCD\,(MAX.)}$	$t_{RAC\,(MAX.)}$	$t_{RAC\,(MAX.)}$
$t_{RAD} > t_{RAD\,(MAX.)}$ and $t_{RCD} \leq t_{RCD\,(MAX.)}$	$t_{AA\,(MAX.)}$	$t_{RAD} + t_{AA\,(MAX.)}$
$t_{RCD} > t_{RCD\,(MAX.)}$	$t_{CAC\,(MAX.)}$	$t_{RCD} + t_{CAC\,(MAX.)}$

$t_{RAD\,(MAX.)}$ and $t_{RCD\,(MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\,(MAX.)}$ and $t_{RCD} \geq t_{RCD\,(MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH\,(MIN.)}$ or $t_{RRH\,(MIN.)}$ should be met in read cycles.

3. $t_{OFF\,(MAX.)}$ and $t_{OEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

6427525 0091430 79T

619

Write Cycle

Parameter	Symbol	tRAC = 50 ns		tRAC = 60 ns		tRAC = 70 ns		tRAC = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	twCH	8	–	10	–	10	–	15	–	ns	1
$\overline{WE}$ pulse width	twP	8	–	10	–	10	–	15	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	tRWL	13	–	15	–	15	–	15	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	tCWL	13	–	15	–	15	–	15	–	ns	
$\overline{WE}$ setup time	twCS	0	–	0	–	0	–	0	–	ns	2
$\overline{OE}$ hold time	tOEH	0	–	0	–	0	–	0	–	ns	
Data-in setup time	tDS	0	–	0	–	0	–	0	–	ns	3
Data-in hold time	tDH	10	–	10	–	15	–	15	–	ns	3

Notes 1. twP (MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, twCH (MIN.) should be met.

2. If twCS ≥ twCS (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. tDS (MIN.) and tDH (MIN.) are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	tRAC = 50 ns		tRAC = 60 ns		tRAC = 70 ns		tRAC = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	tRWC	128	–	153	–	175	–	195	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	70	–	83	–	95	–	105	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	tCWD	33	–	38	–	43	–	45	–	ns	1
Column address to $\overline{WE}$ delay time	tAWD	45	–	53	–	60	–	65	–	ns	1

Note 1. If twCS ≥ twCS (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If tRWD ≥ tRWD (MIN.), tCWD ≥ tCWD (MIN.), tAWD ≥ tAWD (MIN.) and tCPWD ≥ tCPWD (MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.
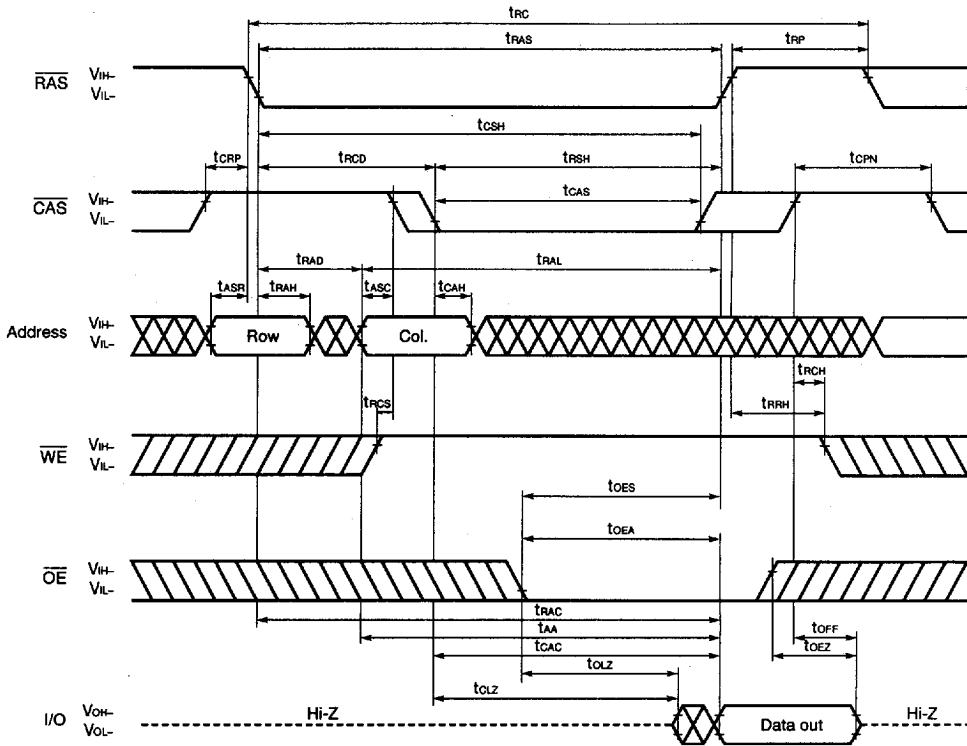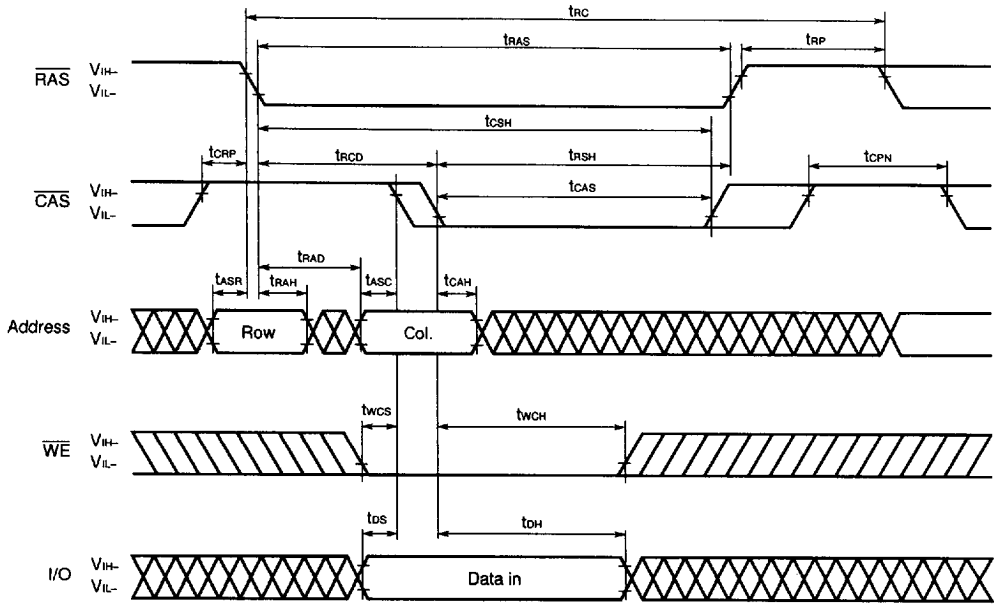
6427525 0091431 626

Fast Page Mode

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Fast page mode cycle time	t_{PC}	35	–	40	–	45	–	50	–	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	–	30	–	35	–	40	–	45	ns	
$\overline{RAS}$ pulse width	t_{RASP}	50	125,000	60	125,000	70	125,000	80	125,000	ns	
$\overline{CAS}$ precharge time	t_{CP}	8	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30	–	35	–	40	–	45	–	ns	
Read modify write cycle time	t_{PRWC}	73	–	83	–	90	–	95	–	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	50	–	58	–	65	–	70	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS}$ (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD}$ (MIN.), $t_{CWD} \geq t_{CWD}$ (MIN.), $t_{AWD} \geq t_{AWD}$ (MIN.) and $t_{CPWD} \geq t_{CPWD}$ (MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Refresh Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ setup time	t_{CSR}	5	–	5	–	5	–	5	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	10	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5	–	5	–	5	–	5	–	ns	
$\overline{WE}$ setup time	t_{WSR}	10	–	10	–	10	–	10	–	ns	
$\overline{WE}$ hold time	t_{WHR}	15	–	15	–	15	–	15	–	ns	

6427525 0091432 562

621

Read Cycle

6427525 0091433 4T9

Early Write Cycle

Remark $\overline{OE}$: Don't care
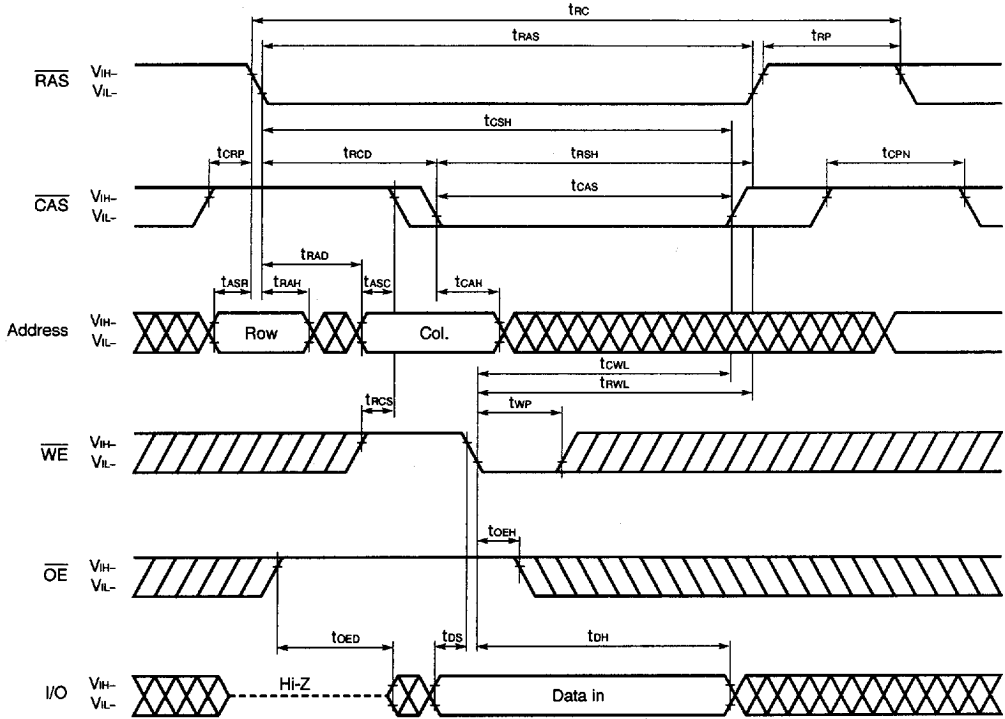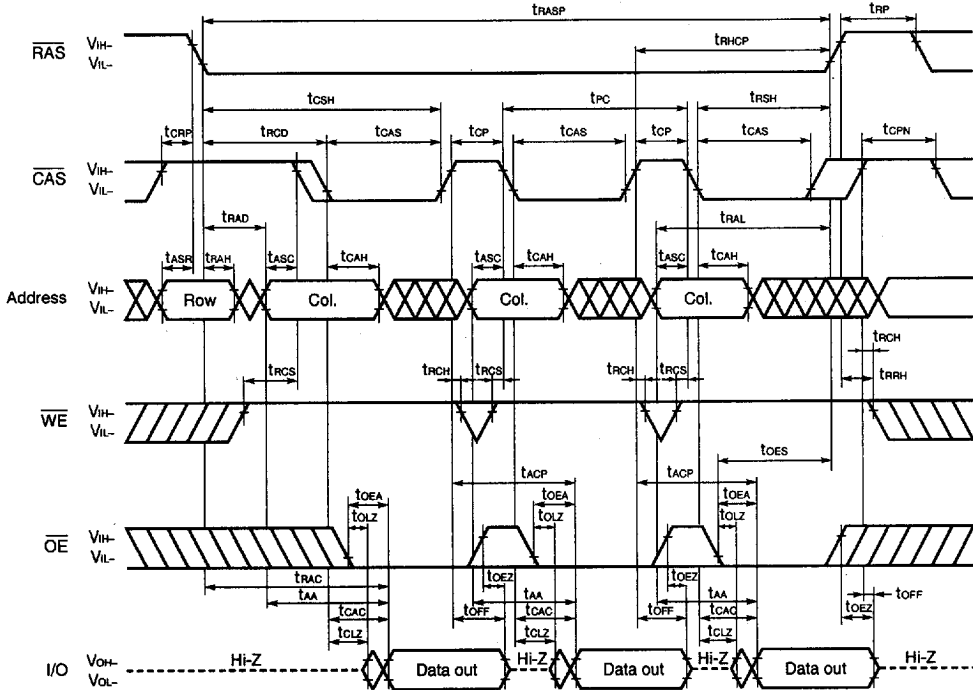
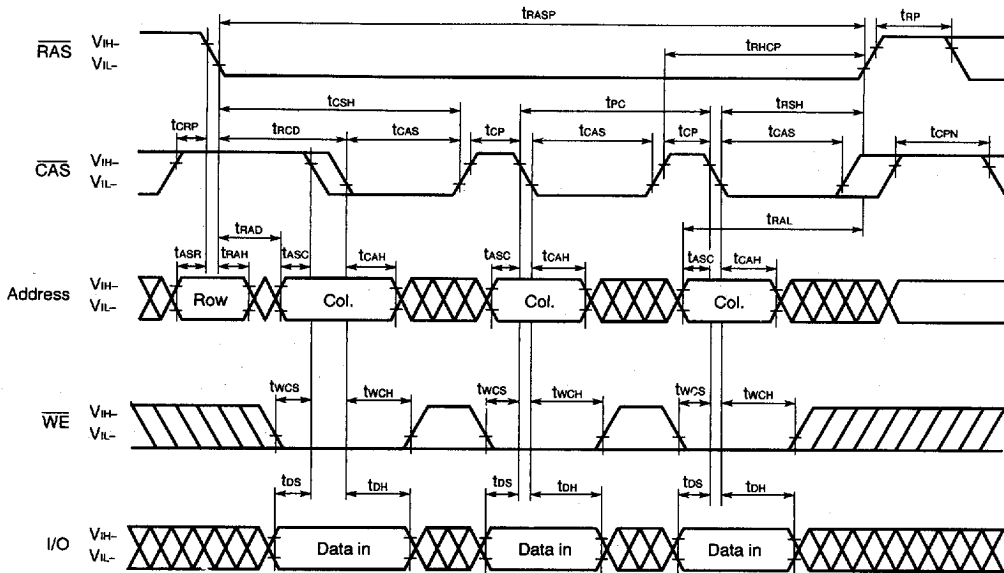**Late Write Cycle**

■ 6427525 0091435 271 ■
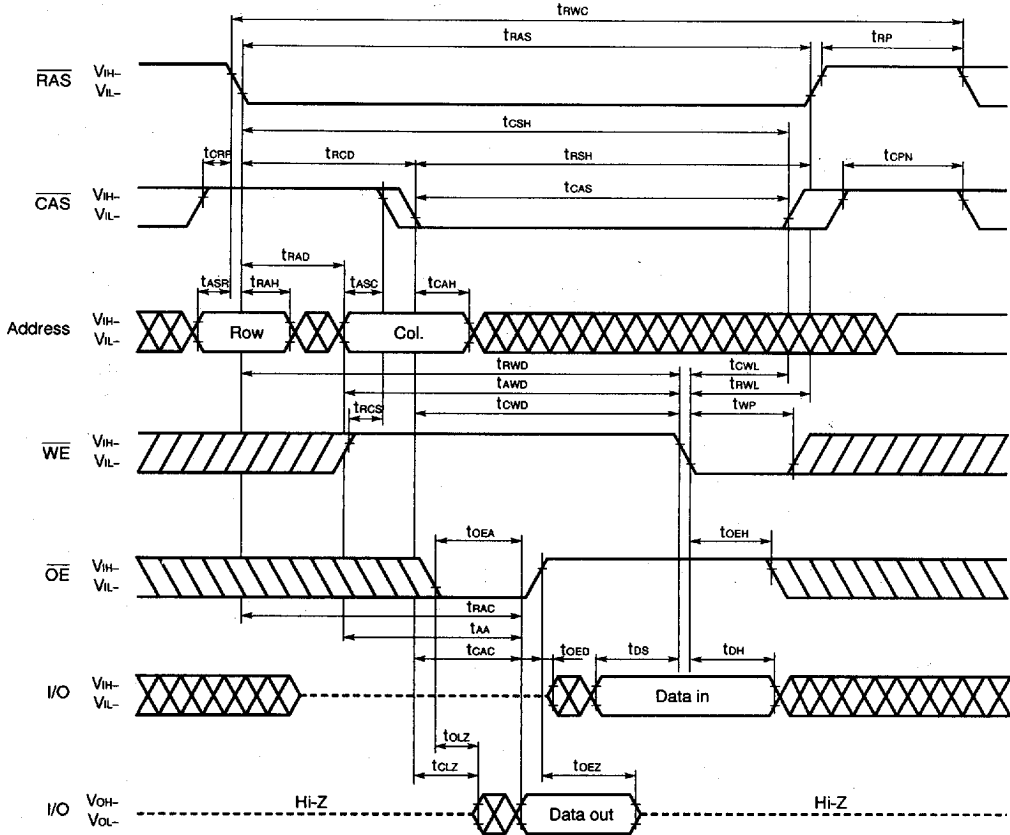
Read Modify Write Cycle
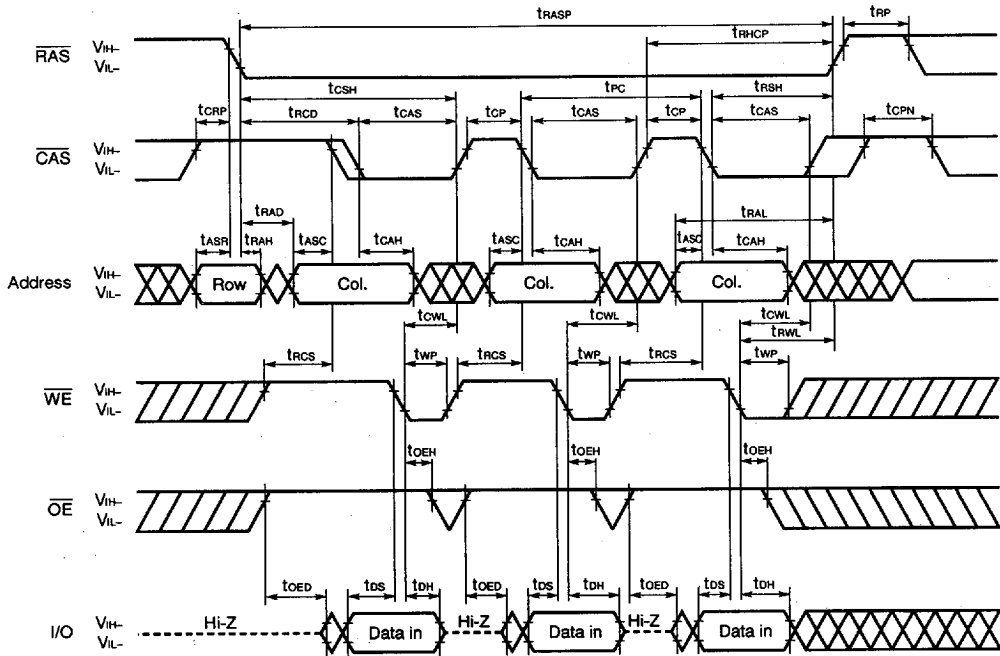
Fast Page Mode Read Cycle

Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Early Write Cycle

Remarks 1. $\overline{OE}$: Don't care

2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Late Write Cycle

Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

■ 6427525 0091439 917 ■

Fast Page Mode Read Modify Write Cycle

Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle
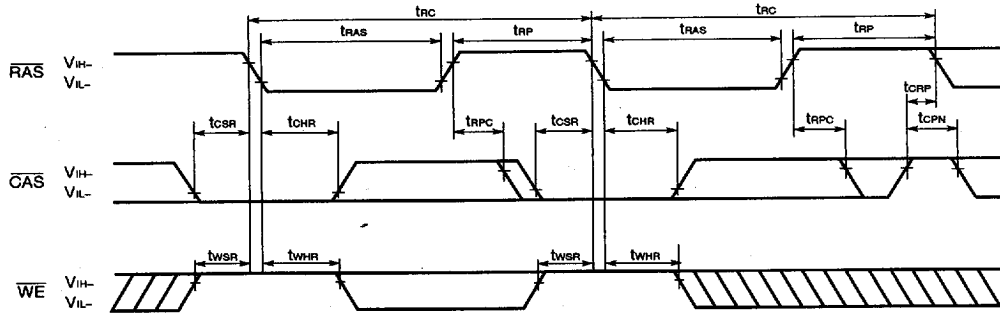
Remark Address, $\overline{\text{OE}}$: Don't care   I/O: Hi-Z

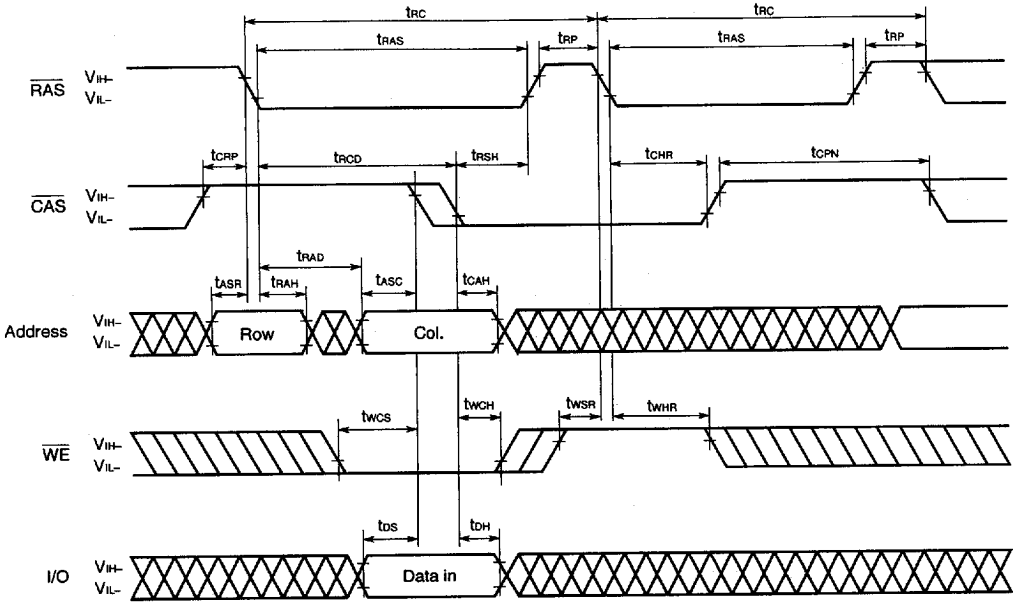## $\overline{\text{RAS}}$ Only Refresh Cycle
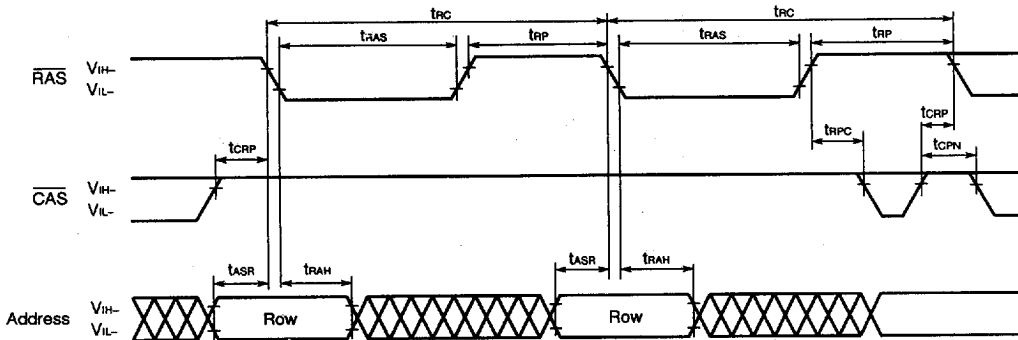
Remark $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care   I/O: Hi-Z
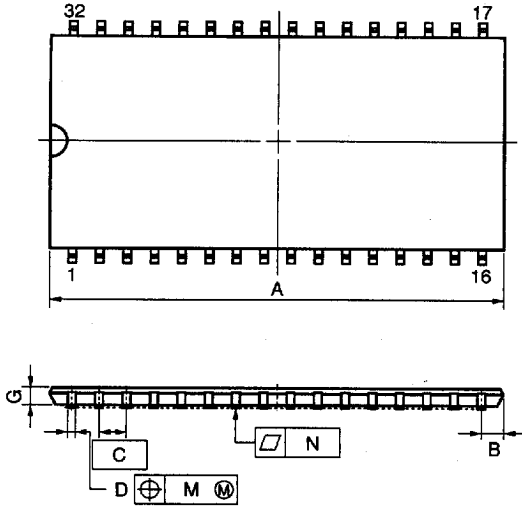
■ 6427525 0091441 575 ■

Hidden Refresh Cycle (Read)
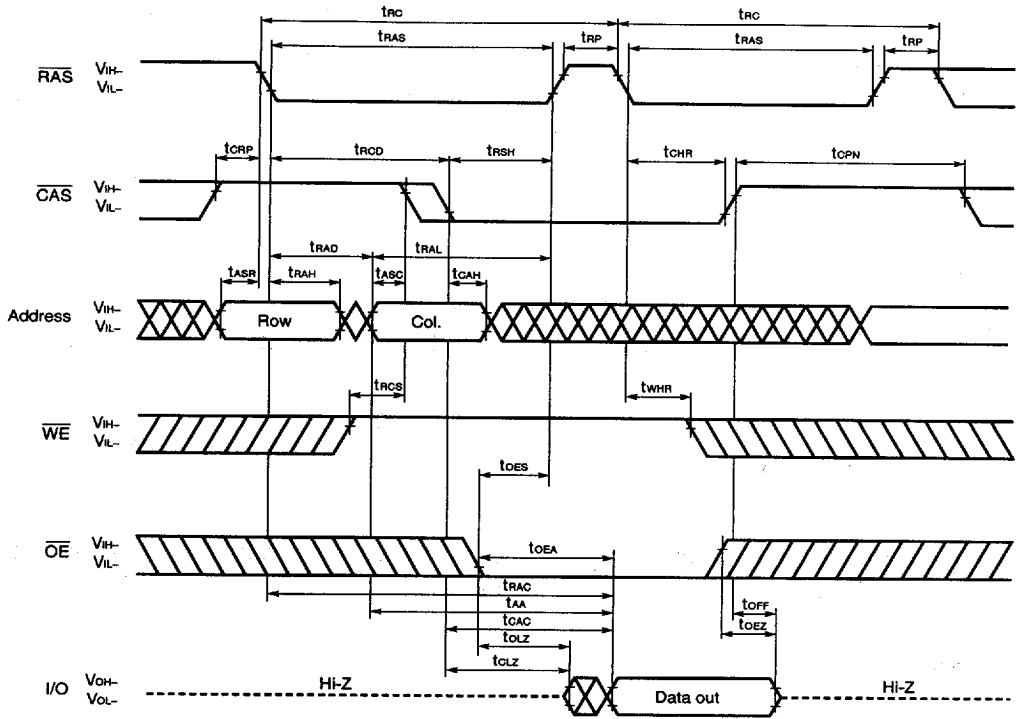
Hidden Refresh Cycle (Write)

Remark $\overline{OE}$: Don't care

■ 6427525 0091443 348 ■

Package Drawings

32PIN PLASTIC TSOP(II) (400 mil)
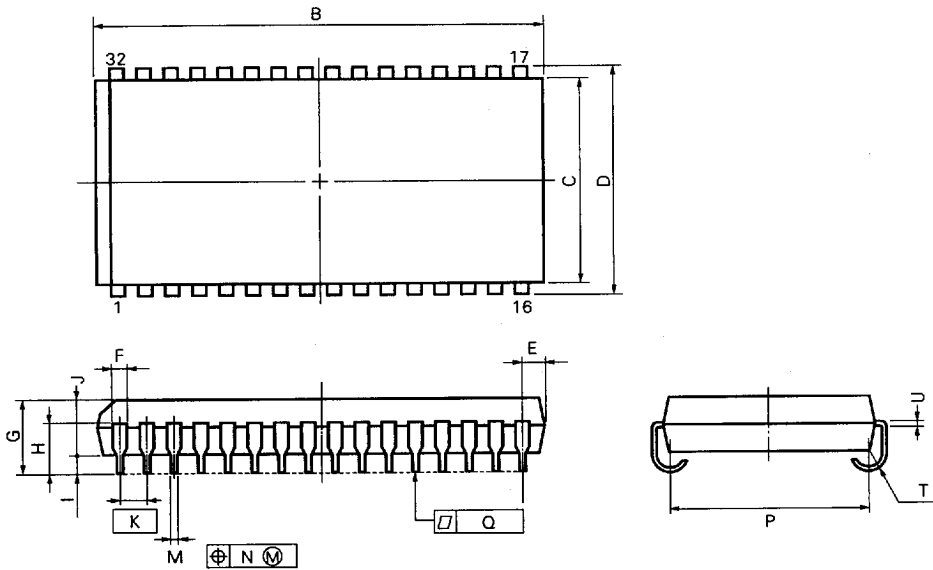
detail of lead end
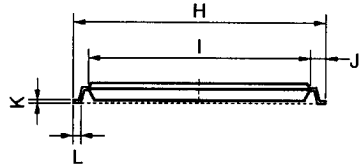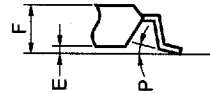
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.075 MAX.	0.043 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.42^{+0.08}_{-0.07}$	0.017±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S32G5-50-7JD2

6427525 0091444 284

32 PIN PLASTIC SOJ (400 mil)

P32LE-400A

NOTE
Each lead centerline is located within 0.12 mm
(0.005 inch) of its true position (T.P.) at maxi-
mum material condition.

ITEM	MILLIMETERS	INCHES
B	21.06±0.2	0.829±0.008
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.005±0.1	$0.040^{+0.004}_{-0.005}$
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.1	0.004
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

■ **6427525 0091445 110** ■

634