CYM4210
CYM4220

CYPRESS SEMICONDUCTOR

Cascadeable 8K x 9 FIFO
Cascadeable 16K x 9 FIFO

Features

- **8K x 9 FIFO buffer memory (4210) or 16K x 9 FIFO buffer memory (4220)**
- **Asynchronous read/write**
- **High-speed 25-MHz read/write**
- **Pin-compatible with 7C42X series of monolithic FIFOs**
- **Low operating power**
  - **I_{CC} (max.) = 540 mA (commercial)**
- **600-mil DIP package**
- **Empty, full flags**
- **Small PCB footprint**
  - **0.88 sq. in.**
- **Expandable in depth and width**

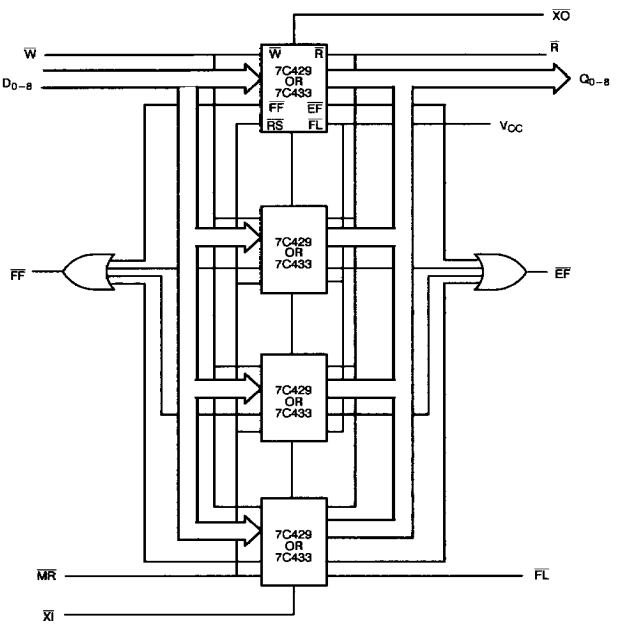
Functional Description

The CYM4210 is a first-in first-out (FIFO) memory module that is 8,192 words by 9 bits wide. The CYM4220 is 16,384 words by 9 bits wide. Each is offered in a 600-mil-wide DIP package. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Full and empty flags are provided to prevent overrun and underrun. Three additional pins are also provided to facilitate unlimited expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another in parallel, thus eliminating the serial addition of propagation delays so that throughput is not reduced. Data is steered in a similar manner.

The read and write operations may be asynchronous; each can occur at a rate of 25 MHz. The write operation occurs when the write ($\overline{W}$) signal is LOW. Read occurs when read ($\overline{R}$) goes LOW. The 9 data outputs go to the high-impedance state when $\overline{R}$ is HIGH.

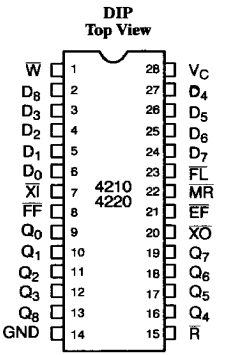
In the depth expansion configuration the ($\overline{XO}$) pin provides the expansion out information that is used to tell the next FIFO that it will be activated.

Logic Block Diagram



4210–1

Pin Configuration



4210–2

Selection Guide

		4210-30 4220-30	4210-40 4220-40	4210-50 4220-50	4210-65 4220-65
Frequency (MHz)		25	20	15.4	12.5
Access Time (ns)		30	40	50	65
Maximum Operating Current (mA)	Commercial	540	540	540	540
	Military		640	640	640

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 0.5V to + 7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Industrial	− 40°C to + 85°C	5V ± 10%
Military[1]	− 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

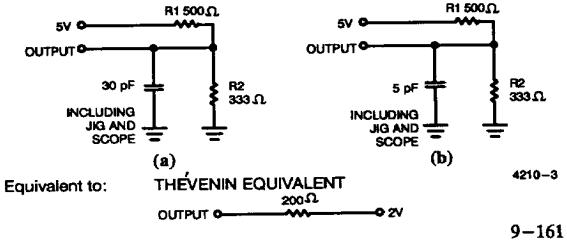
Parameters	Description	Test Conditions		4210 4220 Min.	4210 4220 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 2.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}[2]	Input HIGH Voltage		Com'l	2.0	V_{CC}	V
			Mil/Ind	2.2	V_{CC}	V
V_{IL}	Input LOW Level			− 0.5	0.8	V
I_{IX}	Input Current	$GND \leq V_I \leq V_{CC}$		− 10	+10	μA
I_{OZ}	Output Leakage Current	$\overline{R} \geq V_{IH}$, $GND \leq V_O \leq V_{CC}$		− 10	+10	μA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA, f_{MAX}, Outputs Open	Com'l		540	mA
			Mil/Ind		640	mA
I_{SB1}	Standby Current	All Inputs = V_{IH} Min., V_{CC} = Max. f_{MAX}, I_{OUT} = 0 mA	Com'l		100	mA
			Mil/Ind		120	mA
I_{SB2}	Power-Down Current	All Inputs, $V_{CC} - 0.2 \leq V_{IN} \leq 0.2$, V_{CC} = Max., I_{OUT} = 0, f = 0	Com'l		80	mA
			Mil/Ind		100	mA

Capacitance

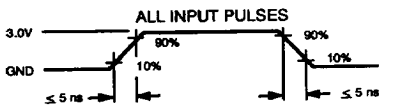
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 4.5V	30	pF
C_{OUT}	Output Capacitance		30	pF

Notes:
1. T_A is the "instant on" case temperature.
2. $\overline{XI}$ must use CMOS levels with $V_{IH} \geq 3.5V$ (CYM4220 only).

AC Test Loads and Waveforms



4210–3



4210–4

Switching Characteristics Over the Operating Range[3, 4, 5]

Parameters	Description	Spec.–30		Spec.–40		Spec.–50		Spec.–65		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	40		50		65		80		ns
t_A	Access Time		30		40		50		65	ns
t_{RR}	Read Recovery Time	10		10		15		15		ns
t_{PR}	Read Pulse Width	30		40		50		65		ns
t_{LZR}	Read LOW to Low Z	3		3		3		3		ns
t_{DVR}	Read HIGH to Data Valid	3		3		3		3		ns
t_{HZR}	Read HIGH to High Z		20		25		30		30	ns
t_{WC}	Write Cycle Time	40		50		65		80		ns
t_{PW}	Write Pulse Width	30		40		50		65		ns
t_{HWZ}	Write HIGH to Low Z	10		10		15		15		ns
t_{WR}	Write Recovery Time	10		10		15		15		ns
t_{SD}	Data Set-Up Time	18		20		30		30		ns
t_{HD}	Data Hold Time	0		0		5		10		ns
t_{MRSC}	$\overline{MR}$ Cycle Time	40		50		65		80		ns
t_{PMR}	$\overline{MR}$ Pulse Width	30		40		50		65		ns
t_{RMR}	$\overline{MR}$ Recovery Time	10		10		15		15		ns
t_{RPW}	Read HIGH to $\overline{MR}$ HIGH	30		40		50		65		ns
t_{WPW}	Write HIGH to $\overline{MR}$ HIGH	30		40		50		65		ns
t_{EFL}	$\overline{MR}$ to $\overline{EF}$ LOW		40		50		65		80	ns
t_{FFH}	$\overline{MR}$ to $\overline{FF}$ HIGH		40		50		65		80	ns
t_{REF}	Read LOW to $\overline{EF}$ LOW		30		40		50		60	ns
t_{RFF}	Read HIGH to $\overline{FF}$ HIGH		30		40		50		60	ns
t_{WEF}	Write HIGH to $\overline{EF}$ HIGH		30		40		50		60	ns
t_{WFF}	Write LOW to $\overline{FF}$ LOW		30		40		50		60	ns
t_{RAE}	Effective Read from Write HIGH		30		40		50		60	ns
t_{RPE}	Effective Read Pulse Width After $\overline{EF}$ HIGH	30		40		50		65		ns
t_{WAF}	Effective Write from Read HIGH		30		40		50		60	ns
t_{WPF}	Effective Write Pulse Width After $\overline{FF}$ HIGH	30		40		50		65		ns
t_{XOL}	Expansion Out LOW Delay from Clock		30		40		50		60	ns
t_{XOH}	Expansion Out HIGH Delay from Clock		30		40		50		60	ns

Notes:

3. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance, as in part (a) of AC Test Load and Waveform, unless otherwise specified.
4. t_{HZR} transition is measured at +500 mV from V_{OL} and −500 mV from V_{OH}. t_{DVR} transition is measured at the 1.5V level. t_{HWZ} and t_{LZR} transition is measured at ±100 mV from the steady state.
5. t_{HZR} and t_{DVR} use capacitance loading as in part (b) of AC Test Load and Waveform.

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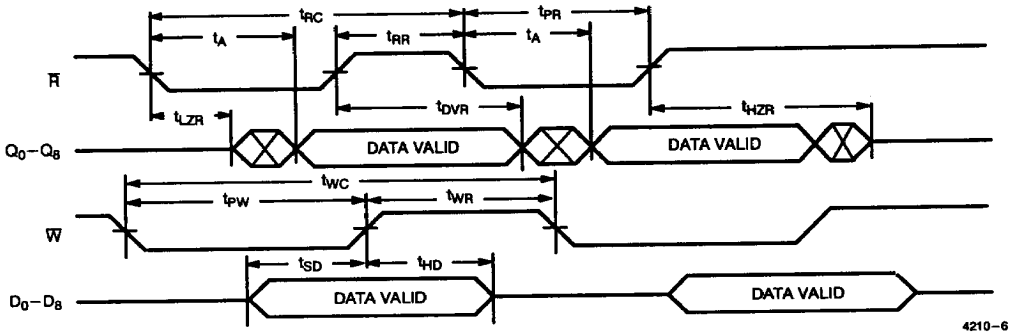
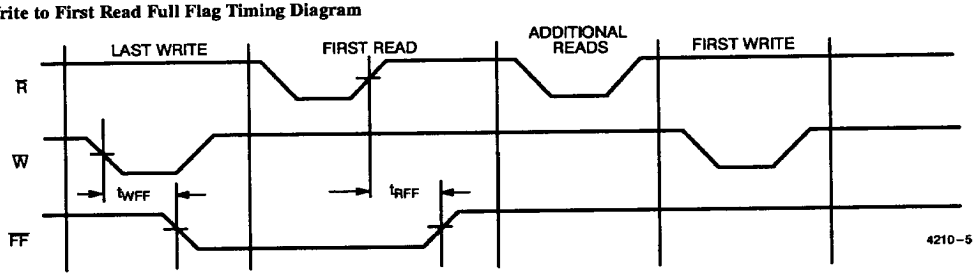
Switching Waveforms

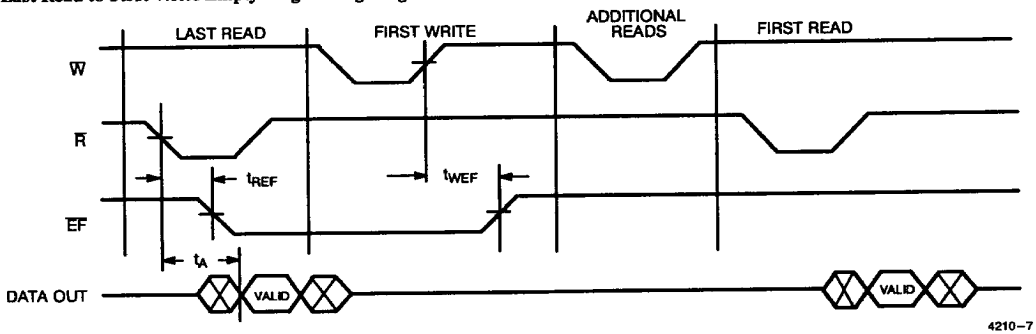
Asynchronous Read and Write Timing Diagram



Last Write to First Read Full Flag Timing Diagram



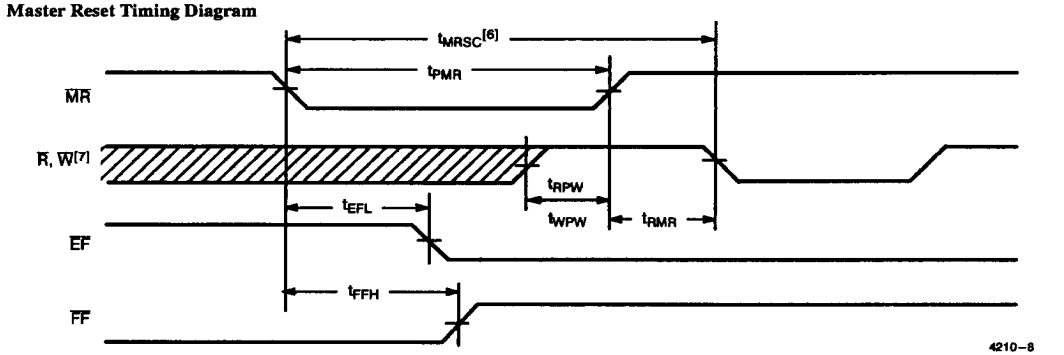
Last Read to First Write Empty Flag Timing Diagram



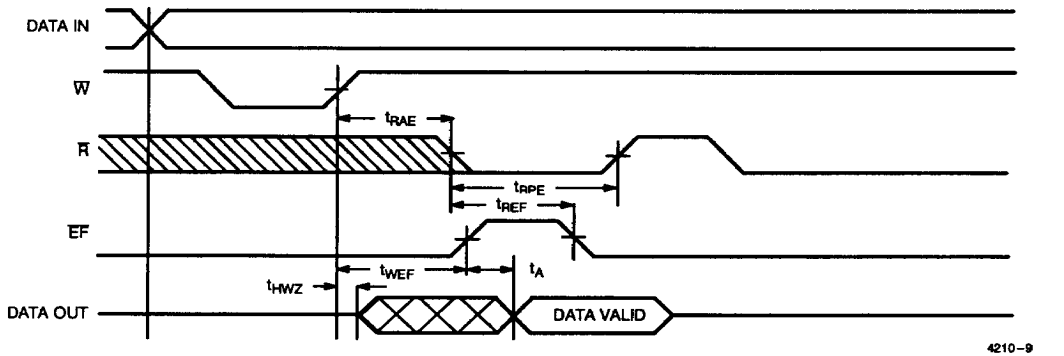
9 MODULES

Switching Waveforms (continued)

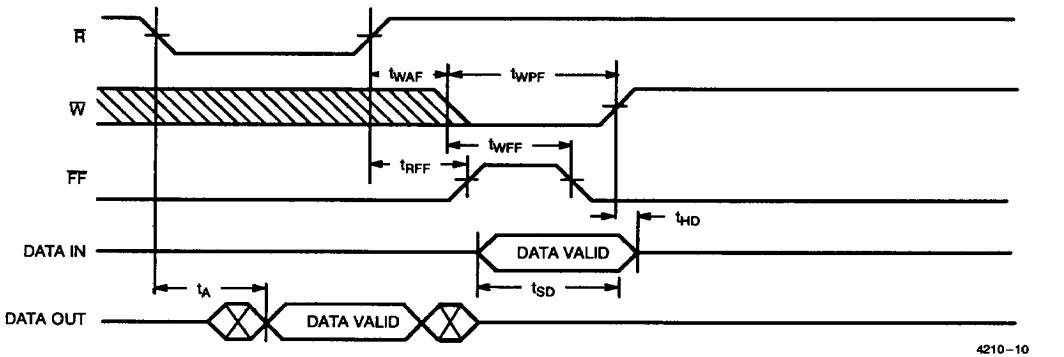
Master Reset Timing Diagram



Empty Flag and Read Bubble-Through Mode Timing Diagram

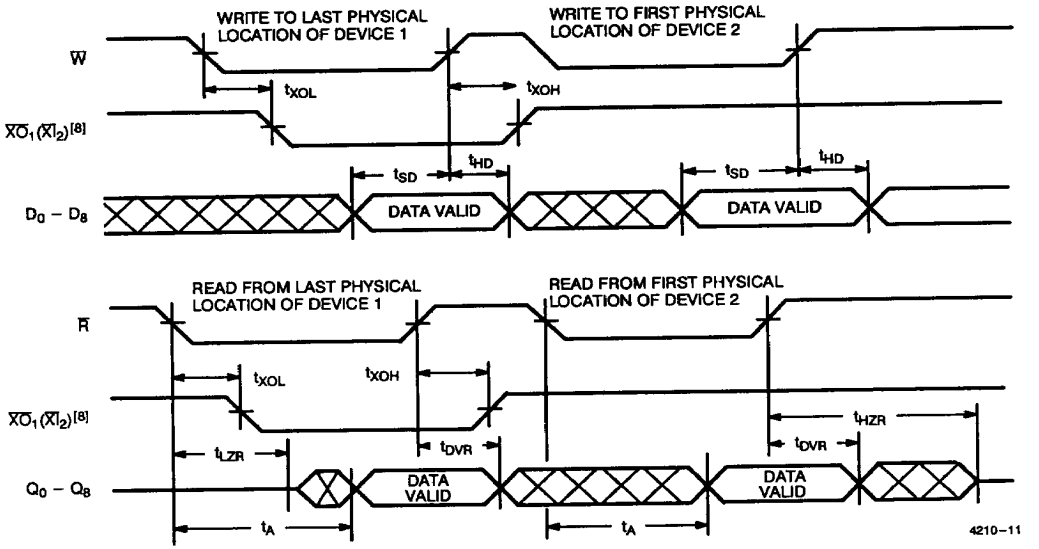


Full Flag and Write Bubble-Through Mode Timing Diagram



Switching Waveforms (continued)

Expansion Timing Diagram



Notes:

6. $t_{MRSC} = t_{PMR} + t_{RMR}$.
7. $\overline{W}$ and $\overline{R} \geq V_{IH}$ for at least t_{WPW} or t_{RPR} before the rising edge of $\overline{MR}$.
8. Expansion Out of Device 1 ($\overline{XO_1}$) is connected to Expansion In of Device 2 ($\overline{XI_2}$).

Architecture

The CYM4210 FIFO module is an array of 8,192 words of 9 bits each and is implemented using four 2K x 9 monolithic FIFOs. The CYM4220 is an array of 16,384 words of 9 bits each and is implemented using four 4K x 9 monolithic FIFOs. Each version has full and empty flags, but since the FIFOs are internally cascaded using the depth mode, the half full and retransmit features are not available.

Pinout of the CYM4210 and CYM4220 are compatible with industry standard 28-pin DIP. The functionality is compatible with monolithic FIFO devices and with other FIFO modules.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a master reset ($\overline{MR}$) cycle. This causes the FIFO to enter the empty condition signified by the empty flag ($\overline{EF}$) being LOW and full flag ($\overline{FF}$) resetting to HIGH. Read ($\overline{R}$) and write ($\overline{W}$) must be HIGH t_{RPW}/t_{WPW} before and t_{RMR} after the rising edge of $\overline{MR}$ for a valid reset cycle.

Writing Data to the FIFO

The availability of an empty location is indicated by the HIGH state of the full flag ($\overline{FF}$). A falling edge of write ($\overline{W}$) initiates a write cycle. Data appearing at the inputs (D_0-D_8) t_{SD} before and t_{HD} after the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

The empty flag ($\overline{EF}$) LOW to HIGH transition occurs t_{WEF} after the first LOW to HIGH transition on the write clock of an empty FIFO. The full flag ($\overline{FF}$) goes LOW on the falling edge of $\overline{W}$ during the cycle in which the last available location in the FIFO is written, prohibiting overflow. $\overline{FF}$ goes HIGH t_{RFF} after the completion of a valid read of a full FIFO.

Reading Data from the FIFO

The falling edge of read ($\overline{R}$) initiates a read cycle if the empty flag ($\overline{EF}$) is not LOW. Data outputs (Q_0-Q_8) are in a high-impedance condition between read operations ($\overline{R}$ HIGH), when the FIFO is empty, or when the FIFO is in the depth expansion mode but is not the active device.

The falling edge of $\overline{R}$ during the last read cycle before the empty condition triggers a HIGH to LOW transition of $\overline{EF}$, prohibiting any further read operations until t_{WEF} after a valid write.

Single Device Mode

Single device mode is entered by connecting $\overline{FL}$ to ground and connecting $\overline{XO}$ to $\overline{XI}$ (see *Figure 1*).

Width Expansion Mode

FIFOs can be expanded in width to provide word widths greater than 9 bits in increments of 9 bits. Devices are connected similar to the single device mode but with control line inputs in common to all devices. Flag outputs from any device can be monitored (see *Figure 2*).

Depth Expansion Mode

Depth expansion mode (see *Figure 3*) is entered when, during a $\overline{MR}$ cycle, expansion out ($\overline{XO}$) of one device is connected to expansion in ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device connected to $\overline{XI}$ of the first device. In the depth expansion mode the first load ($\overline{FL}$) input, when grounded, indicates that this part is the first to be loaded. All other devices must have this pin HIGH. To enable the correct FIFO, $\overline{XO}$ is pulsed LOW when the last physical location of the previous FIFO is written to and is pulsed LOW again when the last physical location is read. Only one FIFO is enabled for read and one is enabled for write at any given time. All other devices are in standby.

FIFOs can also be expanded simultaneously in depth and width. Consequently, any depth or width FIFO can be created of word widths in increments of 9 bits. When expanding in depth, a composite $\overline{FF}$ and $\overline{EF}$ must be created by ORing the $\overline{FF}$s together and the $\overline{EF}$s together.

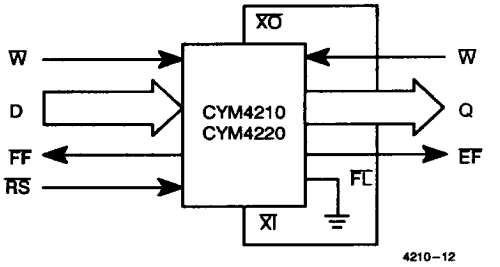


Figure 1. Single Device Mode

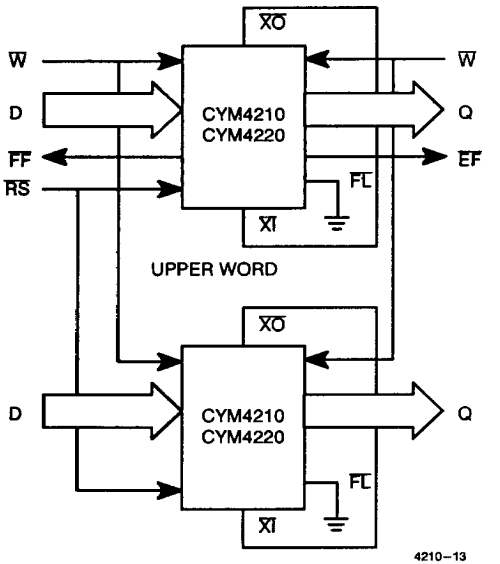


Figure 2. Width Expansion Mode

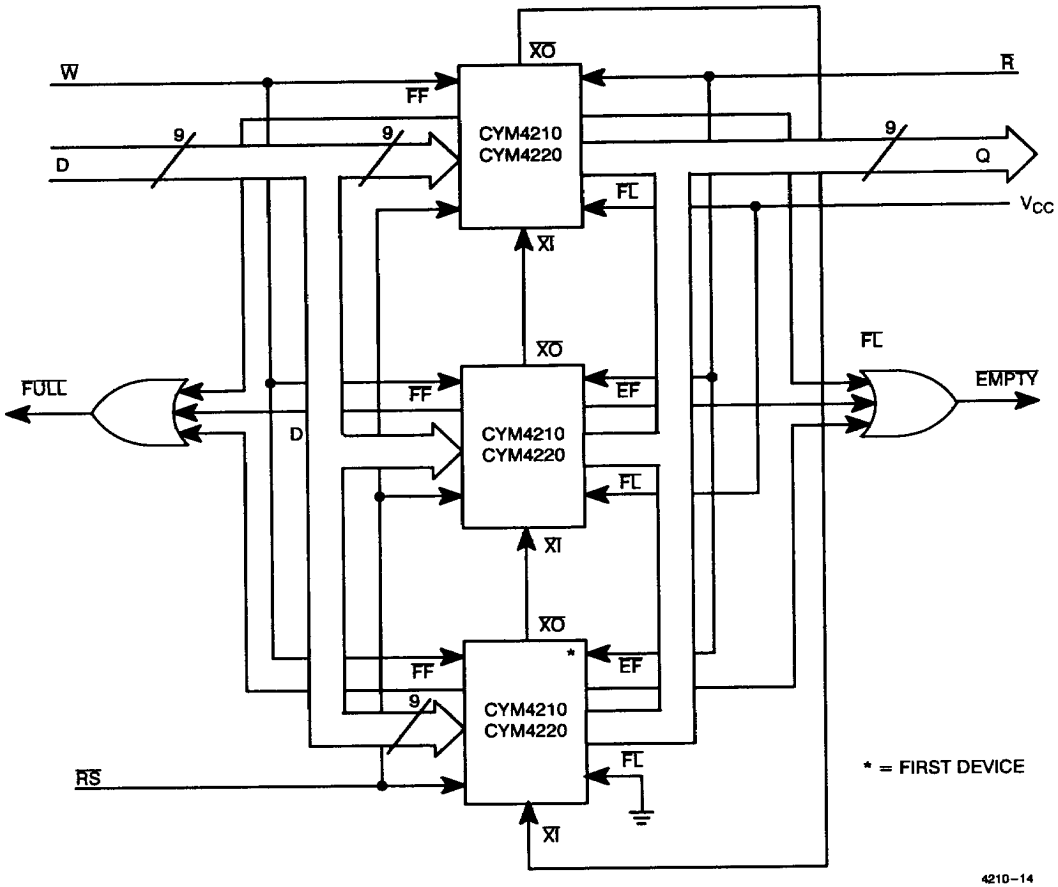


Figure 3. Depth Expansion Mode

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
30	CYM4210HD–30C	HD10	Commercial
40	CYM4210HD–40C	HD10	Commercial
	CYM4210HD–40MB	HD10	Military
50	CYM4210HD–50C	HD10	Commercial
	CYM4210HD–50MB	HD10	Military
65	CYM4210HD–65C	HD10	Commercial
	CYM4210HD–65MB	HD10	Military

Speed (ns)	Ordering Code	Package Type	Operating Range
30	CYM4220HD–30C	HD10	Commercial
40	CYM4220HD–40C	HD10	Commercial
	CYM4220HD–40MB	HD10	Military
50	CYM4220HD–50C	HD10	Commercial
	CYM4220HD–50MB	HD10	Military
65	CYM4220HD–65C	HD10	Commercial
	CYM4220HD–65MB	HD10	Military

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