FEATURES

- Integrates two full-featured M23 and C-bit parity DS3 framer/performance monitors in a single monolithic device.
- Provides a generic microprocessor interface for configuration, control, and status monitoring.
- Generates an interrupt upon detection of any of various alarms, events, or changes in status. Identification of interrupt sources, masking of interrupt sources, and acknowledgement of interrupts is provided via internal registers.
- Low power CMOS technology.
- 84-pin PLCC package.

Each framer/performance monitor section:

- Frames to a DS3 signal with a maximum average reframe time of 1.5 ms.
- Decodes a B3ZS-encoded signal and indicates line code violations.
- Detects loss of signal.
- Provides indication of M-frame and M-subframe boundaries, and overhead bit positions in the DS3 stream.
- Detects the DS3 alarm indication signal (AIS) and idle signal.
- Detection algorithms operate correctly in the presence of a 10^{-3} bit error rate.
- Extracts valid X-bits and indicates far end receive failure.
- Accumulates up to 65,535 line code violation (LCV) events per second, 8191 P-bit parity error events per second, 1023 F-bit or M-bit (framing bit) events per second, and when enabled for C-bit parity mode operation, up to 8191 C-bit parity error events per second, and 8191 far end block error (FEBE) events per second.
- Detects and validates bit-oriented codes in the C-bit parity far end alarm and control channel.
- Optionally extracts the C-bit parity alarm and control signal and serializes it at 9.4 kbit/s.
- Terminates the C-bit parity path maintenance data link with an integral HDLC receiver having a 128-byte deep FIFO buffer. Supports polled, interrupt-driven or DMA access.

- Optionally extracts the C-bit parity mode path maintenance data link signal and serializes it at 28.2 kbit/s.
- Optionally extracts the X, P, M, C and stuff opportunity bits and serializes them at 526 kbit/s on a time division multiplex signal.

REFERENCES

- American National Standard for Telecommunications, ANSI T1.103-1987 - "Digital Hierarchy - Synchronous DS3 Format Specifications".
- American National Standard for Telecommunications, ANSI T1.107-1988 - "Digital Hierarchy - Formats Specifications".
- American National Standard for Telecommunications, ANSI T1.404-1989 - "Customer Installation-to-Network - DS3 Metallic Interface Specification".
- American National Standard for Telecommunications, T1X1.4/89-017R3 - "Draft Proposed Supplement to ANSI T1.107-1988".
- American National Standard for Telecommunications, T1M1.3/90-027R1 - "In-Service Digital Transmission Performance Monitoring Draft Standard".
- Bell Communications Research, TR-TSY-000009 - "Asynchronous Digital Multiplexes Requirements and Objectives," Issue 1, May 1986.
- CCITT Blue Book, Recommendation Q.921 - "ISDN User-Network Interface Data Link Layer Specification", Volume VI, Fascicle VI.10, 1988.
- International Organization for Standardization, ISO 3309:1984 - "High-Level Data Link Control Procedures -- Frame Structure".
- Pacific Microelectronics Centre, PMC 900102, "T1 Solutions Databook," Issue 1, 1990.

DESCRIPTION

The PM8322 T3PM Dual DS3 Framer/Performance Monitor provides DS3 framing and accumulates errors in accordance with ANSI specifications. The device supports a C-bit parity data link through an HDLC interface.

The T3PM is implemented using the PMC Telecom System Block (TSB) library of ASIC functional blocks.

Framing is provided by the FRMR Framer Block. The FRMR accepts either a B3ZS-encoded bipolar or a unipolar signal compatible with M23 and C-bit parity applications. The FRMR frames to a DS3 signal with a maximum average reframe time of 1.5 ms. The FRMR indicates line code violations, loss of signal, framing bit errors, parity errors, C-bit parity errors, AIS, far end receive failure and reception of idle code. When in frame, the FRMR indicates M-frame and M-subframe boundaries and overhead bit positions. When in C-bit parity mode, the FRMR extracts the path maintenance data link and the far end alarm and control (FEAC) channel.

Error event accumulation is provided by the PMON Performance Monitor Block. It accumulates framing bit errors, line code violations, parity errors, C-bit parity errors and far end block errors. The counters are intended to be polled once per second and are sized so as not to saturate at a 10^{-3} bit error rate. Transfer of count values to holding registers may be initiated through the microprocessor port or by an external one second clock.

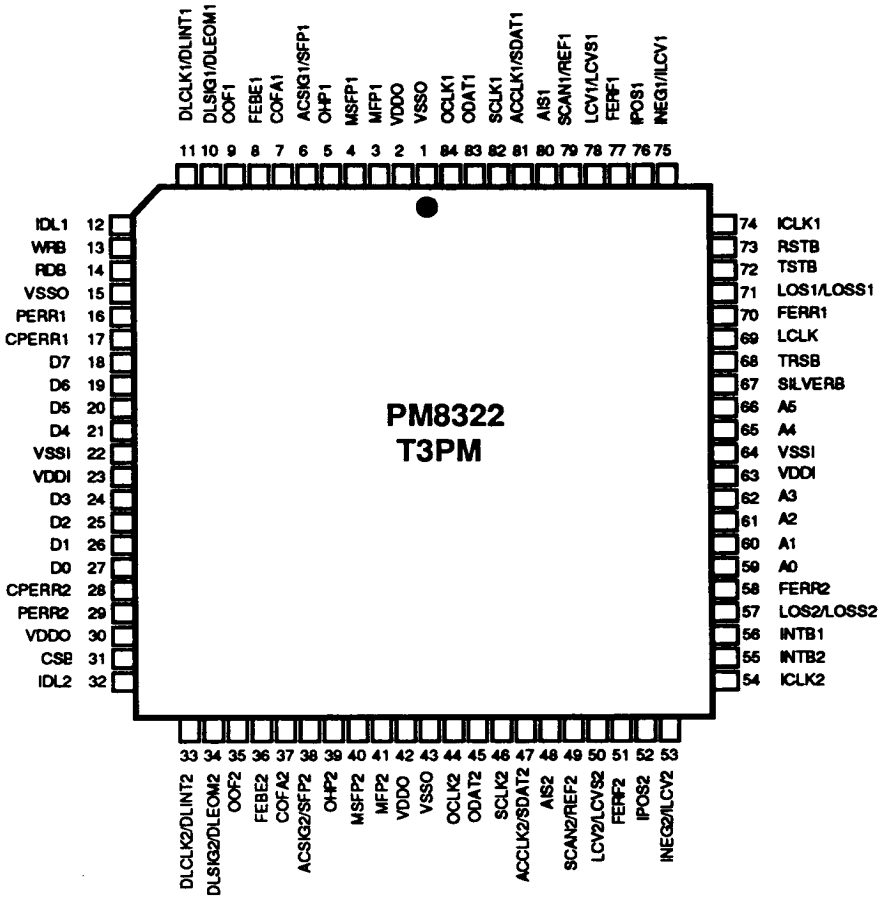
Bit-oriented codes in the FEAC channel are detected by the RBOC Bit-Oriented Code Receiver Block. If enabled, RBOC generates an interrupt when a valid code has been received at least 10 times in succession. The received code may be read through the microprocessor port.

The HDLC controller is implemented by the RDLC Data Link Reciever Block. The RDLC is able to compare the packet destination address against internal register values and places the packet data in a FIFO for access through the microprocessor port. The RDLC supports polled, interrupt-driven and DMA servicing.

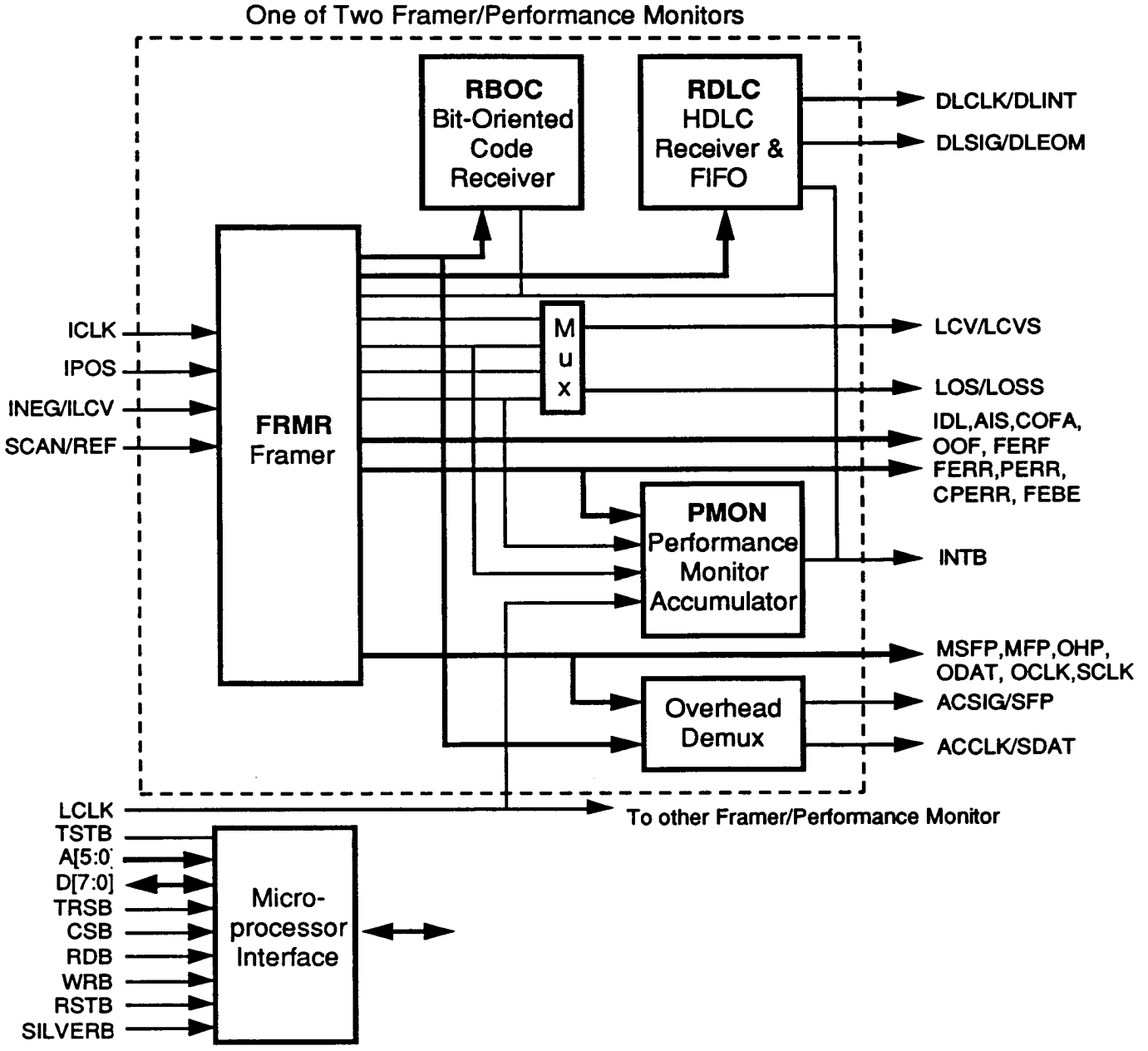
The T3PM is configured, controlled and monitored via a generic 8-bit microprocessor bus through which all internal registers are accessed. All sources of interrupts can be identified, acknowledged, or masked via this interface.

PIN DIAGRAM

The T3PM is available in an 84-pin PLCC package.



BLOCK DIAGRAM



CONNECTOR DESCRIPTION

Pin Name	Type	Pin No.	Function
IPOS1 IPOS2	Input	76 52	The positive input pulse (IPOSx) signals represent the positive pulses received on the B3ZS-encoded line when the UNI bit in the corresponding FRMR Configuration Register is logic 0. IPOSx contains the unipolar DS3 input stream when the UNI bit is logic 1. IPOSx is sampled on the rising edge of the corresponding ICLKx signal if the ICLKINV bit is a logic 0 and on the falling edge of the ICLKx signal if the ICLKINV bit is a logic 1.
INEG1/ ILCV1 INEG2/ ILCV2	Input	75 53	The negative input pulse (INEGx) signals represent the negative pulses received on the B3ZS-encoded line when the UNI bit in the corresponding FRMR Configuration Register is logic 0. Line code violation (LCV) indications may be presented on the ILCVx input if the UNI bit is logic 1. Each LCV is represented by a single ICLKx period-wide pulse. Both INEGx and ILCVx are sampled on the rising edge of the corresponding ICLKx signal if the ICLKINV bit is a logic 0 and on the falling edge of the ICLKx signal if the ICLKINV bit is a logic 1.
ICLK1 ICLK2/ VCLK	Input	74 54	The input clock (ICLKx) signals are nominally 44.736 MHz, 50% duty cycle clocks. All timing for the corresponding performance monitor is derived from the input clock, except timing relating to the Common Bus Interface or to the transfer clock, LCLK. The test vector clock (VCLK) signal is used during T3PM production testing to verify internal functionality of both performance monitors.

SCAN1/ REF1 SCAN2/ REF2	Input	79 49	The scan (SCANx) signals provide a means to sense the state of a logic signal through a microprocessor read. The value of SCANx can always be read, regardless of the state of the EREF bit in the corresponding Master Configuration Register. If enabled, a SCANx state change generates an interrupt. If external reframe is selected (the corresponding EREF bit is a logic 1), the reframe (REFx) signals force the corresponding FRMR to begin a search for frame alignment. A reframe is triggered when a low-to-high transition occurs on the logical OR of REFx and the REFR register bit. REFx is sampled by ICLKx, but may be asynchronous to ICLKx.
LCLK	Input	69	The rising edge of the accumulation interval transfer clock (LCLK) signal causes all event counter values to be saved in the holding registers and the counters to be reset. The time between successive rising edges of LCLK determines the accumulation interval (nominally 1 second), which must be at least 3 full SCLK periods. LCLK may be asynchronous to the ICLKx signals. The LCLK signal must be "glitch-free".
OCLK1 OCLK2	Output	84 44	The output clock (OCLKx) signals provide timing for downstream processing, such as demultiplexing, of each DS3 stream. OCLKx is nominally a 44.736 MHz, 50% duty cycle clock. ODATx, MFPx, MSFPx, OHPx, LCVx, and LOSx are updated on the falling edge of the corresponding OCLKx signal. OCLKx is the same polarity as ICLKx if the ICLKINV bit is a logic one; otherwise, OCLKx is the opposite polarity of ICLKx.
ODAT1 ODAT2	Output	83 45	The decoded data output (ODATx) signals carry the 44.736 Mbit/s NRZ stream decoded from each B3ZS line signal. The frame alignment signals (MFPx, MSFPx, and OHPx) are aligned to the corresponding ODATx stream. ODATx is updated on the falling edge of the corresponding OCLKx signal.

MFP1 MFP2	Output	3 41	When the corresponding performance monitor is in-frame, the M-frame pulse (MFPx) signals mark the first bit (X1) in the M-frame of the DS3 signals on each ODATx signal. When either performance monitor is out-of-frame, the corresponding MFPx signal continues to operate with timing aligned to the old framing position until the performance monitor goes in-frame, at which time a change of frame alignment may occur. MFPx is updated on the falling edge of the corresponding OCLKx signal.
MSFP1 MSFP2	Output	4 40	When the corresponding performance monitor is in-frame, the M-subframe pulse signals (MSFPx) mark the first bit (X, P, or M) in the M-subframe of the DS3 signals on each ODAT signal. When either performance monitor is out-of-frame, the corresponding MSFPx signal continues to operate with timing aligned to the old framing position until the performance monitor goes in-frame, at which time a change of frame alignment may occur. MSFPx is updated on the falling edge of the corresponding OCLKx signal.
OHP1 OHP2	Output	5 39	When the corresponding performance monitor is in-frame, the overhead pulse (OHPx) signals mark the overhead bit positions in the M-frame of the DS3 signals on each ODATx signal. The overhead bit positions are those that carry the X, P, M, F, and C bits. When either performance monitor is out-of-frame, the corresponding OHPx signal continues to operate with timing aligned to the old framing position until the performance monitor goes in-frame, at which time a change of frame alignment may occur. OHPx is updated on the falling edge of the corresponding OCLKx signal.
SCLK1 SCLK2	Output	82 46	The status update clock (SCLKx) signals cycle once per overhead bit. SCLKx is nominally a 526 kHz clock. FERFx, AISx, IDLx, FERRx, PERRx, CPERRx, FEBEx, OOFx, LOSSx, and LCVSx are updated on the falling edge of the corresponding SCLKx. When a change of frame alignment occurs, SCLKx is realigned by lengthening a single cycle. SCLKx is updated on the falling edge of the corresponding OCLKx signal.

LOS1/ LOSS1 LOS2/ LOSS2	Output	71 57	The loss of signal status (LOSx) signals are active when the bipolar, B3ZS encoded, DS3 stream type is selected and loss of signal summing is not selected (the SUM bit in the corresponding Master Configuration Register is a logic 0). LOSx goes high when 175 successive zeros are detected on the corresponding INEGx and IPOSx inputs. LOSx goes low when the ones density is greater than 33% for 175 ± 1 bit periods on the INEGx and IPOSx inputs. LOSx is updated on the falling edge of the corresponding OCLKx signal. The summed loss of signal status (LOSSx) signals are active when the SUM bit in the corresponding Master Configuration Register is a logic 1. LOSSx goes high when a loss of signal is detected during the preceding 85 bits on the corresponding IPOSx and INEGx inputs. LOSSx goes low when a loss of signal declaration is removed during the preceding 85 bits on the IPOSx and INEGx inputs. LOSSx is updated on the falling edge of the corresponding SCLKx signal.
LCV1/ LCVS1 LCV2/ LCVS2	Output	78 50	The line code violation status (LCVx) signals are active when line code violation summing is not selected (the SUM bit in the corresponding Master Configuration Register is a logic 0) and the bipolar, B3ZS encoded, DS3 stream type is selected (the UNI bit in the corresponding FRMR Configuration Register is a logic 0). LCVx goes high for a single bit period when a bipolar violation is detected which is not part of the B3ZS signature or is of the incorrect polarity, or when three consecutive zeros are detected on the corresponding IPOSx and INEGx inputs. LCVx is updated on the falling edge of the corresponding OCLKx signal. The summed line code violation status (LCVSx) signals are active when the SUM bit in the corresponding Master Configuration Register is a logic 1 and the UNI bit in the corresponding FRMR Configuration Register is a logic 0. LCVSx goes high when one or more line code violations are detected during the preceding 85 bits on the corresponding IPOSx and INEGx inputs. LCVSx is updated on the falling edge of the corresponding SCLKx signal.

OOF1 OOF2	Output	9 35	The out-of-frame (OOFx) signals go high when the corresponding performance monitor declares an out-of-frame condition. An out-of-frame condition is defined as 3 out of 16 (default) or 3 out of 8 consecutive F-bits in error or one or more M-bit errors detected in 3 out of 4 consecutive M-frames. OOFx goes low when the performance monitor declares an in-frame condition. The maximum average reframe time is 1.5 ms when an error free DS3 signal is present. OOFx is updated on the falling edge of the corresponding SCLKx signal.
AIS1 AIS2	Output	80 48	The alarm indication signal (AISx) signals go high when the corresponding performance monitor detects the alarm indication signal, even in the presence of a 10^{-3} bit errror rate. The AISx output is activated when the AIS pattern is present for 13.5 ms. The AISx output is deactivated when the AIS pattern is not present for 13.5 ms. AISx is updated on the falling edge of the corresponding SCLKx signal.
IDL1 IDL2	Output	12 32	The idle (IDLx) signals go high when the corresponding performance monitor detects the idle signal, even in the presence of a 10^{-3} bit errror rate. The IDLx output is activated when the idle pattern is present for 13.5 ms. The IDLx output is deactivated when the idle pattern is not present for 13.5 ms. IDLx is updated on the falling edge of the corresponding SCLKx signal.
FERF1 FERF2	Output	77 51	The far end receive failure (FERFx) signals go high when the corresponding performance monitor detects that X2=X1=0. FERFx goes low when the performance monitor detects that X2=X1=1. If the performance monitor detects that X2≠X1, FERFx remains unchanged. Changes in FERFx occur no more than once per M-frame. FERFx is updated on the falling edge of the corresponding SCLKx signal.

FERR1 FERR2	Output	70 58	The framing error (FERRx) signals go high for a single SCLKx period when the corresponding performance monitor detects that an F-bit or an M-bit is in error; otherwise FERRx remains low. FERRx may be high no more than 31 times (of 56 SCLKx cycles) per M-frame. FERRx is updated on the falling edge of the corresponding SCLKx signal.
PERR1 PERR2	Output	16 29	The parity error (PERRx) signals go high for a single SCLKx period when the corresponding performance monitor detects that P2=P1=bad parity or P2≠P1; otherwise PERRx remains low. PERRx may pulse high only once per M-frame. PERRx is updated on the falling edge of the corresponding SCLKx signal.
CPERR1 CPERR2	Output	17 28	The C-bit parity error (CPERRx) signals go high for a single SCLKx period when the corresponding performance monitor detects that the majority vote of the C-bits in M-subframe #3 corresponds to bad parity; otherwise CPERRx remains low. CPERRx may pulse high only once per M-frame. CPERRx is held low if C-bit parity mode is not enabled. CPERRx is updated on the falling edge of the corresponding SCLKx signal.
FEBE1 FEBE2	Output	8 36	The far end block error (FEBEx) signals go high for a single SCLKx period when the corresponding performance monitor detects that the three C-bits in M-subframe #4 are not all equal to logic 1; otherwise FEBEx remains low. FEBEx may pulse high only once per M-frame. FEBEx is held low if C-bit parity mode is not enabled. FEBEx is updated on the falling edge of the corresponding SCLKx signal.
COFA1 COFA2	Output	7 37	The change of frame alignment (COFAx) signals go high for a single SCLKx period when a change of frame alignment is detected by the corresponding performance monitor; otherwise COFAx remains low. COFAx is updated on the falling edge of the corresponding SCLKx signal.

DLCLK1/ DLINT1 DLCLK2/ DLINT2	Output	11 33	The data link clock (DLCLKx) signals are active when an external HDLC receiver is selected (the EXHDLC bit in the corresponding Master Configuration Register is a logic 1). The DLCLKx signals provide timing for the external processing of the data link signal extracted by the corresponding performance monitor. DLCLKx is updated on the falling edge of the corresponding SCLKx signal and cycles 3 times per M-frame. DLCLKx is nominally a 28.2 kHz clock, which is low for at least 1.9 µs per cycle. The data link interrupt (DLINTx) signals are active when the internal HDLC receiver is selected (the EXHDLC in the corresponding Master Configuration Register bit is a logic 0). The DLINTx signals go high when an event occurs which changes the status of the HDLC receiver in the corresponding performance monitor. DLINTx is updated on the falling edge of the corresponding SCLKx signal. DLINTx is brought low when the Interrupt Enable/Status Register is read in the corresponding performance monitor.
DLSIG1/ DLEOM1 DLSIG2/ DLEOM2	Output	10 34	The data link (DLSIGx) signals are active when an external HDLC receiver is selected (the EXHDLC bit in the corresponding Master Configuration Register is a logic 1). The DLSIGx signals carry bits extracted from the three C-bits in M-subframe #5 by the corresponding performance monitor. DLSIGx is held high when C-bit parity mode is not enabled. DLSIGx is updated on the falling edge of the corresponding DLCLKx signal. The end of message (DLEOMx) signals are active if the internal HDLC receiver is selected (the EXHDLC bit in the corresponding Master Configuration Register is a logic 0). The DLEOMx signals go high when the last byte of a sequence is read from the HDLC receiver in the corresponding performance monitor, or if that receiver's buffer overruns. DLEOMx is updated on the falling edge of the corresponding SCLKx signal. DLEOMx is brought low when the Interrupt Enable/Status Register is read in the corresponding performance monitor.

ACSIG1/ SFP1 ACSIG2/ SFP2	Output	6 38	The alarm and control (ACSIGx) signals are active if the status outputs are not selected (the SOEN bit in the corresponding Master Configuration Register is a logic 0). ACSIGx carries bits extracted from the third C-bit in M-subframe #1. ACSIG is held high when C-bit parity mode is not enabled. ACSIG is updated on the falling edge of ACCLK. The status frame pulse (SFPx) signals are active if the status outputs are enabled (the SOEN bit in the corresponding Master Configuration Register is a logic 1). SFPx is high during the first block of the M-frame and marks the X1 bit position of the SDATx serial stream. SFPx is updated on the falling edge of SCLKx.
ACCLK1/ SDAT1 ACCLK2/ SDAT2	Output	81 47	The alarm and control clock (ACCLKx) signals are active if the status outputs are not selected (the corresponding SOEN bit is a logic 0). ACCLKx provides timing for the processing of the alarm and control signal. ACCLKx is updated on the falling edge of SCLK and cycles once per M-frame. ACCLKx is nominally a 9.4 kHz clock, which is low for at least 1.9 µs per cycle. The status data (SDATx) signals are active if the status outputs are enabled (the corresponding SOEN bit is a logic 1). The SDATx signal presents the overhead bits (X, P, M and C) and stuffing opportunity bits in a time multiplexed format. SDATx is updated on the falling edge of the corresponding SCLKx.
INTB1 INTB2	Output	56 55	The active low interrupt (INTBx) signals go low when the COFAx signal goes high, when any of the LOSx, OOFx, FERFx, AISx or IDLx signals change state, or when one of the RDLC, RBOC or PMON TSBs generates an interrupt, provided that the interrupt source in question is not masked. INTBx goes high when the Interrupt Enable/Status Register is read in the corresponding performance monitor. Note that INTBx will remain low until all active, unmasked interrupt sources are acknowledged. Each INTBx signal is an open drain output.
CSB	Input	31	The active low chip select (CSB) signal must be low to enable T3PM register accesses.

D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	I/O	27 26 25 24 21 20 19 18	The bidirectional data bus (D[7:0]) is used during T3PM read and write accesses.
RDB	Input	14	The active low read enable (RDB) signal is pulsed low to enable a T3PM register read access. The T3PM drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are both low.
WRB	Input	13	The active low write strobe (WRB) signal is pulsed low to enable a T3PM register write access. The D[7:0] bus contents are clocked into the addressed normal mode register on the rising edge of WRB while CSB is low.
SILVERB	Input	67	The active low silicon verification mode (SILVERB) signal is used to enable direct access to internal Telecom System Blocks within the T3PM. SILVERB must be high to enable normal operation.
TSTB	Input	72	The active low test mode select (TSTB) signal is low during T3PM production testing. TSTB must be high to enable normal operation.
RSTB	Input	73	The active low reset (RSTB) signal asynchronously resets the T3PM.
TRSB	Input	68	The test register select (TRSB) signal discriminates between normal and test mode register accesses. TRSB is low during test mode register accesses, and is high during normal mode register accesses. TRSB must be high to enable normal operation.
A[0] A[1] A[2] A[3] A[4] A[5]	Input	59 60 61 62 65 66	The address bits (A[6:0]) select specific registers during T3PM register accesses.

VDDO[0] VDDO[1] VDDO[2]	Power	30 2 42	The pad ring power pins (VDDO[2:0]) must be connected to a common, well decoupled +5 VDC supply together with the VDDI[1:0] pins. Care must be taken to avoid coupling noise induced on the VDDO pins into the VDDI pins.
VDDI[0] VDDI[1]	Power	23 63	The core power pins (VDDI[1:0]) must be connected to a common, well decoupled +5 VDC supply together with the VDDO[2:0] pins.
VSSO[0] VSSO[1] VSSO[2]	Ground	15 1 43	The pad ring ground pins (VSSO[2:0]) must be connected to a common ground together with the VSSI[1:0] pins. Care must be taken to avoid coupling noise induced on the VSSO pins into the VSSI pins.
VSSI[0] VSSI[1]	Ground	22 64	The core ground pins (VSSI[1:0]) must be connected to a common ground together with the VSSO[2:0] pins.

Notes on Pin Description:

1. VDDI and VSSI are the +5 V and ground connections, respectively, for the core circuitry of the device. VDDO and VSSO are the +5 V and ground connections, respectively, for the pad ring circuitry of the device. These power supply connections must all be utilized and must all connect to a common +5 V or ground rail, as appropriate. There is no low impedance connection within the PM8322 between the core and pad ring supply rails. Failure to properly make these connections may result in improper operation or damage to the device.
2. Inputs TSTB, RSTB, TRSB, CSB and SILVERB have internal pull-up resistors.

FUNCTIONAL DESCRIPTION

FRMR T3 Framer

The T3 Framer (FRMR) Block integrates circuitry required for decoding a B3ZS-encoded signal and framing to the resulting DS3 bit stream. The FRMR is directly compatible with the M23 and C-bit parity DS3 applications.

The FRMR decodes a B3ZS-encoded signal and provides indications of line code violations. Loss of signal is also detected.

The FRMR frames to a DS3 signal with a maximum average reframe time of 1.5 ms. Once in-frame, the FRMR provides indications of the M-frame and M-subframe boundaries, and identifies the overhead bit positions in the incoming DS3 signal.

While the FRMR is in-frame, the F-bit and M-bit positions in the DS3 stream are examined. Out-of-frame is declared when 3 F-bit errors out of 16 consecutive F-bits or 8 consecutive F-bits are observed (selectable by the M3O8 bit), or when one or more M-bit errors are detected in 3 out of 4 consecutive M-frames. The 3 out of 8 consecutive F-bits out-of-frame ratio provides more robust operation in the presence of a 10^{-3} bit error rate than the 3 out of 16 consecutive F-bits ratio (less than one false OOF every minute verses one false OOF every 6 seconds, respectively); either choice of out-of-frame ratios allows an out-of-frame to be declared quickly when the M-frame, or M-subframe alignment patterns are lost.

Status signals such as the alarm indication signal and the idle signal are detected. The detection algorithms operate in the presence of bit error rates of up to 10^{-3}.

Valid X-bits are extracted by the FRMR to provide indication of far end receive failure. M-bit and F-bit framing errors and P-bit parity errors are indicated. When C-bit parity mode is enabled, both C-bit parity errors and far end block errors are indicated. These error indications, as well as the summed line code violation indication, may be accumulated over 1 second intervals with the T3 Performance Monitor (PMON).

When enabled for C-bit parity operation, both the far end alarm and control channel and the path maintenance data link are extracted and serialized at 9.4 kbit/s and 28.2 kbit/s, respectively. Codes in the extracted far end alarm and control (FEAC) channel may be detected with the Bit-Oriented Code Detector (RBOC). HDLC messages in the extracted path maintenance data link may be received with the Data Link Receiver (RDLC).

The FRMR may be configured for C-bit parity mode or left in M23 mode. When C-bit parity mode is not enabled, outputs relating to C-bit parity features are forced to an inactive state. The FRMR, however, provides an indication of whether the C-bit parity application is present or absent, independent of how it is configured.

The FRMR may be configured to generate interrupts on error events or status changes. All sources of interrupts can be masked or acknowledged via internal registers. Internal registers are also used to configure the FRMR. Access to these registers is via a generic microprocessor bus.

PMON Performance Monitor Accumulator

The T3 Performance Monitor (PMON) Block interfaces directly with the T3 Framer (FRMR) to accumulate summed line code violation (LCVS) events, P-bit parity error (PERR) events, C-bit parity error (CPERR) events, far end block error (FEBE) events, and framing bit error (FERR) events in counters over intervals which are defined by the supplied transfer clock signal. Each counter saturates at a specific value.

When the transfer clock signal is applied, the PMON transfers the counter values into holding registers and resets the counters to begin accumulating error events for the next interval. The counters are reset in such a manner that error events occurring during the reset period are not missed. This transfer can also be triggered by writing to internal registers.

Whenever counter data is transferred into the holding registers, an interrupt is generated, providing the interrupt is enabled. If the holding registers have not been read since the last interrupt, an overrun status bit is set.

RBOC Bit-Oriented Code Detector

The Bit-Oriented Code Detector (RBOC) Block detects the presence of 63 of the 64 possible bit-oriented codes (BOCs) transmitted in the far-end alarm and control (FEAC) channel. The 64th code ("111111") is similar to the HDLC flag sequence and is ignored.

Bit-oriented codes are received on the FEAC channel as 16-bit sequences each consisting of 8 ones, a zero, 6 code bits, and a trailing zero ("111111110xxxxxx0"). BOCs are validated when repeated at least 10 times . The RBOC can be enabled to declare a received code valid if it has been observed for 8 out of 10 times or for 4 out of 5 times, as specified by the AVC bit in the RBOC Configuration/Interrupt Enable Register.

Valid BOCs are indicated through the RBOC Interrupt Status Register. The BOC bits are set to all ones ("111111") if no valid code has been detected. The RBOC can be programmed to generate an interrupt when a detected code has been validated and when the code disappears.

RDLC Data Link Receiver

The Data Link Receiver (RDLC) Block is a microprocessor peripheral used to receive LAPD/HDLC packets on the serial HDLC bit stream that is extracted by the FRMR.

The RDLC detects the change from flag characters to the first byte of data, removes stuffed zeros on the incoming data stream, receives packet data, and calculates the CRC-CCITT frame check sequence (FCS).

In the address matching mode, only those packets whose first data byte matches one of two programmable bytes or the universal address (all ones) are stored in the FIFO. The two least significant bits of the address comparison can be masked for LAPD SAPI matching.

Received data is placed into a 128-level FIFO buffer. An interrupt is generated when a programmable number of bytes are stored in the FIFO buffer. Other sources of interrupt are detection of the terminating flag sequence, abort sequence, or FIFO buffer overrun.

The RDLC Status Register contains bits which indicate the overrun or empty FIFO status, the interrupt status, and the occurrence of first flag or end of message bytes written into the FIFO. The RDLC Status Register also indicates the abort, flag, and end of message status of the data just read from the FIFO. On end of message, the RDLC Status Register indicates the FCS status and if the packet contained a non-integer number of bytes.

Microprocessor Interface

The Microprocessor Interface (MPIF) Block allows for device level configuration of each performance monitor (PM) in the T3PM package. Features such as software reset, device version identification, the selection of summed statuses and the use of the internal or an external HDLC controller are configured via the Master Configuration Register. The Master Interrupt Enable and Status Register provides the two interrupt enables, the state of the SCAN pin and the status of the SCAN interrupt.

The MPIF Block also serves as the physical interface between the microprocessor and the internal blocks. The MPIF Block provides functions such as data bus buffering and address decoding.

Overhead Demultiplexer

The overhead demultiplexer extracts the X, P, M, C and stuff-opportunity bits from the DS3 serial stream and presents the bits at a nominally 526.3 kbit/s rate on the

SDATx output pin. Precise phase relationships and frame format are given in the Functional Timing section.

REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the T3PM. Normal mode registers (as opposed to test mode registers) are selected when TRSB (CBI[13]) is high.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. Reading back unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the the T3PM to determine the programming state of the block.

3. Writeable normal mode register bits are cleared to logic 0 upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect T3PM operation unless otherwise noted.

Normal Mode Register Memory Map (TRSB=1)

PM-1	PM-2	REGISTER DESCRIPTION
00H	20H	MASTER CONFIGURATION
01H	21H	MASTER INTERRUPT ENABLE AND STATUS
02H	22H	VERSION ID
03H	23H	Reserved
04H	24H	FRMR CONFIGURATION
05H	25H	FRMR INTERRUPT ENABLE
06H	26H	FRMR INTERRUPT STATUS
07H	27H	FRMR STATUS
08H	28H	RDLC CONFIGURATION
09H	29H	RDLC INTERRUPT CONTROL
0AH	2AH	RDLC STATUS
0BH	2BH	RDLC DATA
0CH	2CH	RDLC PRIMARY ADDRESS MATCH
0DH	2DH	RDLC SECONDARY ADDRESS MATCH
0EH	2EH	RBOC CONFIGURATION/INTERRUPT ENABLE
0FH	2FH	RBOC INTERRUPT STATUS
10H	30H	Reserved for PMON test
11H	31H	PMON INTERRUPT ENABLE/STATUS

12H-15H	32H-35H	Reserved
16H	36H	PMON FRAMING BIT ERROR EVENT COUNT LSB
17H	37H	PMON FRAMING BIT ERROR EVENT COUNT MSB
18H	38H	PMON LINE CODE VIOLATION EVENT COUNT LSB
19H	39H	PMON LINE CODE VIOLATION EVENT COUNT MSB
1AH	3AH	PMON PARITY ERROR EVENT COUNT LSB
1BH	3BH	PMON PARITY ERROR EVENT COUNT MSB
1CH	3CH	PMON C-BIT PARITY ERROR EVENT COUNT LSB
1DH	3DH	PMON C-BIT PARITY ERROR EVENT COUNT MSB
1EH	3EH	PMON FEBE EVENT COUNT LSB
1FH	3FH	PMON FEBE EVENT COUNT MSB

Note: All register bits are cleared to logic 0 upon activation of T3PM reset unless otherwise noted.

Internal Registers

Register 00H, 20H: Master Configuration

Bit	Type	Function
Bit 7	R/W	SUM
Bit 6	R/W	UNILCV
Bit 5	R/W	SOEN
Bit 4	R/W	EREF
Bit 3	R/W	ICLKINV
Bit 2	R/W	AISABORT
Bit 1	R/W	DLINVERT
Bit 0	R/W	EXHDLC

This register allows software to configure the associated performance monitor (PM) (address 00H for PM-1, address 20H for PM-2) in the T3PM.

The state of the external HDLC (EXHDLC) bit determines whether the performance monitor (PM) uses the internal HDLC receiver or provides the data and clock signals for an external HDLC receiver. When the EXHDLC bit is a logic 0, the internal HDLC receiver is selected; the DLINTx/DLSIGx pin is configured to output the interrupt signal (DLINTx) from the internal HDLC receiver and the DLEOMx/DLCLKx pin is configured to output the end-of-message signal (DLEOMx) from the internal HDLC receiver. When the EXHDLC bit is a logic 1, the use of an internal HDLC receiver is selected; the DLINTx/DLSIGx pin is configured to output the data link

data stream (DLSIGx) and the DLEOMx/DLCLKx pin is configured to output the data link clock signal (DLCLKx). The EXHDLC bit is cleared to logic 0 upon reset.

The data link invert (DLINVERT) bit unconditionally inverts the message data sent to the RDLC TSB or the DLSIGx pin if set to a logic 1. The DLINVERT is cleared to logic 0 upon reset.

If the AISABORT bit is a logic 1, the message data presented to the RDLC TSB and on the DLSIGx is set to all ones when AIS is detected (provided the DLINVERT bit is a logic 0, otherwise the data is set to all zeros). The all ones data causes the RDLC to abort. The AISABORT bit is cleared to logic 0 upon reset.

The ICLKINV bit determines the active edge of the ICLKx input pin. If ICLKINV is a logic 0, the IPOSx and INEGx data are clocked on the rising edge of ICLKx. If ICLKINV is a logic 1, the IPOSx and INEGx data are clocked on the falling edge of ICLKx. The ICLKINV bit is cleared to logic 0 upon reset.

The external reframe (EREF) bit configures the corresponding SCANx/REFx pin. If EREF is a logic 1, a reframe is triggered when a low-to-high transition occurs on the SCANx/REFx pin. The ability to read the state of SCANx/REFx through the microprocessor port is not affected by the EREF bit.

The state of the status output enable (SOEN) bit configures the ACCLKx/SDATx and ACSIGx/SFPx outputs. When the SOEN bit is a logic 0, the ACCLKx/SDATx pin is configured to output the alarm and control clock (ACCLKx) and the ACSIGx/SFPx pin is configured to output the alarm and control signal (ACSIGx). When the SOEN bit is a logic 1, the ACCLKx/SDATx pin is configured to output the status data (SDATx) and the ACSIGx/SFPx pin is configured to output status frame pulse signal (SFPx). Upon reset of a PM, the SOEN bit is cleared to logic 0, thus selecting ACCLKx and ACSIGx.

The UNILCV bit allows the accumulation of line code violations (LCVs) when the framer is configured in unipolar receive mode. This feature assumes that the external line interface unit has an LCV indication output, connected to the INEGx/ILCVx pin, which pulses high for one OCLK cycle for each LCV. If UNILCV is a logic 1, LCVs are accumulated and the state of ILCVx is output on the LCVx/LCVSx pin. This bit is distinct from the FRMR UNI bit and should be set to a logic 0 if the UNI bit is a logic 0. Upon reset of a PM, the UNILCV bit is cleared to logic 0.

The SUM bit determines the data format for the LCVx/LCVSx and LOSx/LOSSx pins. If SUM is a logic 0, the real time LCVx and LOSx statuses, synchronized to OCLKx, are output. If SUM is a logic 1, the summed statuses, LCVSx and LOSSx are updated on the falling edge of SCLKx. LCVSx is asserted if one or more line code violations occurred since the last falling edge of SCLKx. LOSSx changes if the internal LOS status has changed since the last falling edge of SCLKx. Upon reset of a PM, the SUM bit is cleared to logic 0.

Register 01H, 21H: Master Interrupt Enable and Status

Bit	Type	Function
Bit 7	R	RDLCI
Bit 6	R	RBOCI
Bit 5	R	FRMRI
Bit 4	R	PMONI
Bit 3	R	SCANI
Bit 2	R	SCANV
Bit 1	R/W	SCANE
Bit 0	R/W	RDLCE

The RDLCE bit controls interrupt generation by the RDLC. If RDLCE is a logic 1, an interrupt sourced by RDLC causes the active low INTBx pin to be brought low. If RDLCE is a logic 0, only the DLINTx pin is asserted (brought high) by a RDLC interrupt.

The SCANE bit controls interrupt generation on SCANx pin state changes. If SCANE is a logic 1, a change in the state of the SCANx pin causes the active low INTBx pin to be brought low. When the T3PM is reset, the SCANE bit is reset to 0, disabling the interrupt. The interrupt generated by SCANx is cleared by reading this register. This bit does not affect the SCAN pin interrupt status (SCANI) bit.

The SCANV bit represents the present state of the SCANx input.

The SCANI bit is the SCAN pin interrupt status. The SCANI bit is set to a logic 1 when the SCAN pin changes state. The SCANI bit is cleared to a logic 0 after a read of this register. This bit is not affected by the state of the SCANE bit.

The PMONI bit is a logic 1 if the PMON is presently generating an interrupt; otherwise, it is a logic 0.

The FRMRI bit is a logic 1 if the FRMR is presently generating an interrupt; otherwise, it is a logic 0.

The RBOCI bit is a logic 1 if the RBOC is presently generating an interrupt; otherwise, it is a logic 0.

The RDLCI bit is a logic 1 if the RDLC is presently generating an interrupt which causes INTBx to be asserted; otherwise, it is a logic 0.

Register 02H, 22H: Version Identification

Bit	Type	Function
Bit 7	R/W	RESET
Bit 6	R	ID[6]
Bit 5	R	ID[5]
Bit 4	R	ID[4]
Bit 3	R	ID[3]
Bit 2	R	ID[2]
Bit 1	R	ID[1]
Bit 0	R	ID[0]

The version identification bits, ID[6:0], are set to a fixed value representing the version number of the T3PM. The identification bits of each PM are identical.

The RESET bit implements a software reset for each PM independently. If the RESET bit is a logic 1, the entire PM is held in reset. The bit is not self-clearing; therefore, a logic 0 must be written to bring the PM out of reset. Holding the PM in a reset state effectively puts it into a low power, stand-by mode. A hardware reset clears the RESET bit, thus deasserting the software reset.

FRMR Registers

Register 04H, 24H: FRMR Configuration

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4	R/W	M3O8
Bit 3	R/W	UNI
Bit 2	R/W	REFR
Bit 1	R/W	AISC
Bit 0	R/W	CBE

The CBE bit selects whether the C-bit parity application is enabled. When a logic 1 is written to CBE, C-bit parity mode is enabled. When a logic 0 is written, C-bit parity mode is disabled.

The AISC bit controls the algorithm used to detect the alarm indication signal (AIS). When a logic 1 is written to AISC, the algorithm checks that all C-bits are set to logic 0 before declaring AIS. When a logic 0 is written, the algorithm ignores the C-bits and only demands that a framed AIS pattern (1010...) is present.

The REFR bit is used to trigger reframing. If a logic 1 is written to REFR when it was previously logic 0, the FRMR is forced out-of-frame, and a new search for frame alignment is initiated. Note that only a low to high transition of the logical OR of the REFR bit and the REF input triggers reframing; multiple write operations are required to ensure such a transition.

The UNI bit is used to configure the FRMR to accept either unipolar or bipolar data streams. When a logic 1 is written to UNI, the FRMR accepts unipolar data on IPOSx. When a logic 0 is written to UNI, the FRMR accepts bipolar data on IPOSx and INEGx and performs B3ZS decoding and line code violation reporting.

The M3O8 bit configures the out of frame decision criteria. If M3O8 is a logic 1, out of frame is declared if at least 3 of 8 framing bits are in error. If M3O8 is a logic 0, the standard 3 of 16 bits in error criteria is used.

Register 05H, 25H:
FRMR Interrupt Enable

Bit	Type	Function
Bit 7	R/W	COFAE
Bit 6		Unused
Bit 5	R/W	CBITE
Bit 4	R/W	FERFE
Bit 3	R/W	IDLE
Bit 2	R/W	AISE
Bit 1	R/W	OOFE
Bit 0	R/W	LOSE

The LOSE, OOFE, AISE, IDLE, FERFE, CBITE, and COFAE bits are interrupt enables. A change of state on a corresponding FRMR output or an event on the COFAx output causes the interrupt output to be set high when the corresponding interrupt enable bit is written with a logic 1.

A FRMR generated interrupt is cleared when the FRMR Interrupt Status Register is read.

Register 06H, 26H:
FRMR Interrupt Status

Bit	Type	Function
Bit 7	R	COFAI
Bit 6		Unused
Bit 5	R	CBITI
Bit 4	R	FERFI
Bit 3	R	IDLI
Bit 2	R	AISI
Bit 1	R	OOFI
Bit 0	R	LOSI

The LOSI, OOFI, AISI, IDLI, FERFI, CBITI, and COFAI bits are interrupt status indicators. A change of state on the corresponding FRMR output or an event on the COFAx output causes the corresponding interrupt status bit to be set.

The interrupt status bits are cleared when the FRMR Interrupt Status Register is read.

Register 07H, 27H:
FRMR Status

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5	R	CBITV
Bit 4	R	FERFV
Bit 3	R	IDLV
Bit 2	R	AISV
Bit 1	R	OOFV
Bit 0	R	LOSV

The LOSV, OOFV, AISV, IDLV, FERFV, and CBITV bits in this register reflect the state of the corresponding FRMR outputs.

RDLC Registers

Register 08H, 28H: RDLC Configuration

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4	R/W	DMAEN
Bit 3	R/W	MEN
Bit 2	R/W	MAM
Bit 1	R/W	TR
Bit 0	R/W	EN

The enable (EN) bit controls the overall operation of the RDLC. When EN is set to logic 1, the RDLC is enabled; when set to logic 0, the RDLC is disabled. When the RDLC is disabled, the FIFO buffer and interrupts are all cleared. When the RDLC is enabled, it will immediately begin looking for flags.

Setting the terminate reception (TR) bit to logic 1 forces the RDLC to immediately terminate the reception of the current data frame, empty the FIFO buffer, clear the interrupts, and begin searching for a new flag sequence. The RDLC handles a terminate reception event in the same manner as it would the toggling of the EN bit from logic 1 to logic 0 and back to logic 1. Thus, the RDLC state machine will begin searching for flags. An interrupt will be generated when the first flag is detected. The TR bit in the RDLC Configuration Register will reset itself to logic 0 after a rising and falling edge have occurred on the CLK input, once the write strobe (CBI[9]) goes high. If the RDLC Configuration Register is read after this time, the TR bit value returned will be logic 0.

Setting the Mask Address Match (MAM) bit to logic 1 ignores the PA[1:0] bits of the Primary Address Match Register, the SA[1:0] bits of the Secondary Address Match Register, and the two least significant bits of the universal all ones address when the address comparison occurs.

Setting the Match Enable (MEN) bit to logic 1 enables the detection and storage in the FIFO of only those packets whose first data byte matches either of the bytes written to the Primary or Secondary Address Match Registers, or the universal all

ones address. When the MEN bit is logic 0, all packets received are written into the FIFO.

Setting the DMA Enable (DMAEN) bit to logic 1 enables the internal ANDing of the INT output and the inverted EOM output. Under DMA operating mode, when EOM is set to logic 1 (indicating to the micro processor that the RDLC needs servicing), the INT output must be gated off so that no DMA access are performed until the micro processor services the RDLC.

Register 09H, 29H:
RDLC Interrupt Control

Bit	Type	Function
Bit 7	R/W	INTE
Bit 6	R/W	INTC[6]
Bit 5	R/W	INTC[5]
Bit 4	R/W	INTC[4]
Bit 3	R/W	INTC[3]
Bit 2	R/W	INTC[2]
Bit 1	R/W	INTC[1]
Bit 0	R/W	INTC[0]

Bits 6 to 0 (INTC[6:0]) of this register control the assertion of FIFO fill level set point interrupts. Writing all zeros into this register has the same affect has clearing the EN bit in the RDLC Configuration Register. This is the reset state.

The Interrupt Enable bit (INTE) must set to logic 1 to allow the internal interrupt status to be propagated to the DLINTx output. When the INTE bit is logic 0 the DLINTx output is forced to logic 0.

The contents of the RDLC Interrupt Control Register should only be changed when the EN bit in the RDLC Configuration Register is logic 0. This prevents any erroneous interrupt generation.

Register 0AH, 2AH: RDLC Status

Bit	Type	Function
Bit 7	R	FE
Bit 6	R	OVR
Bit 5	R	COLS
Bit 4	R	PKIN
Bit 3	R	PBS[2]
Bit 2	R	PBS[1]
Bit 1	R	PBS[0]
Bit 0	R	INTR

The interrupt (INTR) bit reflects the status of the INTx output unless the INTC[6:0] bits are set to all zeros to disable interrupts. In that case, the INTx output is forced low and the INTR bit of this register will reflect the state of the internal interrupt latch.

The packet byte status (PBS[2:0]) bits indicates the status of the data last read from the FIFO.

If the PBS[2:0] bits are binary 000, then the data byte read from the FIFO is non-special.

If the PBS[2:0] bits are binary 001, then the data byte read from the FIFO is the dummy byte that was written into the FIFO when the first HDLC flag sequence (01111110) was detected. This indicates that the data link became active.

If the PBS[2:0] bits are binary 010, then the data byte read from the FIFO is the dummy byte that was written into the FIFO when the HDLC abort sequence (01111111) was detected. This indicates that the data link became inactive.

If the PBS[2:0] bits are binary 100, then the data byte read from the FIFO is the last byte of a normally terminated packet with no CRC error and the packet received had an integer number of bytes.

If the PBS[2:0] bits are binary 101, then the data byte read from the FIFO must be discarded because there was an non-integer number of bytes in the packet.

If the PBS[2:0] bits are binary 110, then the data byte read from the FIFO is the last byte of a normally terminated packet with a CRC error. The packet was received in error.

If the PBS[2:0] bits are binary 111, then the data byte read from the FIFO is the last byte of a normally terminated packet with a CRC error and an non-integer number of bytes. The packet was received in error.

The Packet In (PKIN) bit is logic 1 when the last byte of a non-aborted packet is written into the FIFO. The PKIN bit is cleared to logic 0 after the Status Register is read.

The Change of Link Status (COLS) bit is set to logic 1 if the RDLC has detected the HDLC flag sequence (01111110) or HDLC abort sequence (01111111) in the data. This indicates that there has been a change in the data link status. The COLS bit is cleared to logic 0 by reading this register or by clearing the EN bit in the Configuration Register. For each change in link status, a byte is written into the FIFO. If the COLS bit is found to be logic 1 then the FIFO must be read until empty. The status of the data link is determined by the PBS bits associated with the data read from the FIFO.

The overrun (OVR) bit is set to logic 1 when data is written over unread data in the FIFO buffer. This bit is not reset to logic 0 until after the Status Register is read. While the OVR bit is logic 1, the RDLC and FIFO buffer are held in the reset state, causing the COLS and PKIN bits to be reset to logic 0.

The FIFO buffer empty (FE) bit is set to logic 1 when the last FIFO buffer entry is read. The FE bit goes to logic 0 when the FIFO is loaded with new data.

Register 0BH, 2BH:
RDLC Data

Bit	Type	Function
Bit 7	R	RD[7]
Bit 6	R	RD[6]
Bit 5	R	RD[5]
Bit 4	R	RD[4]
Bit 3	R	RD[3]
Bit 2	R	RD[2]
Bit 1	R	RD[1]
Bit 0	R	RD[0]

RD[0] corresponds to the first bit of the serial byte received on the DATA input.

This register is actually a 128-byte FIFO buffer. If data is available, the FE bit in the FIFO Input Status Register is logic 0.

When an overrun is detected, an interrupt is generated and the FIFO buffer is held cleared until the FIFO Input Status Register is read.

Register 0CH,2CH:
Primary Address Match

Bit	Type	Function
Bit 7	R/W	PA[7]
Bit 6	R/W	PA[6]
Bit 5	R/W	PA[5]
Bit 4	R/W	PA[4]
Bit 3	R/W	PA[3]
Bit 2	R/W	PA[2]
Bit 1	R/W	PA[1]
Bit 0	R/W	PA[0]

The first byte received after a flag character is compared against the contents of this register. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. PA[0] corresponds to the first bit of the serial byte received by the RDLC. The MAM bit in the RDLC Configuration Register is used to mask off PA[1:0] during the address comparison. This register is reset to all ones when the RDLC is reset.

Register 0DH, 2DH:
Secondary Address Match

Bit	Type	Function
Bit 7	R/W	SA[7]
Bit 6	R/W	SA[6]
Bit 5	R/W	SA[5]
Bit 4	R/W	SA[4]
Bit 3	R/W	SA[3]
Bit 2	R/W	SA[2]
Bit 1	R/W	SA[1]
Bit 0	R/W	SA[0]

The first byte received after a flag character is compared against the contents of this register. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. SA[0] corresponds to the first bit of the serial byte received by the RDLC. The MAM bit in the RDLC Configuration Register is used to mask off SA[1:0] during the address comparison. This register is reset to all ones when the RDLC is reset.

RBOC Registers

Register 0EH, 2EH: RBOC Configuration/Interrupt Enable

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2	R/W	IDLE
Bit 1	R/W	AVC
Bit 0	R/W	BOCE

This register selects the validation criteria to be used in determining a valid bit-oriented code (BOC) on the far-end alarm and control (FEAC) channel and enables generation of an interrupt at code validation.

The BOCE bit position enables or disables the generation of an interrupt when a valid BOC is detected. A logic 1 in this bit position enables generation of an interrupt; a logic 0 in this bit position disables interrupt generation. When the T3PM is reset, BOCE is reset to logic 0; therefore, interrupt generation is disabled.

The AVC bit position selects the validation criterion used in determining a valid BOC. A logic 0 selects the 8 out of 10 matching BOC criterion; a logic 1 in the AVC bit position selects the "alternative" validation criterion of 4 out of 5 matching BOCs.

The IDLE bit position enables or disables the generation of an interrupt when there is a transition from a validated BOC to idle code. A logic 1 in this bit position enables generation of an interrupt; a logic 0 in this bit position disables interrupt generation.

Register 0FH, 2FH:
RBOC Interrupt Status

Bit	Type	Function
Bit 7	R	IDLEI
Bit 6	R	BOCI
Bit 5	R	BOC[5]
Bit 4	R	BOC[4]
Bit 3	R	BOC[3]
Bit 2	R	BOC[2]
Bit 1	R	BOC[1]
Bit 0	R	BOC[0]

The bit positions BOC[5:0] contain the received bit-oriented codes. A logic 1 in the BOCI bit position indicates that a validated BOC code has generated an interrupt; a logic 0 in the BOCI bit position indicates that no BOC has been detected. Since the bit-oriented code "111111" is not recognized by the RBOC, the BOC[5:0] bits are set to all ones ("111111") if no valid code has been detected. The BOCI bit position is cleared to logic 0 and the interrupt is deasserted when this register is read.

The IDLEI bit position indicates whether an interrupt was generated by the detection of the transition from a valid BOC to idle code. A logic 1 in the IDLEI bit position indicates that a transition from a valid BOC to idle code has generated an interrupt; a logic 0 in the IDLEI bit position indicates that no transition from a valid BOC to idle code has been detected. IDLEI is cleared to logic 0 when the register is read.

PMON Registers

Latching Performance Data

The Performance Monitor (PMON) data registers (0AH-0FH, 4AH-4FH) are updated by the rising edge of LCLK. The time between successive rising edges of LCLK determines the accumulation interval, which is nominally one second. A single LCLK input serves both performance monitors in the T3PM. A microprocessor write to any of the PMON LSB data registers also causes an update of the PMON data registers associated with that performance monitor in the T3PM. The PMON is loaded with new performance data within 3 SCLK periods of the rising edge of LCLK. With SCLK at its nominal frequency of 526 kHz, the PMON registers should not be read until 6 µs have elapsed since the rising edge of LCLK or a microprocessor write was performed. The data contained in the holding registers are subsequently read from the PMON registers by the microprocessor. The loading is synchronized to the internal event timing so that no events are missed.

Register 11H, 31H: PMON Interrupt Enable/Status

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2	R/W	INTE
Bit 1	R	INTR
Bit 0	R	OVR

The overrun (OVR) bit indicates the overrun status of the holding registers. A logic 1 in this bit position indicates that a previous interrupt has not been cleared before the end of the next accumulation interval, and that the contents of the holding registers have been overwritten. A logic 0 indicates that no overrun has occurred. This bit is reset to logic 0 when this register is read.

The interrupt (INTR) bit indicates the current status of the internal interrupt signal. A logic 1 in this bit position indicates that a transfer of counter values to the holding registers has occurred; a logic 0 indicates that no transfer has occurred. The INTR bit is set to logic 0 when this register is read. The value of the INTR bit is not affected by the value of the INTE bit.

A logic 1 in the INTE bit position enables the PMON to generate a microprocessor interrupt and assert the INTBx output when the counter values are transferred to the holding registers. A logic 0 in the INTE bit position disables the PMON from generating an interrupt. When the TSB is reset, the INTE bit is set to logic 0, disabling the interrupt. The interrupt is cleared when this register is read.

Register 16H, 36H:
FERR Count LSB

Bit	Type	Function
Bit 7	R	FERR[7]
Bit 6	R	FERR[6]
Bit 5	R	FERR[5]
Bit 4	R	FERR[4]
Bit 3	R	FERR[3]
Bit 2	R	FERR[2]
Bit 1	R	FERR[1]
Bit 0	R	FERR[0]

Register 17H, 37H:
FERR Count MSB

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3		Unused
Bit 2		Unused
Bit 1	R	FERR[9]
Bit 0	R	FERR[8]

These registers indicate the number of framing error (FERR) events that occurred during the previous accumulation interval.

A transfer operation of all counter registers within the selected PMON, equivalent to that generated by a rising edge on LCLK, can be triggered by writing to the FERR Count LSB Register.

Register 18H, 38H:
LCVS Count LSB

Bit	Type	Function
Bit 7	R	LCVS[7]
Bit 6	R	LCVS[6]
Bit 5	R	LCVS[5]
Bit 4	R	LCVS[4]
Bit 3	R	LCVS[3]
Bit 2	R	LCVS[2]
Bit 1	R	LCVS[1]
Bit 0	R	LCVS[0]

Register 19H, 39H:
LCVS Count MSB

Bit	Type	Function
Bit 7	R	LCVS[15]
Bit 6	R	LCVS[14]
Bit 5	R	LCVS[13]
Bit 4	R	LCVS[12]
Bit 3	R	LCVS[11]
Bit 2	R	LCVS[10]
Bit 1	R	LCVS[9]
Bit 0	R	LCVS[8]

These registers indicate the number of summed line code violations (LCVS) that occurred during the previous accumulation interval.

A transfer operation of all counter registers within the selected PMON, equivalent to that generated by a rising edge on LCLK, can be triggered by writing to the LCVS Count LSB Register.

Register 1AH, 3AH:
PERR Count LSB

Bit	Type	Function
Bit 7	R	PERR[7]
Bit 6	R	PERR[6]
Bit 5	R	PERR[5]
Bit 4	R	PERR[4]
Bit 3	R	PERR[3]
Bit 2	R	PERR[2]
Bit 1	R	PERR[1]
Bit 0	R	PERR[0]

Register 1BH, 3BH:
PERR Count MSB

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4	R	PERR[12]
Bit 3	R	PERR[11]
Bit 2	R	PERR[10]
Bit 1	R	PERR[9]
Bit 0	R	PERR[8]

These registers indicate the number of P-bit parity error (PERR) events that occurred during the previous accumulation interval.

A transfer operation of all counter registers within the selected PMON, equivalent to that generated by a rising edge on LCLK, can be triggered by writing to the PERR Count LSB Register.

Register 1CH, 3CH: CPERR Count LSB

Bit	Type	Function
Bit 7	R	CPERR[7]
Bit 6	R	CPERR[6]
Bit 5	R	CPERR[5]
Bit 4	R	CPERR[4]
Bit 3	R	CPERR[3]
Bit 2	R	CPERR[2]
Bit 1	R	CPERR[1]
Bit 0	R	CPERR[0]

Register 1DH, 3DH: CPERR Count MSB

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4	R	CPERR[12]
Bit 3	R	CPERR[11]
Bit 2	R	CPERR[10]
Bit 1	R	CPERR[9]
Bit 0	R	CPERR[8]

These registers indicate the number of C-bit parity error (CPERR) events that occurred during the previous accumulation interval.

A transfer operation of all counter registers within the selected PMON, equivalent to that generated by a rising edge on LCLK, can be triggered by writing to the CPERR Count LSB Register.

Register 1EH, 3EH: FEBE Count LSB

Bit	Type	Function
Bit 7	R	FEBE[7]
Bit 6	R	FEBE[6]
Bit 5	R	FEBE[5]
Bit 4	R	FEBE[4]
Bit 3	R	FEBE[3]
Bit 2	R	FEBE[2]
Bit 1	R	FEBE[1]
Bit 0	R	FEBE[0]

Register 1FH, 3FH: FEBE Count MSB

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4	R	FEBE[12]
Bit 3	R	FEBE[11]
Bit 2	R	FEBE[10]
Bit 1	R	FEBE[9]
Bit 0	R	FEBE[8]

These registers indicate the number of far end block error (FEBE) events that occurred during the previous accumulation interval.

A transfer operation of all counter registers within the selected PMON, equivalent to that generated by a rising edge on LCLK, can be triggered by writing to the FEBE Count LSB Register.

TEST FEATURES DESCRIPTION

Simultaneously asserting the CSB, RDB and WRB inputs causes all output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the T3PM. Test mode registers (as opposed to normal mode registers) are selected when TRSB is low.

Test mode registers may also be used for board testing. When all of the constituent Telecom System Blocks within the T3PM are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. Reading unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.

2. Writeable test mode register bits are not initialized upon reset unless otherwise noted.

Test Mode Register Memory Map (TRSB=0)

PM-1	PM-2	REGISTER DESCRIPTION
00H	20H	Unused
01H		Master Test Register
	21H	Unused
02H	22H	Unused
03H	23H	Unused
04H	24H	FRMR, Test Register 0
05H	25H	FRMR, Test Register 1
06H	26H	FRMR, Test Register 2
07H	27H	FRMR, Test Register 3
08H	28H	RDLC, Test Register 0
09H	29H	RDLC, Test Register 1
0AH	2AH	RDLC, Test Register 2
0BH	2BH	RDLC, Test Register 3
0CH	2CH	RDLC, Test Register 4

0DH	2DH	Unused
0EH	2EH	RBOC, Test Register 0
0FH	2FH	RBOC, Test Register 1
10H	30H	PMON, Test Register 0
11H	31H	PMON, Test Register 1
12H	32H	Unused
13H	33H	Unused
...	...	Unused
1FH	3FH	Unused

Internal Registers

Register 01H: Master Test Register

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3	W	DBCTRL
Bit 2	W	IOTST
Bit 1	W	HIZDATA
Bit 0	W	HIZIO

This register is used to select T3PM test features. All bits are reset to zero by either a hardware reset of the T3PM or a software reset of both PMs in the T3PM.

The IOTST bit is used to allow normal microprocessor access to the test registers in each block in the T3PM. When IOTST is a logic 1, all blocks are held in test mode (i.e. the TSTB line to each block is asserted internally) and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequently the device outputs (refer to the section "Test Mode 0" for details). When IOTST is a logic 0, the timing and signals associated with test mode 0 are not compatible with normal microprocessor bus cycles.

The HIZIO and HIZDATA bits control the tri-state modes of the T3PM . While the HIZIO bit is a logic 1, all output pins of the T3PM except the data bus are held in a high-impedance state. The microprocessor interface is still active. While the

HIZDATA bit is a logic 1, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles.

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic 1, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the T3PM to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

Test Mode 0

In test mode 0, the T3PM allows the logic levels on the device inputs to be read through the microprocessor interface, and allows the device outputs to be forced to either logic level through the microprocessor interface.

To enable test mode 0, the TSTB and TRSB inputs must be set low (the IOTST bit in the Test Mode Select Register may be set to logic 1 in lieu of the TSTB line being asserted) and the following addresses must be written with 00H: 05H, 09H, 0FH, 11H, 25H, 29H, 2FH, 31H.

Reading the following address locations returns the values for the indicated inputs:

PM-1	PM-2	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04H	24H					REF	INEG*	IPOS*	ICLK
10H	30H			LCLK					

Note: *The IPOS and INEG inputs must be clocked in by an ICLK cycle before they can be read. The active edge of ICLK depends of the ICLKINV bit of the Master Configuration Register.

Writing the following address locations forces the outputs to the value in the corresponding bit position:

PM-1	PM-2	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04H	24H	INTB†	LCV	LOS	OHP	MSFP	MFP	ODAT	OCLK
06H	26H		FERF	AIS	IDL	LOSS	LCVS	COFA	SCLK
07H	27H	OOF	FEBE	CPERR	PERR	FERR	ACCLK	DLCLK	ACSIG/ DLSIG
08H	28H							DLEOM	DLINT
0EH	2EH		INTB†						
10H	30H								INTB†

Notes: †Writing a logic 1 to any of the block interrupt signals asserts the INTB output low.

The LCV, LCVS, LOS, LOSS, DLCLK, DLINT, DLSIG, DLEOM, ACCLK, SDAT, ACSIG, SFP outputs can only be forced if they are configured to be presented in normal mode (i.e. the normal mode configuration bits are set appropriately).

The ODAT, LCV, LOS, MFP, MSFP and OHP outputs must be clocked out by the falling edge of OCLK (i.e. write a one and then a zero to the OCLK bit).

DATA LINK RECEIVER OPERATION

On power up of the system, the RDLC should be disabled by setting the EN bit in the Configuration Register to logic 0. The Interrupt Control Register should then be initialized to enable the DLINTx output and to select the FIFO buffer fill level at which an interrupt will be generated. If the INTE bit is not set to logic 1, the Status Register must be continuously polled to check the interrupt status (INTR) bit.

After the Interrupt Control Register has been written, the RDLC can be enabled at any time by setting the EN bit in the Configuration Register to logic 1. When the RDLC is enabled, it will assume the link status is idle (all ones) and immediately begin searching for flags. When the first flag is found, an interrupt will be generated, and a dummy byte will be written into the FIFO buffer. This is done to provide alignment of link up status with the data read from the FIFO. When an abort character is received, another dummy byte and link down status is written into the FIFO. This is done to provide alignment of link down status with the data read from the FIFO. It is up to the controlling processor to check the COLS Status Register bit for a change in the link status. If the COLS Status Register bit is set to logic 1, the FIFO must be emptied to determine the current link status. The first flag and abort status encoded in the PBS bits is used to set and clear a Link Active software flag.

When the last byte of a properly terminated packet is received, an interrupt is generated. While the Status Register is being read the PKIN bit will be logic 1. This can be a signal to the external processor to empty the bytes remaining in the FIFO or to just increment a number-of-packets-received count and wait for the FIFO to fill to a programmable level. Once the Status Register is read, the PKIN bit is cleared to logic 0 . If the Status Register is read immediately after the last packet byte is read from the FIFO, the PBS[2] bit will be logic 1 and the CRC and non-integer byte status can be checked by reading the PBS[1:0] bits.

When the FIFO fill level is exceeded, an interrupt is generated. The FIFO must be emptied to remove this source of interrupt.

The RDLC can be used in a polled, interrupt driven, or DMA-controlled mode for the transfer of frame data. In the polled mode, the DLINTx and DLEOMx outputs are not used, and the processor controlling the RDLC must periodically read the RDLC Status Register to determine when to read the Data Register. In the interrupt driven

mode, the processor controlling the RDLC uses the DLINTx output to determine when to read the RDLC Data Register. In the DMA-controlled mode, the DLINTx output is used as a DMA request input to the DMA controller, and the DLEOMx output is used as an interrupt to the processor to allow handling of exceptions and as an indication of when to process a frame.

In the case of interrupt driven data transfer from the RDLC to the processor, the DLINTx output is connected to the interrupt input of the processor. The processor interrupt service routine should process the data in the following order:

1) RDLC Status Register Read. If INTR=1 then proceed to step 2 else find the interrupt source elsewhere.

2) If OVR = 1, then discard last frame and go to step 1. Overflow causes a reset of FIFO pointers. Any packets that may have been in the FIFO are lost.

3) If COLS = 1, then set the EMPTY FIFO software flag.

4) If PKIN = 1, increment the PACKET COUNT. If the FIFO is desired to be emptied as soon as a complete packet is received, set the EMPTY FIFO software flag. If the EMPTY FIFO software flag is not set, FIFO emptying will delayed until the FIFO fill level is exceeded.

5) RDLC Data Register Read.

6) RDLC Status Register Read.

7) If OVR = 1, then discard last frame and go to step 1. Overflow causes a reset of FIFO pointers. Any packets that may have been in the FIFO are lost.

8) If COLS = 1, then set the EMPTY FIFO software flag.

9) If PKIN = 1, increment the PACKET COUNT. If the FIFO is desired to be emptied as soon as a complete packet is received, set the EMPTY FIFO software flag. If the EMPTY FIFO software flag is not set, FIFO emptying will delayed until the FIFO fill level is exceeded.

10) Start the processing of FIFO data. Use the PBS[2:0] packet byte status bits to decide what is to be done with the FIFO data.

    10.1) If PBS[2:0] = 001, discard data byte read in step 5 and set the LINK ACTIVE software flag.

    10.2) If PBS[2:0] = 010, discard the data byte read in step 5 and clear the LINK ACTIVE software flag.

10.3) If PBS[2:0] = 1XX, store the last byte of the packet, decrement the PACKET COUNT, and check the PBS[1:0] bits for CRC or NVB errors before deciding whether or not to keep the packet.

10.4) If PBS[2:0] = 000, store the packet data.

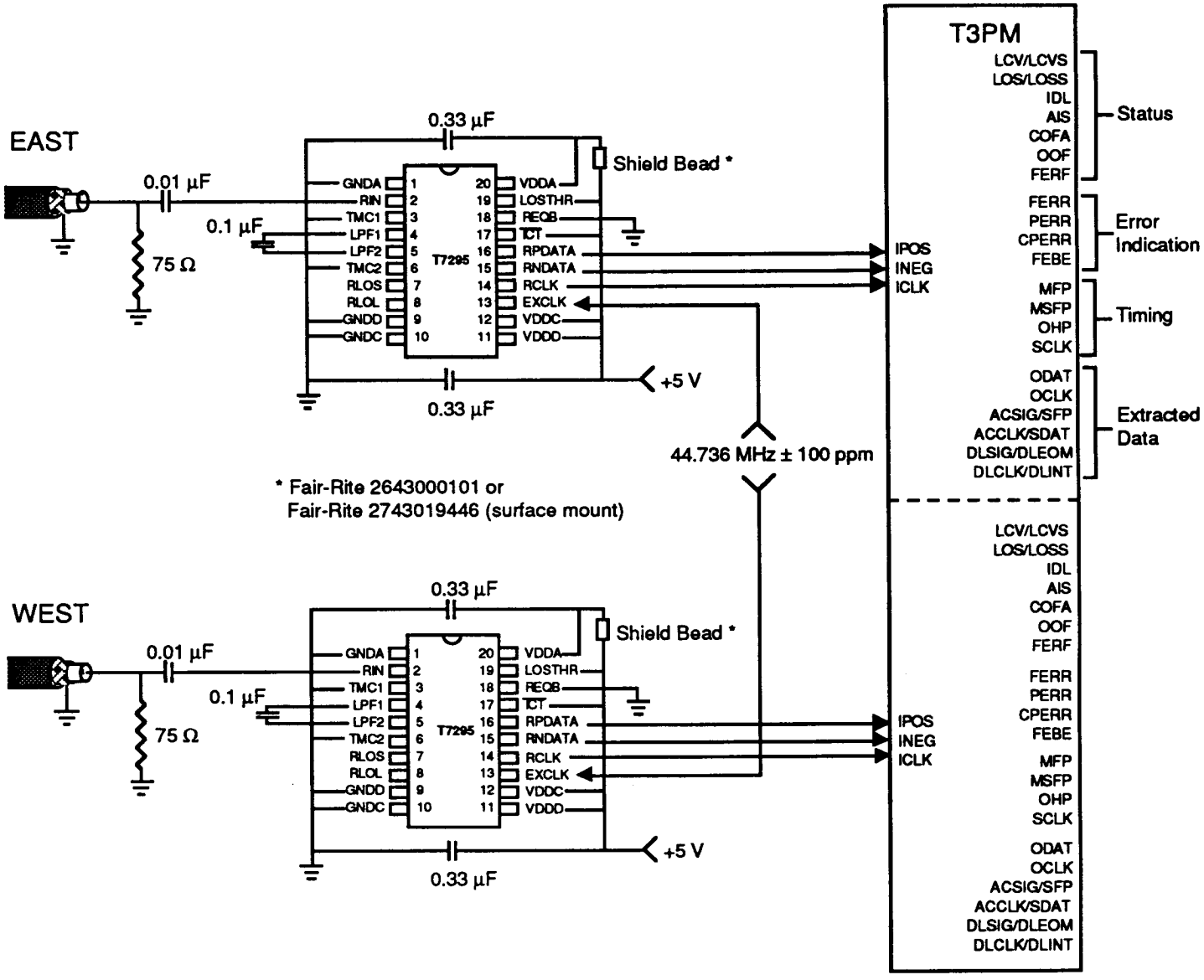
11) If FE = 0 and INTR = 1 or FE = 0 and EMPTY FIFO = 1, go to step 5 else clear the EMPTY FIFO software flag and leave this interrupt service routine to wait for the next interrupt.

The link state is typically a local software variable. The link state is inactive if the RDLC is receiving all ones or receiving bit-oriented codes which contain a sequence of eight ones. The link state is active if the RDLC is receiving flags or data.

If the RDLC data transfer is operating in the polled mode, processor operation is exactly as shown above for the interrupt driven mode, except that the entry to the service routine is from a timer, rather than an interrupt.

The RDLC can also be used with a DMA controller to process the frame data. In this case, the DLEOMx output is connected to the processor interrupt input and the DMAEN bit in the RDLC Configuration Register should be set. The DMA controller reads the data bytes from the RDLC whenever the DLINTx output is high. When the current byte read from the Data Register is the last byte in a frame (due to end-of-message or abort), or an overrun condition occurs, the DLEOMx output is forced to logic 1. When EOM is logic 1, DLINTx is forced to logic 0 via the DMAEN bit gating. As a result, the DMA controller is inhibited from reading any more bytes, and the processor is interrupted. The processor can then halt the DMA controller, read the Status Register, process the frame, and finally reset the DMA controller to process the data for the next frame.

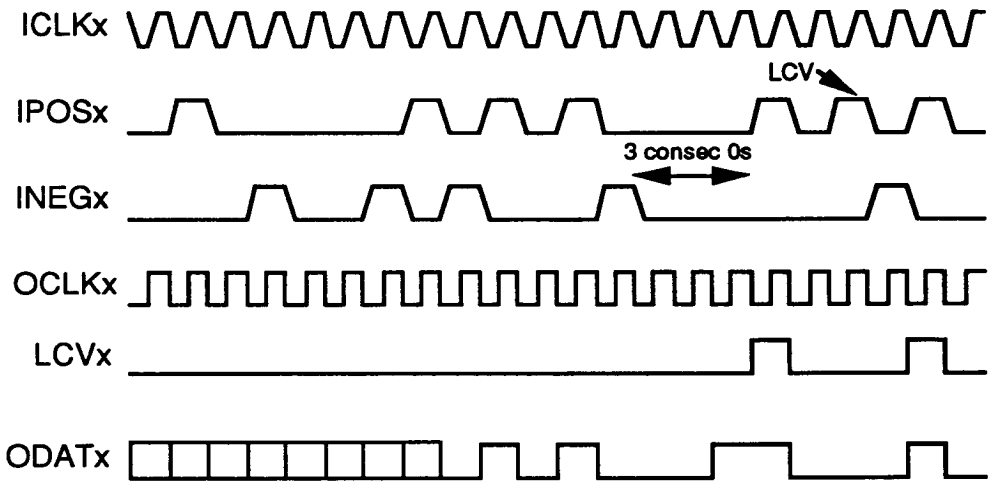
TYPICAL APPLICATION



A typical application showing one T3PM used to monitor a duplex DS3 signal. The analog interface shown is the AT&T T7295 DS3 Integrated Line Receiver. As shown, the analog interface is configured to accept monitor-level signals which are -20 dB from nominal DSX-3 levels.

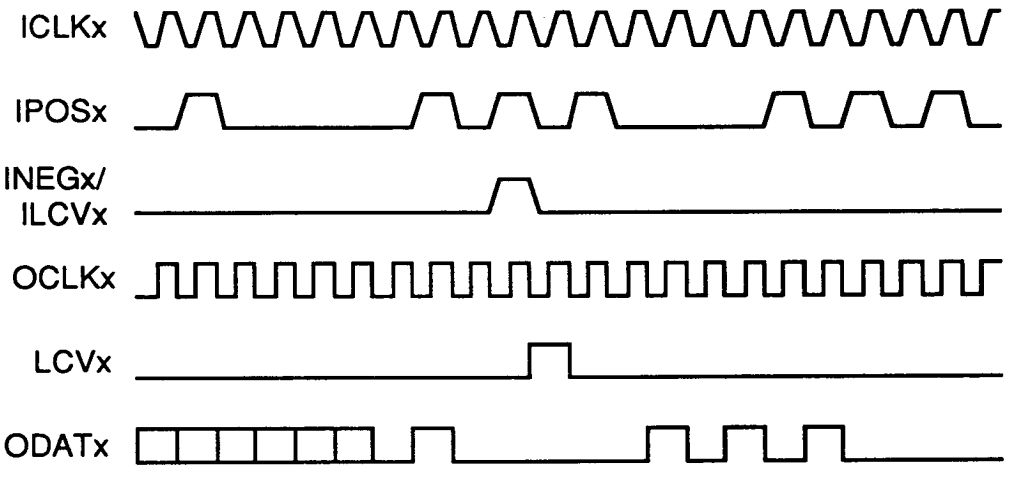
FUNCTIONAL TIMING

Fig. 1 Bipolar DS3 Stream Processing



The Bipolar DS3 Stream Processing timing diagram (figure 1) shows the operation of the FRMR while processing a B3ZS-encoded DS3 stream on inputs IPOSx and INEGx (UNI register bit is set to logic 0). It is assumed that the first bipolar violation (on INEGx) illustrated corresponds to a valid B3ZS signature. The LCV output is set high upon detection of three consecutive zeros in the incoming stream, or upon detection of a bipolar violation which is not part of a valid B3ZS signature. Outputs LCVx and ODATx may be sampled by downstream circuitry using the high speed clock output, OCLKx.

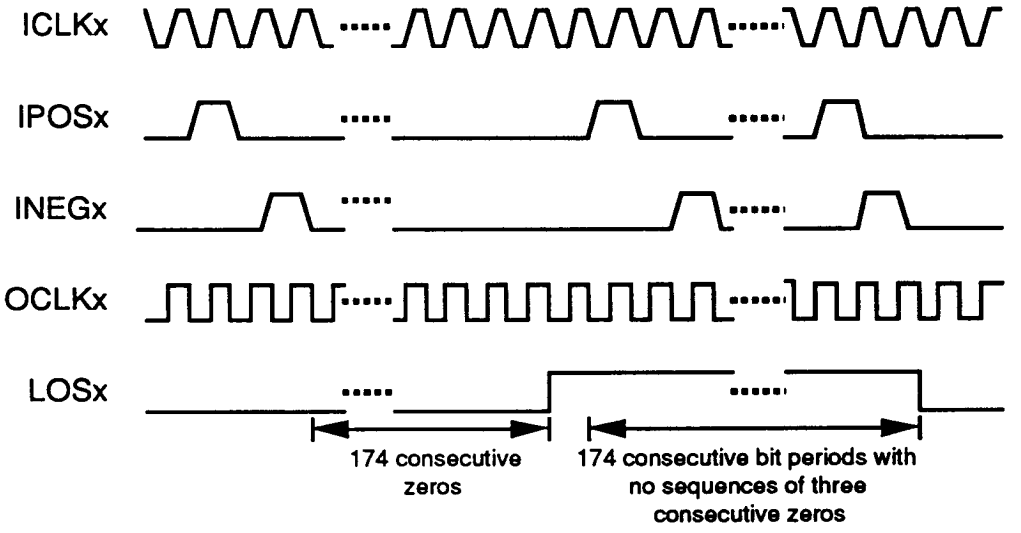
Fig. 2 Unipolar DS3 Stream Processing



The Unipolar DS3 Stream Processing timing diagram (figure 2) shows the operation of the FRMR while processing a DS3 stream on input IPOSx (UNI is set to logic 1). Output ODATx may be sampled by downstream circuitry using the high speed clock output, OCLKx.

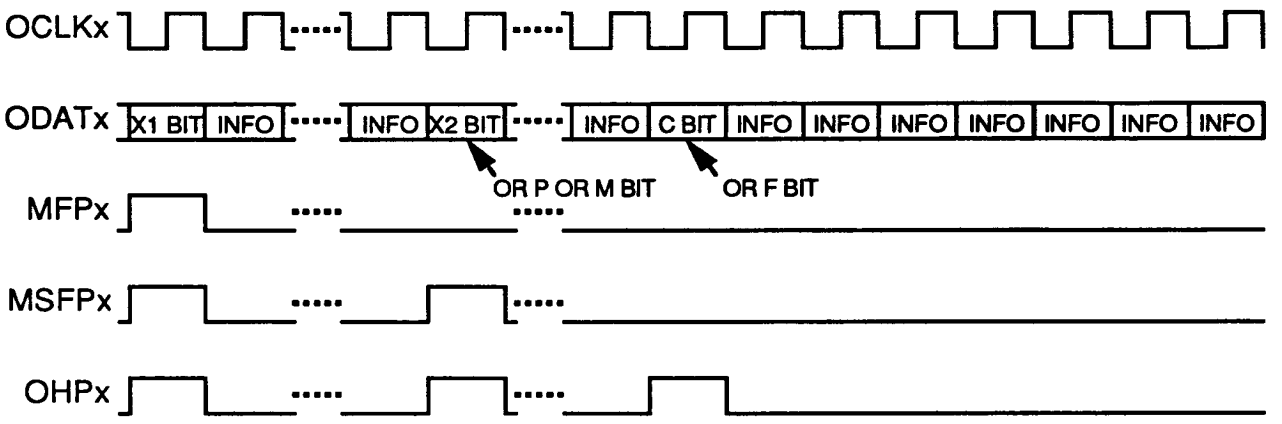
In figure 2, the SUM bit is logic 0 and UNILCV is logic 1, therefore the ILCVx pulses are accumulated by the performance monitor. If the SUM and the UNILCV bits are logic 1, the LCVSx output will only change on the falling edge of SCLKx and is brought high when at least one LCV has been indicated on ILCVx since the last falling edge of SCLKx.

Fig. 3 Loss of Signal



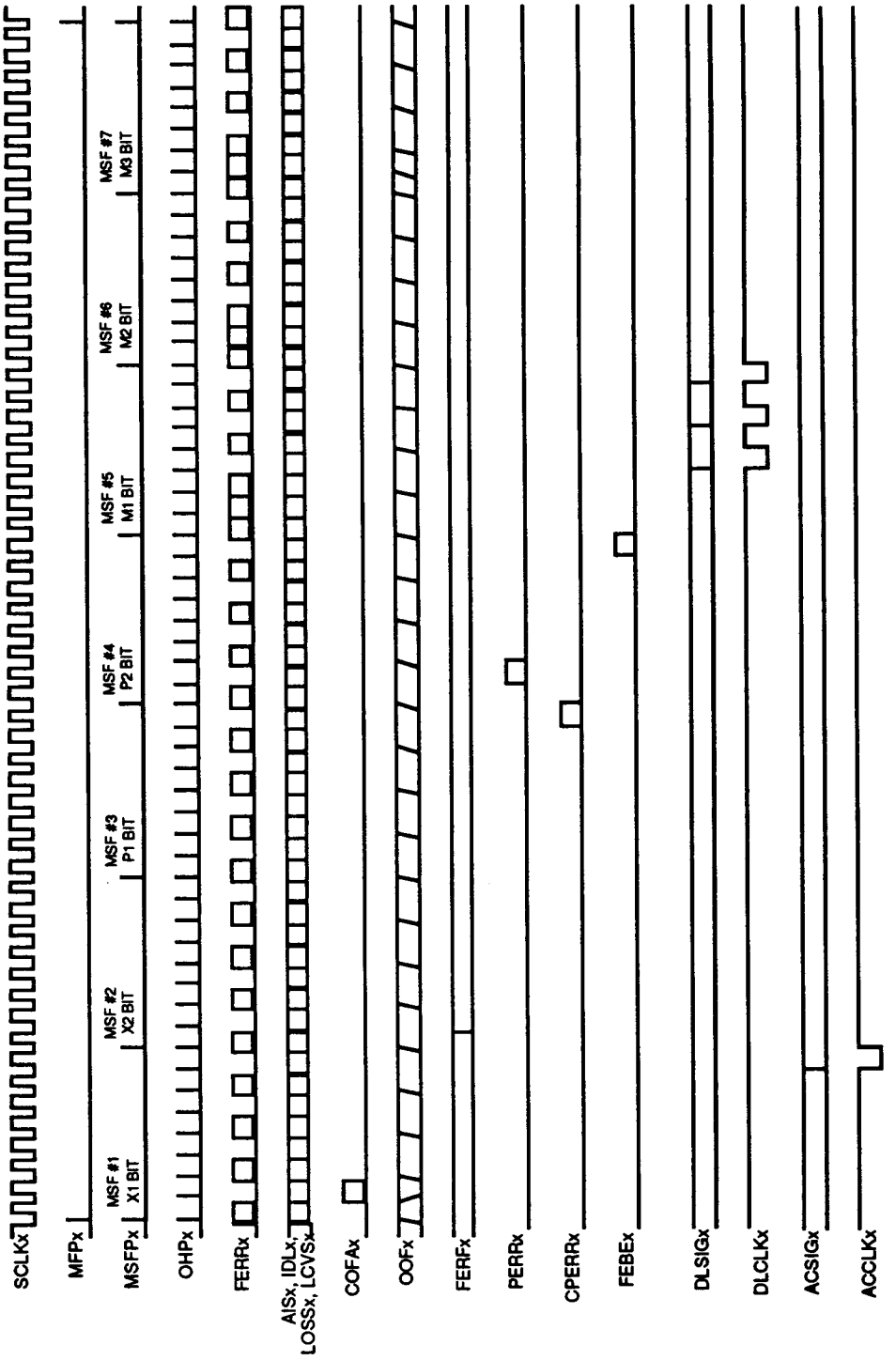
The Loss of Signal timing diagram (figure 3) shows the operation of the loss of signal feature. LOS is set high when 174 consecutive zero bit periods are observed on the IPOS and INEG inputs. LOS is set low when 174 consecutive bit periods containing no sequences of three consecutive zeros (that is, a pulse density greater than 33%) are observed on IPOS and INEG. LOS is closely aligned to the falling edge of OCLK.

Fig. 4 M-Subframe Alignment



The M-subframe timing diagram (figure 4) shows the operation of the M-subframe alignment signals. Output MFPx is set high once per M-frame during the first overhead bit position of M-subframe #1 (the X1 bit position) in the ODATx output stream. Output MSFPx is set high during the first overhead bit position of each M-subframe(the X1, X2, P1, P2, M1, M2, or M3 bit positions) in the ODATx output stream. Output OHPx is set high during each of the overhead bit positions (X, P, M, F, and C bits) in the ODATx output stream.

Fig. 5 M-frame



The M-frame timing diagram (figure 5) shows the operation of the FRMR status outputs. The falling edge of output SCLKx is used to update the status outputs. The SCLKx period is equivalent to the interval between overhead bits in the DS3 stream (85 bit periods).

Outputs AISx, IDLx, LOSSx, and LCVSx are set high if the corresponding pattern/alarm has been detected during the previous SCLKx period.

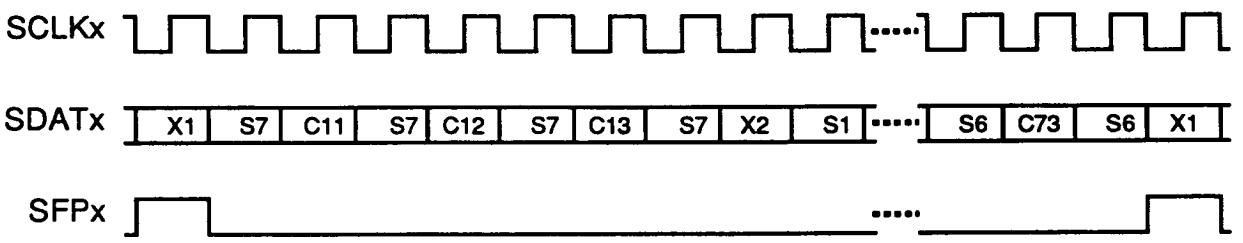
Output OOFx may be set low once per M-frame by the first falling SCLKx edge after the X1 bit position in the ODATx stream. OOFx may be set high by the first falling SCLKx edge after any F-bit or the M3 bit position in the ODATx stream. OOFx is set high when the out-of-frame threshold is exceeded. Output COFAx may pulse high once within an M-frame at the first falling SCLKx edge after the X1 bit position in the ODATx stream.

The FERFx output is updated once per M-frame by the first falling SCLKx edge after the X2 bit position in the ODATx stream.

The PERRx output may pulse high once per M-frame at the first falling SCLKx edge after the P2 bit position in the ODATx stream. The CPERRx and FEBEx outputs are active when C-bit parity mode is enabled. The CPERRx output may pulse high once per M-frame at the first falling SCLKx edge after the C3 bit position in the third M-subframe. The FEBEx output may pulse high once per M-frame at the first falling SCLKx edge after the C3 bit position in the fourth M-subframe. The FERRx output may pulse high up to 31 times per M-frame at the first falling SCLKx edge after the F-bit or M-bit positions in the ODATx stream.

The DLSIGx output are active when C-bit parity mode is enabled. DLSIGx is updated by the first falling SCLKx edge after the C1, C2, and C3 bit positions in the fifth M-subframe. DLCLKx may be used by downstream circuitry to process the values on DLSIGx.

Fig. 6 Overhead Serial Stream



The SFPx pulse occurs during the first block of the M-frame.

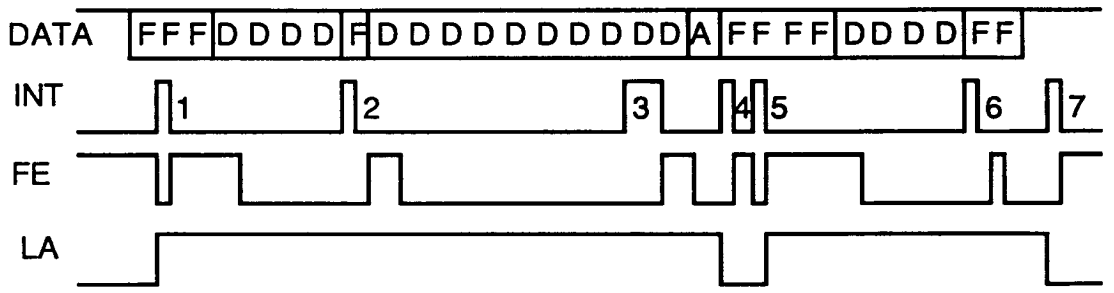
The overhead serial stream is presented in the following format:

	Block							
M-subframe	1	2	3	4	5	6	7	8
1	X_1	S_7	C_{11}	S_7	C_{12}	S_7	C_{13}	S_7
2	X_2	S_1	C_{21}	S_1	C_{22}	S_1	C_{23}	S_1
3	P_1	S_2	C_{31}	S_2	C_{32}	S_2	C_{33}	S_2
4	P_2	S_3	C_{41}	S_3	C_{42}	S_3	C_{43}	S_3
5	M_1	S_4	C_{51}	S_4	C52	S_4	C_{53}	S_4
6	M_2	S_5	C_{61}	S_5	C62	S_5	C_{63}	S_5
7	M_3	S_6	C_{71}	S_6	C72	S_6	C_{73}	S_6

The S_n are the unused stuff-opportunity bits, where "n" is the number of the DS2 input. These uncommitted bits in the C-parity format may be used for proprietary purposes.

The SDATx data becomes valid upon the first SFPx after if the corresponding framer deasserts the out-of-frame (OOF) indication. The data has no meaning when frame alignment has been lost.

Fig. 7 RDLC Example Multi-Packet Operation Sequence



Key to figures 7:

F	- flag sequence (01111110)
A	- abort sequence (01111111)
D	- packet data bytes
INT	- internal interrupt status and state of the active high DLINTx output if enabled
FE	- internal FIFO empty status
LA	- state of the LINK ACTIVE software flag

Figure 7 shows the timing of interrupts, the state of the FIFO, and the state of the Data Link relative the input data sequence. The cause of each interrupt and the processing required at each point is described in the following paragraphs.

This example assumes the FIFO fill level at which an interrupt occurs has been set to 8 bytes.

At points 1 and 5, the first flag after all ones or abort is detected. A dummy byte is written in the FIFO, FE goes low, and an interrupt goes high. When the interrupt is detected by the processor, it reads the dummy byte, the FIFO becomes empty, and the interrupt is removed. The LINK ACTIVE (LA) software flag is set to logic 1.

At points 2 and 6, the last byte of a packet is detected and interrupt goes high. When the interrupt is detected by the processor it reads the data and status registers until the FIFO becomes empty. The interrupt is removed as soon as the Status Register is read since the FIFO fill level of 8 bytes has not been exceeded. It is possible to store many packets in the FIFO and empty the FIFO when the FIFO fill level is exceeded. In either case the processor should use this interrupt to count the number of packets written into the FIFO. The packet count or a software time-out can be used as a signal to empty the FIFO.

At point 3, the FIFO fill level of 8 bytes is exceeded and interrupt goes high. When the interrupt is detected by the processor it must read the data and status registers until the FIFO becomes empty and the interrupt is removed.

At points 4 or 7, an abort character is detected, a dummy byte is written into the FIFO, and interrupt goes high. When the interrupt is detected by the processor it must read the data and status registers until the FIFO becomes empty and the interrupt is removed. The LINK ACTIVE software flag is cleared.

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0°C to +85°C
Storage Temperature	-40°C to +125°C
Voltage on V_{DD} with Respect to GND	-0.5V to +6.0V
Voltage on Any Pin	-0.5V to +6.0V
Static Discharge Voltage	2000 V
Latch-Up Current (T_a = 0°C to +85°C)	400 mA

D.C. CHARACTERISTICS

(T_a = 0°C to +85°C, V_{DD} = 5 V ±10%)

Symbol	Parameter	Min	Max	Unit	Conditions
V_{DD}	Power Supply	4.5	5.5	Volts	
V_{IL} (CMOS)	Input Low Voltage	-0.5	0.3 *V_{DD}	Volts	Guaranteed Input LOW Voltage for ICLK, IPOS and INEG inputs
V_{IH} (CMOS)	Input High Voltage	0.7 *V_{DD}	V_{DD}	Volts	Guaranteed Input HIGH Voltage for ICLK, IPOS and INEG inputs
V_{IL} (TTL)	Input Low Voltage	-0.5	0.8	Volts	Guaranteed Input LOW Voltage for other inputs
V_{IH} (TTL)	Input High Voltage	2.0	V_{DD}	Volts	Guaranteed Input HIGH Voltage for other inputs
V_{OL}	Output or Bidirectional Low Voltage		0.4	Volts	V_{DD} = min, I_{OL} = 4 mA for data bus pins, OCLK, ODAT, MFP, MSFP, OHP, LCV and INTB and 2 mA for others

V_{OH}	Output or Bidirectional High Voltage	2.4		Volts	V_{DD} = min, I_{OL} = 4 mA for data bus pins, OCLK, ODAT, MFP, MSFP, OHP, LCV and INTB and 2 mA for others
V_T	Reset Input High Voltage	2.3	2.8	Volts	
V_{TH}	Reset Input Hysteresis Voltage	0.5	1.2	Volts	
I_{ILPU}	Input Low Current	-26	-110	µA	$V_{IL} \leq 1.65$ V, Notes 1, 3
I_{IHPU}	Input High Current	-48	-110	µA	$V_{IH} \geq 3.85$ V, Notes 1, 3
I_{IL}	Input Low Current	-10	0	µA	$V_{IL} \leq 1.65$ V, Notes 2, 3
I_{IH}	Input High Current	-10	10	µA	$V_{IH} \geq 3.85$ V, Notes 2, 3
I_{DDOP}	Active Current		200	mA	V_{DD}=5.5V, Outputs Unloaded at TSB Nominal Operating Frequencies
I_{DDSB}	Idle Current		500	µA	V_{DD}=5.5 V, Outputs Unloaded, Device Unclocked.

Notes on D.C. Characteristics:

1. Input pin or bidirectional pin with internal pull-up resistors.
2. Input pin or bidirectional pin without internal pull-up resistors
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

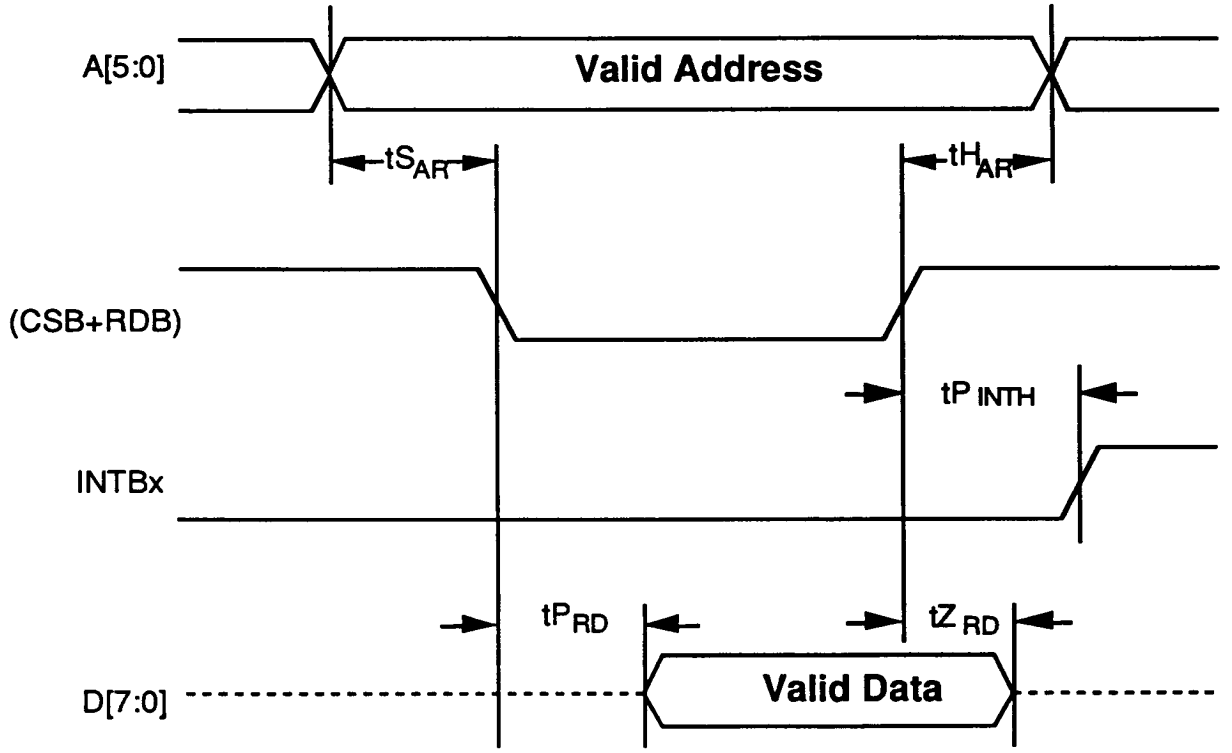
(T_a = 0°C to +85°C, V_{DD} = 5 V ±10%)

External Read Access (Fig. 8)

Symbol	Parameter	Min	Max	Units
t_{CYC}	Read cycle time	240*		ns
tS_{AR}	Address to Valid Read Set-up Time	20		ns
tH_{AR}	Address to Valid Read Hold Time	20		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		100	ns
tZ_{RD}	Valid Read Deasserted to Output Tri-state		40	ns
tP_{INTH}	Valid Read Deasserted to Interrupt Deasserted		100	ns

* The read cycle time is limited by the RDLC TSB access time. Ten ICLK periods are required between the falling edges of RDB to allow the FIFO time to process a read request. Other read accesses require only a 140 ns cycle.

Fig. 8 External Read Access Timing



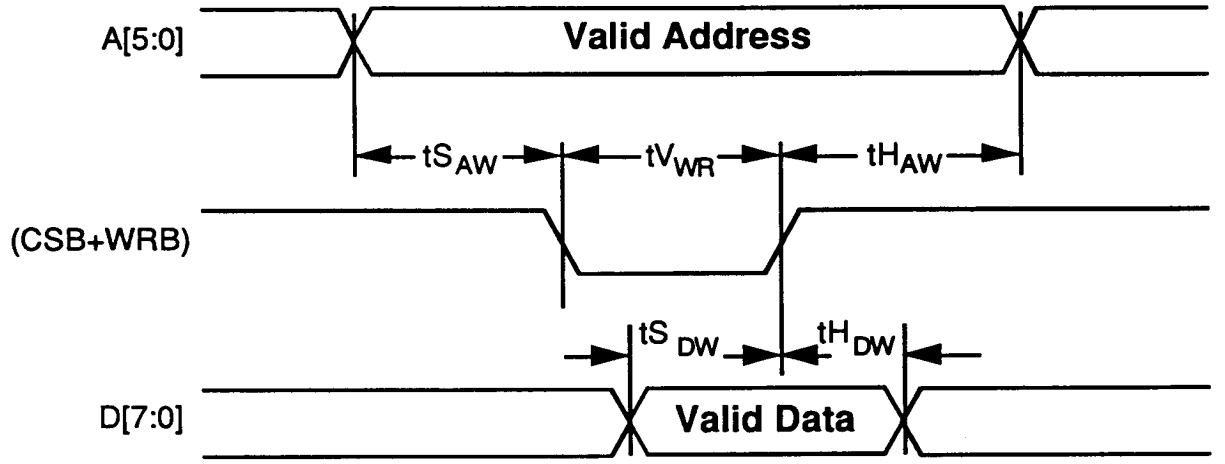
Notes on External Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 50% point of the reference signal to the 30% or 70% point of the output.
2. Maximum output propagation delays are measured with a 50 pF load on the data bus, (D[7:0]).
3. A valid read cycle is defined as the logical OR of the CSB and the RDB signals.
4. The microprocessor timing applies to normal mode register accesses only.

External Write Access (Fig. 9)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	20		ns
tS_{DW}	Data to Valid Write Set-up Time	40		ns
tH_{DW}	Data to Valid Write Hold Time	30		ns
tH_{AW}	Address to Valid Write Hold Time	20		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Fig. 9 External Write Access Timing



Notes on External Write Timing:

1. A valid write cycle is defined as the logical OR of the CSB and the WRB signals.
2. The microprocessor timing applies to normal mode register accesses only.

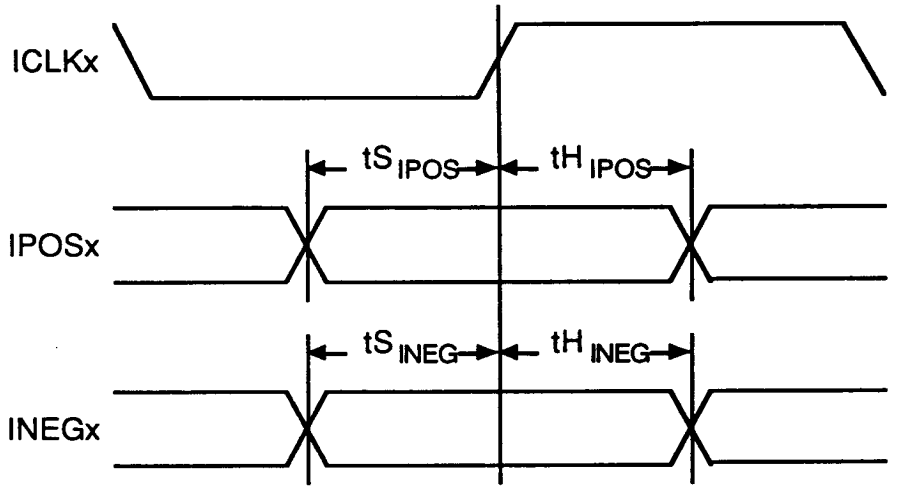
T3PM TIMING CHARACTERISTICS

(T_a = 0°C to +85°C, V_{DD} = 5 V ±10%)

T3PM Input (Fig. 10)

Symbol	Description	Min	Max	Units
	ICLK Frequency (nominally 44.736 MHz)		45	MHz
	ICLK Duty Cycle	40	60	%
tS_{IPOS}	IPOSx Set-up Time	5		ns
tS_{INEG}	INEGx Set-up Time	5		ns
tH_{IPOS}	IPOSx Hold Time	7		ns
tH_{INEG}	INEGx Hold Time	7		ns

Fig. 10 Input Timing



Notes on Input Timing:

1. If the ICLKINV bit of the Master Configuration register is a logic 1, then setup and hold times are relative to the falling edge of ICLK instead of the rising edge as shown here.

2. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 50% point of the input to the 50% point of the clock.

3. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 50% point of the clock to the 50% point of the input.

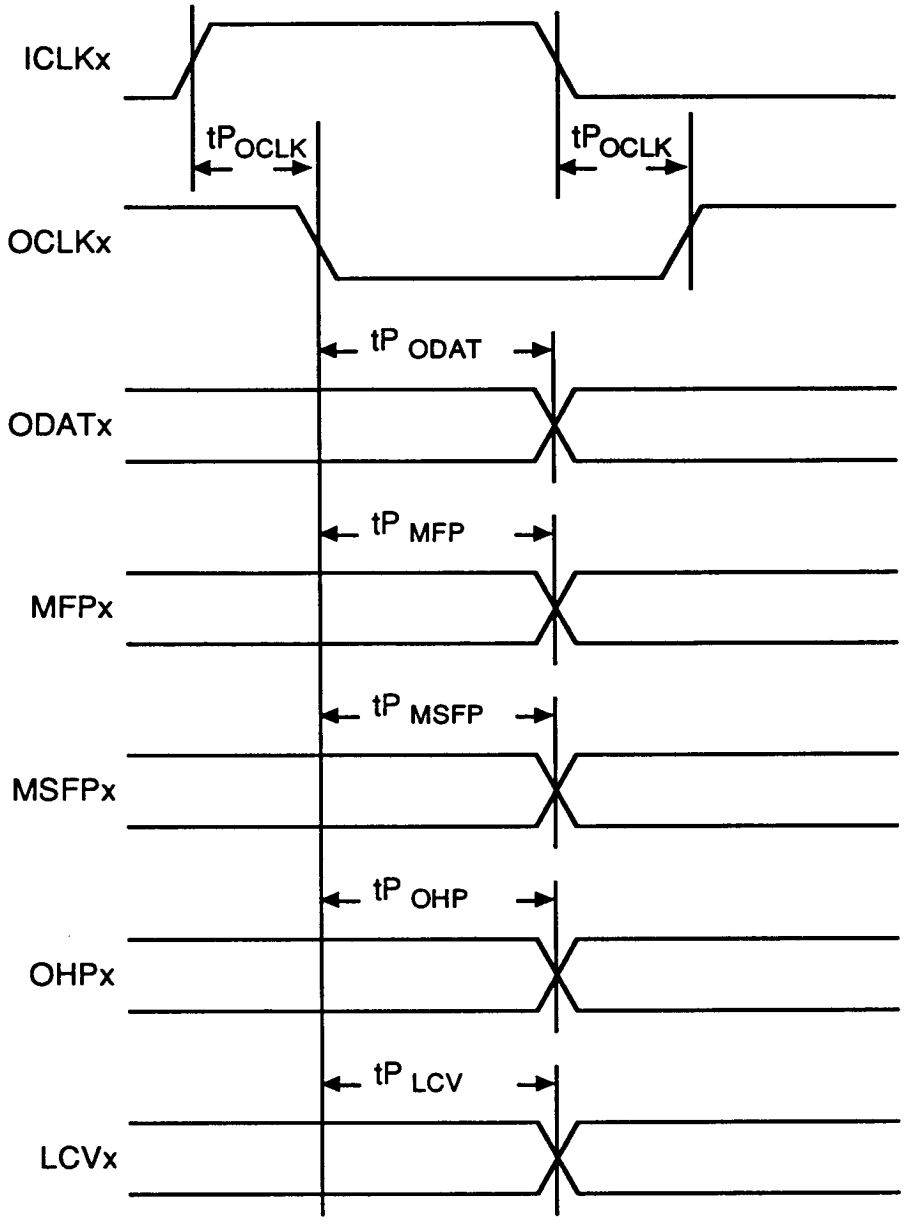
T3PM Output (Fig. 11, 12, 13, 14, & 15)

Symbol	Description	Min	Max	Units
tP_{OCLK}	ICLK Edge to OCLK Edge Propagation Delay	10	50	ns
tP_{ODAT}	OCLK Low to ODAT Valid Propagation Delay	-4	4	ns
tP_{MFP}	OCLK Low to MFP Valid Propagation Delay	-4	4	ns
tP_{MSFP}	OCLK Low to MSFP Valid Propagation Delay	-4	4	ns
tP_{OHP}	OCLK Low to OHP Valid Propagation Delay	-4	4	ns
tP_{LCV}	OCLK Low to LCV Valid Propagation Delay	1	8	ns
tP_{OOF}	SCLK Low to OOF Valid Propagation Delay		70	ns
tP_{COFA}	SCLK Low to COFA Valid Propagation Delay		70	ns
tP_{LCVS}	SCLK Low to LCVS Valid Propagation Delay		70	ns
tP_{LOSS}	SCLK Low to LOSS Valid Propagation Delay		70	ns
tP_{AIS}	SCLK Low to AIS Valid Propagation Delay		70	ns
tP_{IDL}	SCLK Low to IDL Valid Propagation Delay		70	ns
tP_{FERF}	SCLK Low to FERF Valid Propagation Delay		70	ns
tP_{FERR}	SCLK Low to FERR Valid Propagation Delay		70	ns
tP_{PERR}	SCLK Low to PERR Valid Propagation Delay		70	ns
tP_{CPERR}	SCLK Low to CPERR Valid Propagation Delay		70	ns
tP_{FEBE}	SCLK Low to FEBE Valid Propagation Delay		70	ns
tP_{SDAT}	SCLK Low to SDAT Valid Propagation Delay		70	ns
tP_{SFP}	SCLK Low to SFP Valid Propagation Delay		70	ns
tP_{DLSIG}	DLCLK Low to DLSIG Valid Propagation Delay		70	ns
$tP_{DLINTL1}$	RDB Low to DLINT Low Propagation Delay on RDLC Data Register Read		200*	ns
$tP_{DLINTL2}$	RDB High to DLINT Low Propagation Delay on RDLC Status Register Read		80	ns

Symbol	Description	Min	Max	Units
tP_{DLINTH}	DLCLK Low to DLINT High Propagation Delay		400*	ns
tPEINTH	DLEOM High to DLINT Low Propagation Delay		50	ns
tPEINTL	DLEOM Low to DLINT High Propagation Delay		50	ns
tP_{EOML}	RDB High to DLEOM Low Propagation Delay		80	ns
tP_{EOMH}	RDB Low to DLEOM High Propagation Delay		80	ns

* Several high speed clock cycles (period of 44.7 ns) are required to process this event, thus the long delay.

Fig. 11 OCLKx Based Output Timing



Notes on OCLKx Based Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 50% point of the reference signal to the 30% or 70% point of the output.

2. Maximum output propagation delays are measured with a 30 pF load on the outputs. The variance in the delay of signals relative to OCLK will depend on the external loads.

3. The OCLKx phase relationship to ICLKx is shown for the case where the ICLKINV bit is a logic 0. If the ICLKINV bit is logic 1, ICLKx would be inverted with respect to the levels shown here.

Fig. 12 SCLKx Based Output Timing

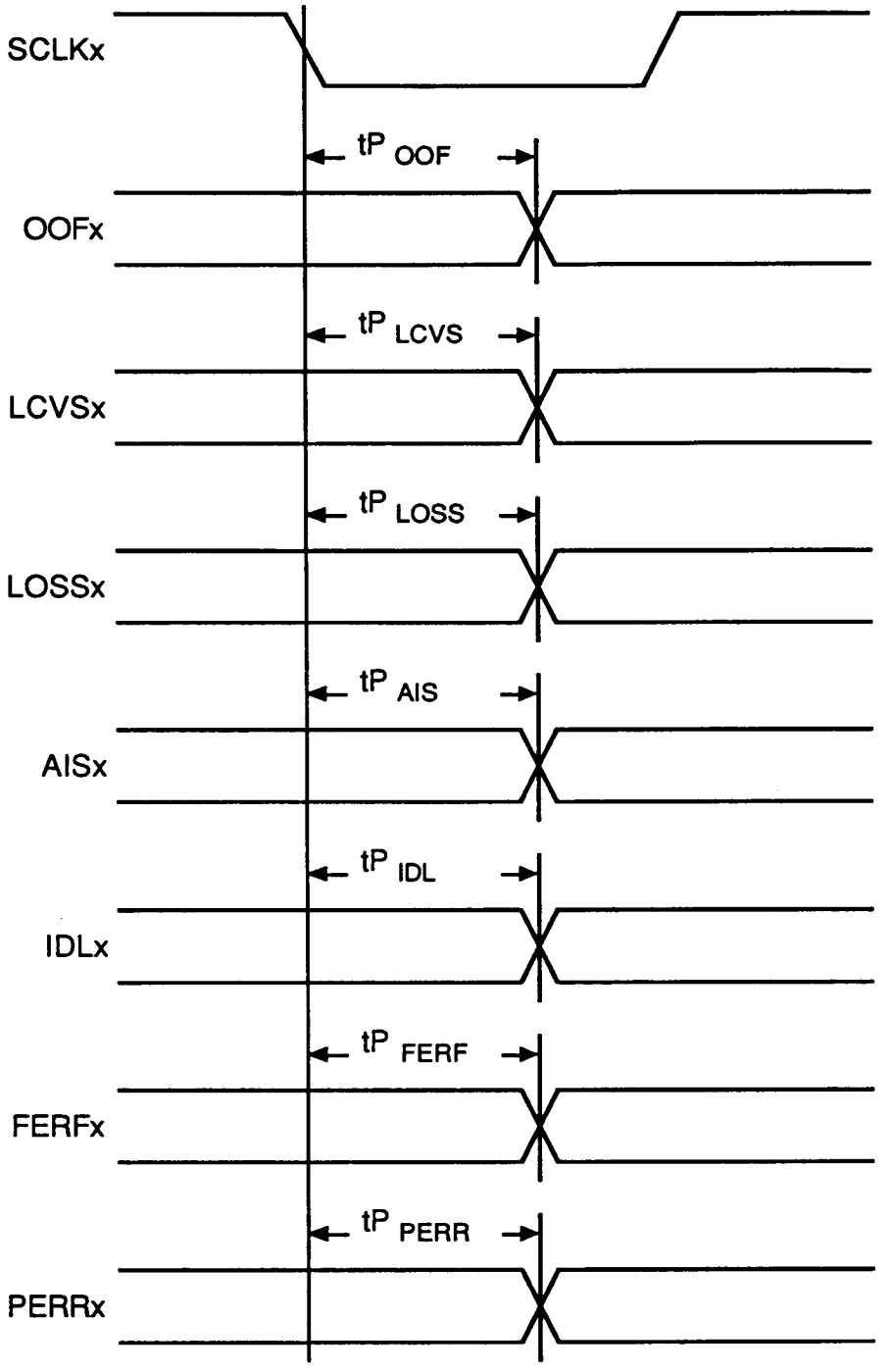
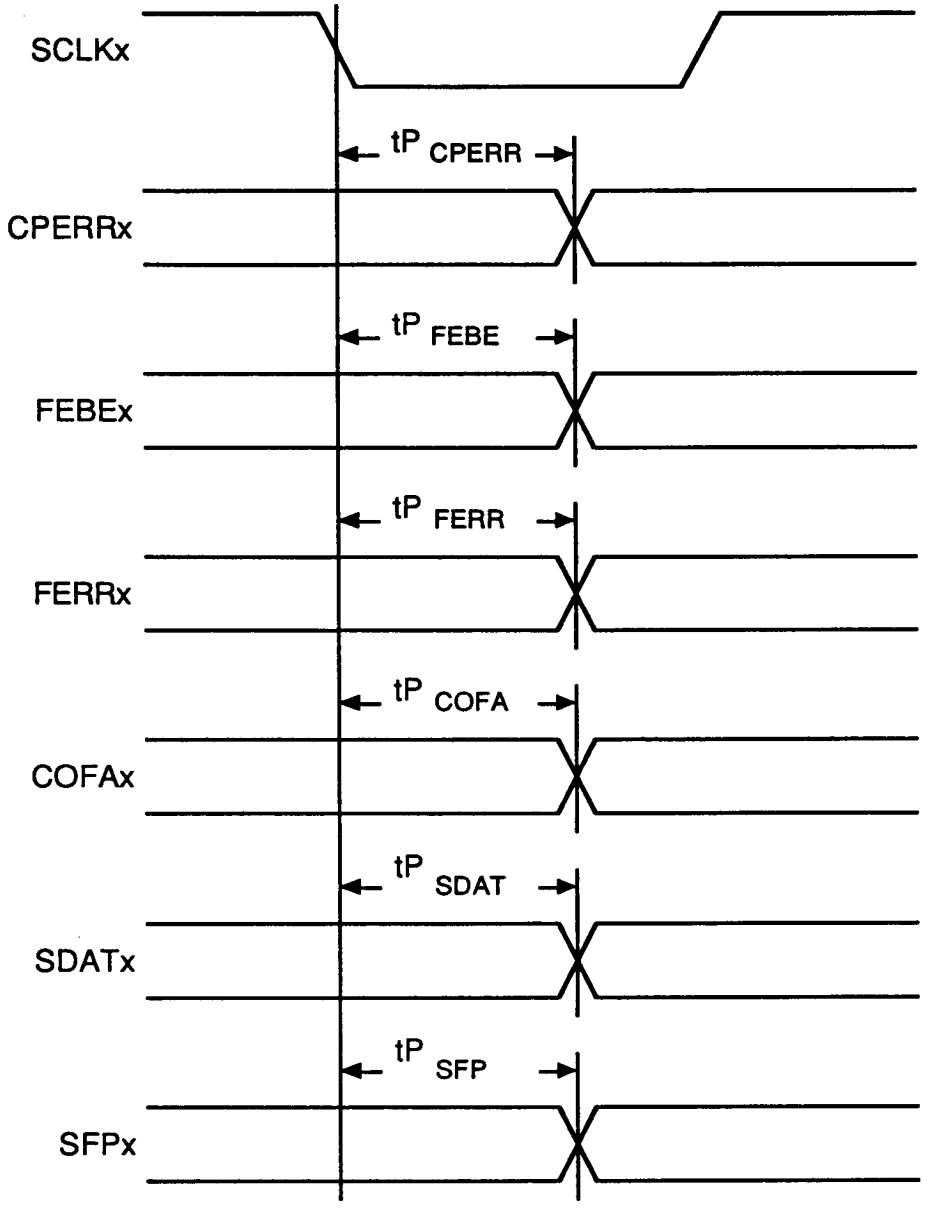


Fig. 12 SCLKx Based Output Timing (cont.)



Notes on SCLKx Based Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 50% point of the reference signal to the 30% or 70% point of the output.

2. Maximum output propagation delays are measured with a 50 pF load on the outputs.

Fig. 13 Data Link Clock and Signal Timing

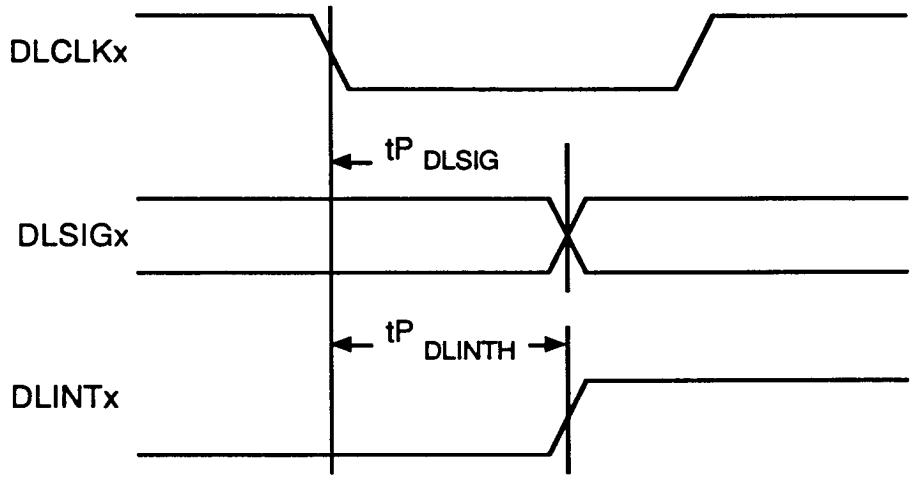


Fig. 14 HDLC DMA Mode Timing

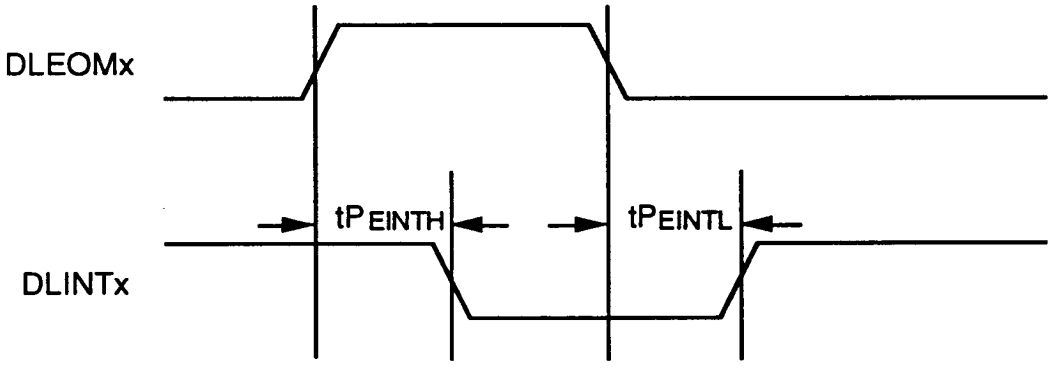
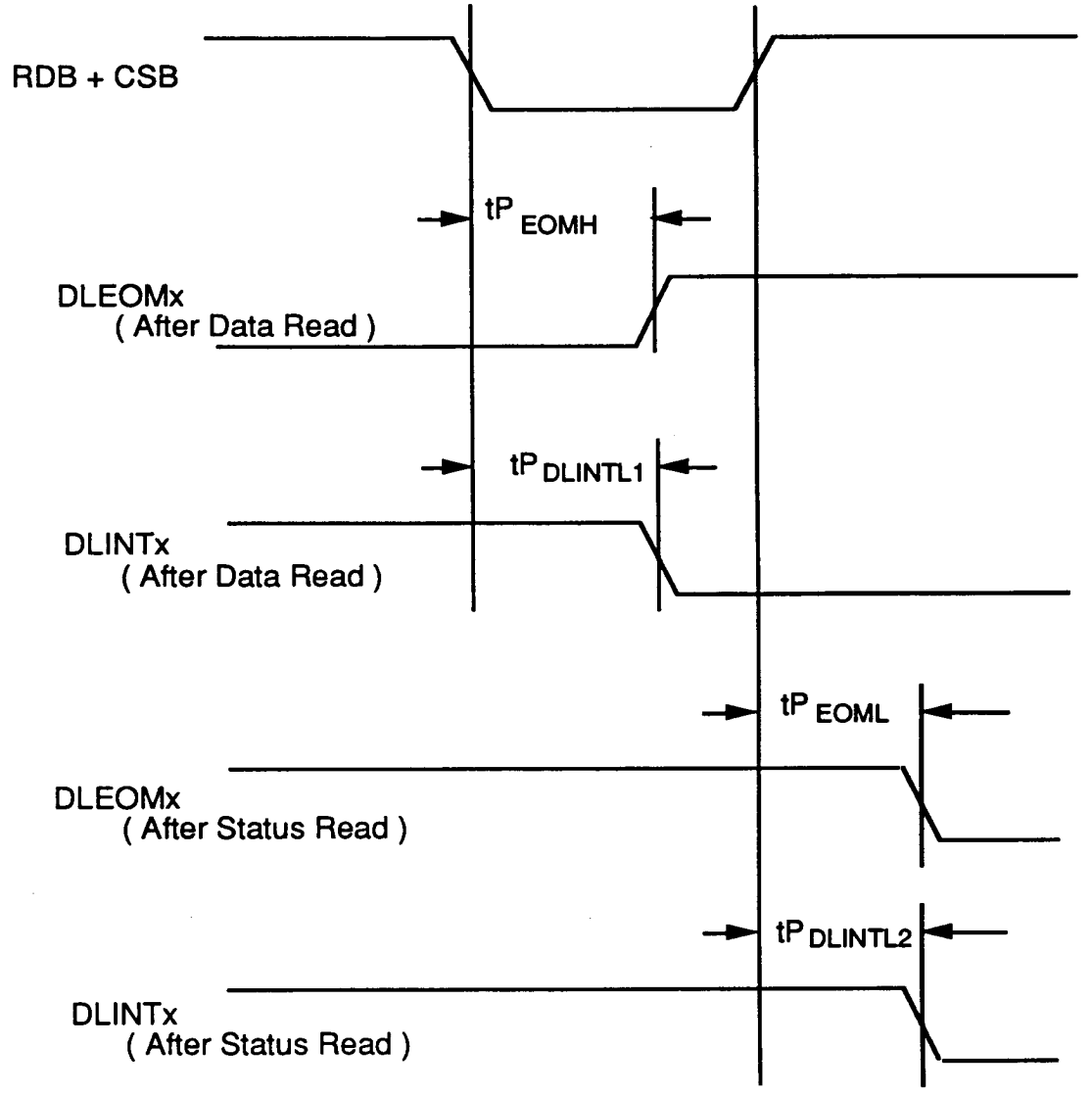


Fig. 15 HDLC Receiver Microprocessor Associated Timing



Notes on HDLC Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 50% point of the reference signal to the 30% or 70% point of the output.
2. Maximum output propagation delays are measured with a 50 pF load on the outputs.

MECHANICAL DATA

Devices are packaged in a 84 pin PLCC (plastic leaded chip carrier).

Critical dimension drawings for this package type are available in the VLSI Technology, Inc. "Package Selection Guide".

NOTES

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