Features

- **Comprehensive Library of Standard Logic Cells**
- **ATC25 I/O Cells Designed to Operate with V_{DD} = 2.5V ± 0.25V as Main Target Operating Conditions**
- **IO33 Pad Library Provides Interface to 3V Environment**
- **Oscillators Provide Stable Clock Sources**
- **Basic Analog Input/Output, Power, Ground and Multiplexer Cells Available, High-performance Analog Cells Can Be Developed on Request**
- **Memory Cells Compiled to the Precise Requirements of the Design**
- **Compatible with Atmel's Extensive Range of Microcontroller, DSP, Standard Interface and Application Specific Cells**

Description

The Atmel ATC25 CBIC family is fabricated on a proprietary 0.25 micron five-layer-metal CMOS process intended for use with a supply voltage of 2.5V ± 0.25V. The following table shows the range for which Atmel library cells have been characterized.

Table 1. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	DC Supply Voltage	Core and Standard I/Os	2.25	2.5	2.75	V
V_{DD3}	DC Supply Voltage	3V Interface I/Os	3	3.3	3.6	V
V_I	DC Input Voltage		0		V_{DD}	V
V_O	DC Output Voltage		0		V_{DD}	V
TEMP	Operating Free Air Temperature Range	Industrial	-40		+85	°C

The Atmel cell libraries and megacell compilers have been designed in order to be compatible with each other. Simulation representations exist for three types of operating conditions; they correspond to three characterization conditions defined as follows:

- MIN conditions:
  T_J = -40°C
  V_{DD} (cell) = 2.75V
  Process = fast (industrial best case)
- TYP conditions:
  T_J = +25°C
  V_{DD} (cell) = 2.5V
  Process = typ (industrial typical case)
- MAX conditions:
  T_J = +100°C
  V_{DD} (cell) = 2.25V
  Process = slow (industrial worst case)

Delays to tri-state are defined as delay to turn off (VGS < VT) of the driving devices. Output pad drain current corresponds to the output current of the pad when the output voltage is V_{OL} or V_{OH}. The output resistor of the pad and the voltage drop due to access resistors (in and out of the die) are taken into account. In order to have accurate timing estimates, all characterization has been run on electrical netlists extracted from the layout database.

Cell-based ASIC

ATC25

Summary

Rev. 1306DS–CBIC–09/02

Standard Cell Library SClib

The Atmel Standard Cell Library, SClib, contains a comprehensive set of combinational logic and storage cells. The SClib library includes cells which belong to the following categories:

- Buffers and Gates
- Multiplexers
- Flip-flops
- Scan Flip-flops
- Latches
- Adders and Subtractors

Decoding the Cell Name

The table below shows the naming conventions for the cells in the SClib library. Each cell name begins with either a two-, three-, or four-letter code that defines the type of cell. This indicates the range of standard cells available.

Table 2. Cell Codes

Code	Description	Code	Description
AD	Adder	INVT	Inverting 3-State Buffer
AH	Half Adder	JK	JK Flip-Flop
AS	Adder/Subtractor	LA	D Latch
AN	AND Gate	MI	Inverting Multiplexer
AOI	AND-OR-Invert Gate	MX	Multiplexer
AON	AND-OR-AND-Invert Gates	ND	NAND Gate
AOR	AND-OR Gate	NR	NOR Gate
BH	Bus Holder	OAI	OR-AND-Invert Gate
BUFB	Balanced Buffer	OAN	OR-AND-OR-Invert Gates
BUFF	Non-Inverting Buffer	OR	OR Gate
BUFT	Non-Inverting 3-State Buffer	ORA	OR-AND Gate
CG	Carry Generator	SD	Multiplexed Scan D Flip-Flop
CLK2	Clock Buffer	SE	Multiplexed Scan Enable D Flip-Flop
DE	D-Enabled Flip-Flop	SRLA	Set/Reset Latches with NAND input
DF	D Flip-Flop	SU	Subtractor
INV0	Inverter	XN	Exclusive NOR Gate
INVB	Balanced Inverter	XR	Exclusive OR Gate

Cell Matrices

The following three tables provide a quick reference to the storage elements in the SClib library. Note that all storage elements feature buffered clock inputs and buffered output.

Table 3. JK Flip-flops

Macro Name	Set	Clear	1x Drive	2x Drive
JKBRBx	•	•	•	•

Table 4. D Flip-flops

Macro Name	Set	Clear	Enabled D Input	1x Drive	2x Drive	Single Output
DFBRBx	•	•		•	•	
DFCRBx		•		•	•	
DFCRQx		•		•	•	•
DFCRNx		•		•	•	
DFNRBx				•	•	
DFNRQx				•	•	•
DFPRBx	•			•	•	
DEPRQx	•		•	•	•	•
DENRQx			•	•	•	•
DENRBx			•	•	•	
DECRQx		•	•	•	•	•

Table 5. Scan Flip-flops

Macro Name	Set	Clear	1x Drive	2x Drive	Single Output
SDBRBx	•	•	•	•	
SDCRBx		•	•	•	
SDCRNx		•	•	•	•
SDCRQx		•	•	•	•
SDNRBx			•	•	
SDNRNx			•	•	•
SDNRQx			•	•	•
SDPRBx	•		•	•	
SECRQx		•	•	•	•
SENRQx			•	•	•
SEPRQx	•		•	•	•

Input/Output Pad Cell Libraries IO25lib and IO33lib

The Atmel Input/Output Cell Library, IO25lib, contains a comprehensive list of input, output, bidirectional and tristate cells. The ATC25 (2.5V) cell library includes a special set of I/O cells, IO33lib, for interfacing with external 3V devices.

Voltage Levels

The IO25lib library is made up exclusively of low-voltage chip interface circuits powered by a voltage in the range of 2.25V to 2.75V. The library is compatible with the SClib 2.5-volt standard cells library.

Power and Ground Pads

Designers are strongly encouraged to provide three kinds of power pairs for the IO25lib library. These are “AC”, “DC” and core power pairs. AC power is used by the I/O to switch its output from one state to the other. This switching generates noise in the AC power buses on the chip. DC power is used by the I/O to maintain its output in a steady state. The best noise performance is achieved when the DC power buses on the chip are free of noise; designers are encouraged to use separate power pairs for AC and DC power to prevent most of the noise in the AC power buses from reaching the DC power buses. The same power pairs can be used to supply both DC power to the I/Os and power to the core without affecting noise performance.

Table 6. VSS Power Pad Combinations

Core	Switching I/O	Quiet I/O	Library Cell Name	Signal Name
Vssi	VssAC	VssDC		
•			pv25i00	VSS
	•		pv25a00	VSS
		•	pv25d00	VSS
	•	•	pv25e00	VSS
•		•	pv25b00	VSS
•	•	•	pv25f00	VSS

Table 7. VDD Power Pad Combinations

Core	Switching I/O	Quiet I/O	Library Cell Name	Signal Name
Vddi	VddAC	VddDC		
•			pv25i25	VDD
	•		pv25a25	VDD
		•	pv25d25	VDD
	•	•	pv25e25	VDD
•		•	pv25b25	VDD
•	•	•	pv25f25	VDD

Cell Matrices

Table 8. CMOS Pads

CMOS Cell Name	3-State I/O	Output Only	3-State Output Only	Drive Strength	Pad Sites Used
PC25B01	•			1x	1
PC25B02	•			2x	1
PC25B03	•			3x	1
PC25B04	•			4x	1
PC25B05	•			5x	1
PC25O01		•		1x	1
PC25O02		•		2x	1
PC25O03		•		3x	1
PC25O04		•		4x	1
PC25O05		•		5x	1
PC25T01			•	1x	1
PC25T02			•	2x	1
PC25T03			•	3x	1
PC25T04			•	4x	1
PC25T05			•	5x	1

Table 9. TTL Pads

TTL Cell Name	3-State I/O	Output Only	3-State Output Only	Drive Strength	Pad Sites Used
PT25B01	•			2 mA	1
PT25B02	•			4 mA	1
PT25B03	•			8 mA	1
PT25O01		•		2 mA	1
PT25O02		•		4 mA	1
PT25O03		•		8 mA	1
PT25T01			•	2 mA	1
PT25T02			•	4 mA	1
PT25T03			•	8 mA	1

Table 10. CMOS/TTL Input Only Pad

CMOS Cell Name	Input Levels	Schmitt Input Level Shifter	Non-Inverting	Inverting	Pad Sites Used
PC25D01	CMOS		•		1
PC25D11	CMOS			•	1
PC25D21	CMOS	•	•		1
PC25D31	CMOS	•		•	1

Note: All 3-state I/Os, 3-state output only and input pads are also available with pull-up and pull-down device.

IO33lib Low Slew Rate Cells

The IO33lib cells comprise a series of 2.5V/3.3V input/output pads developed for low supply voltage processes in order to interface 2.5V ASICs to 3.3V environments.

All IO33lib cells are slew rate controlled. Advantage has been taken of the 2.5V to 3.3V level shifter (slow by construction) to reduce the slew rate without reducing speed.

Table 11. IO33lib Pads

3V Interface Pad Name	3-State I/O	Output Only	3-State Output Only	Input Only	Drive Strength	Pad Sites Used
pc33b0x	•				2 mA, 4 mA, 8 mA, 16 mA	1
pc33d00				•		1
pc33o0x		•			2 mA, 4 mA, 8 mA, 16 mA	1
pc33t0x			•		2 mA, 4 mA, 8 mA, 16 mA	1

Note: All 3-state I/Os, 3-state output only and input pads are also available with pull-up and pull-down device.

Table 12. IO33lib Power Pads

Cell Name	Power Bus Connections				Pad Sites Used
	vssi	mixvss	vddi	mixvdd	
pv33e00		•			1
pv33i00	•				1
pv33i25			•		1
pv33e33				•	1
pv33ecrn		•		•	2

Oscillator Cell Library Osc25lib

The Atmel Oscillator Library provides stable clock sources. It comprises four oscillators and one power-on-reset.

Crystal Oscillators

The Atmel two-pad oscillators are designed with the Pierce three-point oscillator structure. For the 32.768 Hz oscillator, the load capacitance must be between 6 pF and 12.5 pF For high-frequency oscillators, the load capactance must be between 15 pF and 20 pF. External capacitors must be added in order to obtain the correct load capacitance.

Clock output is high at off state (onosc = 0).

The oscillators provide a bypass mode (onosc = 1), clock = not (xin).

Table 13 gives the available oscillator cells.

Table 13. Oscillator and POR Cells

Cell Name	Description
OSC25f33K	Low-power, optimized for 32.786 kHz crystal
OSC25f9M	9 MHz crystal oscillator
OSC25f16M	16 MHz crystal oscillator
OSC25f27M	27 MHz crystal oscillator
POR25	Static and dynamic reset with internal hysterisis

Basic Analog Cell Library ANA25lib, ANA33lib

The Atmel CBIC analog library makes the following parts available:

- Multiplexer modules
  - Multiplexers to minimize cross-talk (for use with high-impedance nodes).
  - Multiplexers to minimize ON resistance.
- Analog input and output cells
- Analog power and ground cells

A special set of basic analog I/O cells, ANA33lib, is available for interfacing with external 3.3V devices.

Atmel Compiled Megacell Library

The Atmel Compiled Megacell Library enables compilation of megacells for the functions Synchronous RAM, High-range Synchronous RAM, Asynchronous RAM, Asynchronous Dual-port RAM, Asynchronous Two-port RAM and Synchronous ROM, according to the user's precise requirements.

The Atmel megacells can be instanced as often as required in designs and can be used in parallel with cells from all other Atmel CBIC libraries. All the megacell representations required for schematic entry, simulation, place and route, layout generation, and verification are created automatically.

Compiled Synchronous RAM Megacells

The Atmel Synchronous RAM compiler has bidirectional or separate I/O ports, and can be configured in multi-bank form, with a maximum of four banks.

The range of permitted Synchronous RAM megacell configurations is as follows:

```
Number of bits   128, .. 144K bits
Number of words  32, .. 8K
Word Size        4, .. 36 bits
```

The following table shows the range of performances for particular Synchronous RAM configurations under typical conditions.

Configuration	1K x 8 (8K bits)	2K x 16 (32K bits)	4K x 32 (128K bits)
Density (Kbits/mm^2)	51	58	62
Frequency (MHz)	305	242	169
Dynamic Power (mW/MHz)	0.17	0.36	0.73

Compiled High-range Synchronous RAM Megacells

The Atmel High-range Synchronous RAM compiler has bidirectional or separate I/O ports, and can be configured in multi-bank form, with a maximum of four banks.

The range of permitted High-range Synchronous RAM megacell configurations is as follows:

```
Number of bits   16K, .. 2.25M bits
Number of words  2K, .. 32K
Word Size        8, .. 72 bits
```

The following table shows the range of performances for particular High-range Synchronous RAM configurations under typical conditions.

Configuration	8K x 8 (64K bits)	16K x 16 (256K bits)	32K x 32 (1M bits)
Density (Kbits/mm^2)	80	84	87
Frequency (MHz)	186	120	71
Dynamic Power (mW/MHz)	0.29	0.55	1.22

Compiled Asynchronous RAM Megacells

The Atmel Asynchronous RAM compiler has bidirectional or separate I/O ports, and can be configured in multi-bank form, with a maximum of four banks.

The range of permitted Asynchronous RAM megacell configurations is as follows:

```
Number of bits   128, .. 128K bits
Number of words  16, .. 4K
Word Size        8, .. 36 bits
```

The following table shows the range of performances for particular Asynchronous RAM configurations under typical conditions.

Configuration	1K x 8 (8K bits)	2K x 16 (32K bits)	4K x 32 (128K bits)
Density (Kbits/mm^2)	40	40	50
Frequency (MHz)	380	378	293
Dynamic Power (mW/MHz)	0.24	0.38	0.63

Compiled Asynchronous Dual-port RAM Megacells

The Atmel Asynchronous Dual-port RAM has bidirectional or separate I/O ports, and can be configured in multi-bank form, with a maximum of four banks.

The range of permitted Asynchronous Dual-port RAM Megacell configurations is as follows:

```
Number of bits     128, .. 16K
Number of words(1) 64, .. 2K
Word Size(1)       2, .. 36 bits
```

Note: 1. Must be the same for both ports.

The following table shows the range of performances for particular Asynchronous Dual-port RAM configurations under typical conditions.

Configuration	128 x 8 (1K bits)	256 x 16 (4K bits)	512 x 32 (16K bits)
Density (Kbits/mm^2)	22	32	36
Frequency (MHz)	305	274	248
Dynamic Power (mW/MHz)	0.09	0.31	0.41

Compiled Two-port RAM Megacells

The Atmel Asynchronous Two-port RAM can be configured in multi-bank form, with a maximum of four banks, and can be used to achieve FIFO functions.

The range of permitted Asynchronous Two-port RAM Megacell configurations is as follows:

```
Number of bits      128, .. 36K
Number of words(1)  64, .. 2K
Word Size(1)        2, .. 36 bits
```

Note: 1. Must be the same for both ports.

The following table shows the range of performances for particular Asynchronous Two-port RAM configurations under typical conditions.

Configuration	256 x 8 (2K bits)	512 x 16 (8K bits)	1K x 32 (32K bits)
Density (Kbits/mm^2)	20	24	27
Frequency (MHz)	385	357	294
Dynamic Power (mW/MHz)	0.06	0.10	0.18

Compiled Synchronous ROM Megacells

The Atmel Synchronous ROM is diffusion programmable and is applicable in low power solutions. It can be configured in multi-bank form, with a maximum of four banks.

The range of permitted Synchronous ROM Megacell configurations is as follows:

```
Number of bits          256, .. 512K
Number of words         64, .. 8K
Word Size               4, .. 72 bits
```

The following table shows the range of performances for particular Synchronous ROM configurations under typical conditions.

Configuration	2K x 8 (16K bits)	4K x 16 (64K bits)	8K x 32 (256K bits)
Density (Kbits/mm^2)	400	568	669
Frequency (MHz)	198	187	140
Dynamic Power (mW/MHz)	0.13	0.26	0.54

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