CY62167E MoBL®

16-Mbit (1M x 16 / 2M x 8) Static RAM

Features

- Configurable as 1M x 16 or as 2M x 8 SRAM
- Very high speed: 45 ns
- Wide voltage range: 4.5V–5.5V
- Ultra low standby power
  - Typical standby current: 1.5 µA
  - Maximum standby current: 12 µA
- Ultra low active power
  - Typical active current: 2.2 mA @ f = 1 MHz
- Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Offered in 48-pin TSOP I package

Functional Description[1]

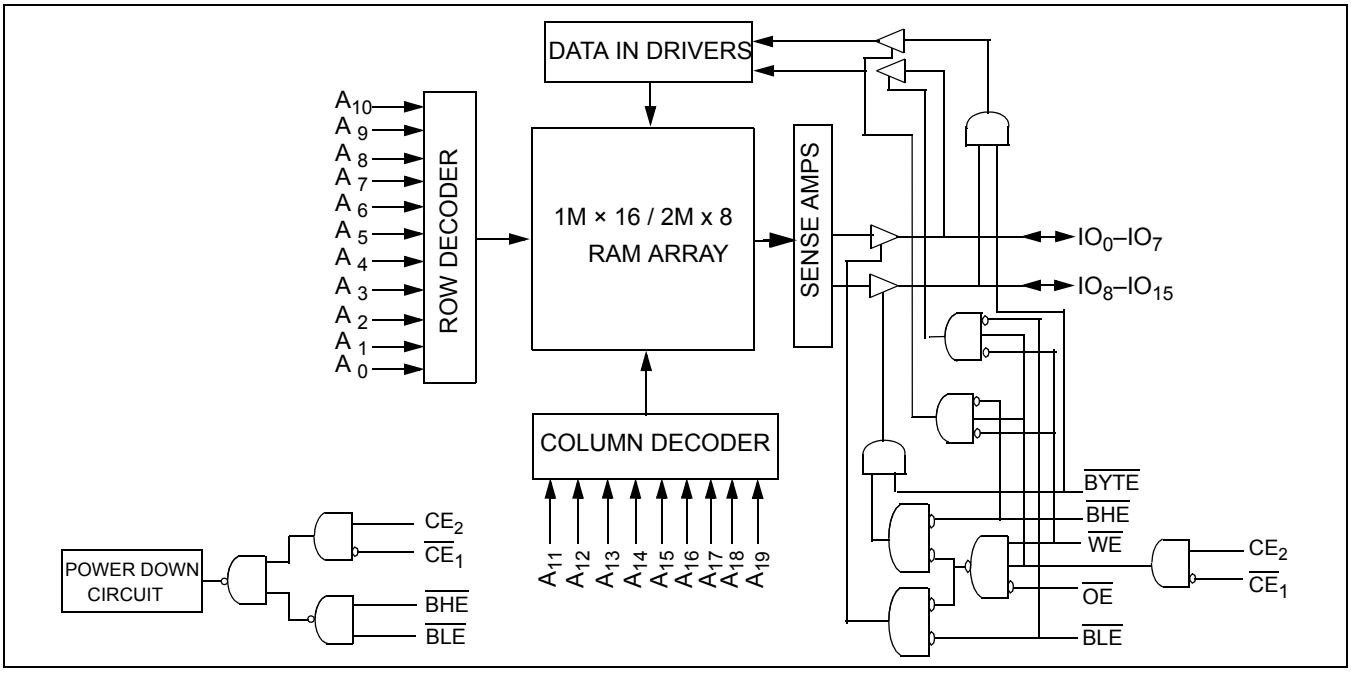
The CY62167E is a high performance CMOS static RAM organized as 1M words by 16 bits/2M words by 8 bits. This device features advanced circuit design to provide an ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that reduces power consumption by 99% when addresses are not toggling. Place the device into standby mode when deselected ($\overline{CE}_1$ HIGH, or CE_2 LOW, or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input and output pins (IO_0 through IO_{15}) are placed in a high impedance state when:

- The device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW)
- Outputs are disabled ($\overline{OE}$ HIGH)
- Both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH) or
- A write operation is in progress ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW)

To write to the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from IO pins (IO_0 through IO_7), is written into the location specified on the address pins (A_0 through A_{19}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from the IO pins (IO_8 through IO_{15}) is written into the location specified on the address pins (A_0 through A_{19}).

To read from the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appears on IO_0 to IO_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on IO_8 to IO_{15}. See the "Truth Table" on page 10 for a complete description of read and write modes.

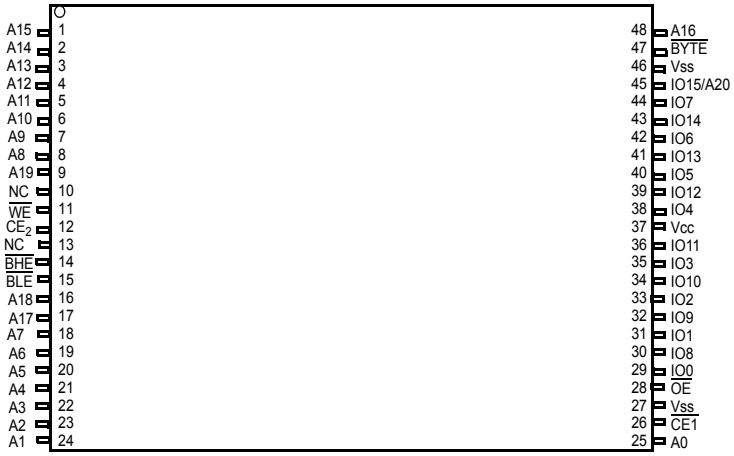
Logic Block Diagram



Note
1. For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.

Pin Configuration[2, 3]

48-Pin TSOP I Top View



Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC} (mA)				Standby I_{SB2} (μA)	
					f = 1 MHz		f = f_{max}			
	Min	Typ[4]	Max		Typ[4]	Max	Typ[4]	Max	Typ[4]	Max
CY62167ELL	4.5	5.0	5.5	45	2.2	4.0	25	30	1.5	12

Notes
2. NC pins are not connected on the die.
3. The BYTE pin in the 48-TSOPI package must be tied to V_{CC} to use the device as a 1M X 16 SRAM. The 48-TSOPI package can also be used as a 2M X 8 SRAM by tying the BYTE signal to V_{SS}. In the 2M x 8 configuration, pin 45 is A20, while BHE, BLE and IO_8 to IO_{14} pins are not used.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC}(typ), T_A = 25°C.

Maximum Ratings

Exceeding the maximum ratings may shorten the battery life of the device. User guidelines are not tested.

Storage Temperature ..... –65°C to + 150°C

Ambient Temperature with Power Applied ..... –55°C to + 125°C

Supply Voltage to Ground Potential ..... –0.5V to 6.0V

DC Voltage Applied to Outputs in High-Z State[5, 6] ..... –0.5V to 6.0V

DC Input Voltage[5, 6] ..... –0.5V to 6.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (MIL-STD-883, Method 3015)

Latch Up Current ..... >200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[7]
CY62167ELL	Industrial	–40°C to +85°C	4.5V to 5.5V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		45 ns			Unit
				Min	Typ[4]	Max	
V_{OH}	Output HIGH Voltage	I_{OH} = –1.0 mA		2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1mA				0.4	V
V_{IH}	Input HIGH Voltage	V_{CC} = 4.5V to 5.5V		2.2		V_{CC} + 0.5V	V
V_{IL}	Input LOW Voltage	V_{CC} = 4.5V to 5.5V		–0.5		0.7[8]	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	f = f_{MAX} = $1/t_{RC}$	V_{CC} = V_{CC}(max) I_{OUT} = 0 mA CMOS levels		25	30	mA
		f = 1 MHz			2.2	4.0	mA
I_{SB2}[9]	Automatic CE Power Down Current—CMOS Inputs	$\overline{CE}_1$ ≥ V_{CC} – 0.2V or CE_2 ≤ 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0, V_{CC} = $V_{CC(max)}$			1.5	12	µA

Capacitance[10]

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output Capacitance		10	pF

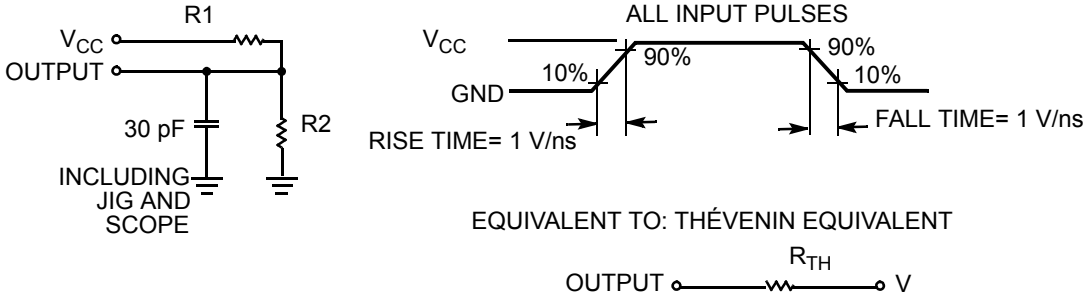
Thermal Resistance[10]

Parameter	Description	Test Conditions	TSOP I	Unit
Θ_{JA}	Thermal Resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	60	°C/W
Θ_{JC}	Thermal Resistance (junction to case)		4.3	°C/W

Notes

5. V_{IL}(min) = –2.0V for pulse durations less than 20 ns.
6. V_{IH}(max) = V_{CC} + 0.75V for pulse durations less than 20 ns.
7. Full Device AC operation is based on a 100 µs ramp time from 0 to V_{CC} (min) and 200 µs wait time after V_{CC} stabilization.
8. Under DC conditions the device meets a V_{IL} of 0.8V. However, in dynamic conditions Input LOW Voltage applied to the device must not be higher than 0.7V.
9. Only chip enables ($\overline{CE}_1$ and CE_2), byte enables ($\overline{BHE}$ and $\overline{BLE}$) and $\overline{BYTE}$ need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
10. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



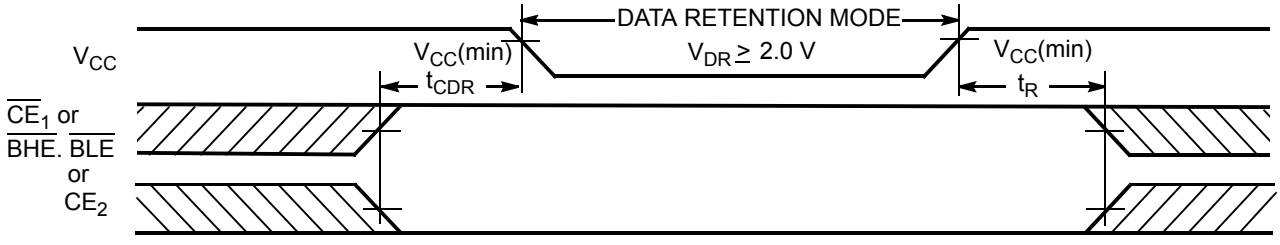
Parameters	Values	Unit
R1	1800	Ω
R2	990	Ω
R_{TH}	639	Ω
V_{TH}	1.77	V

Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ[4]	Max	Unit
V_{DR}	V_{CC} for Data Retention		2.0			V
I_{CCDR}[9]	Data Retention Current	V_{CC}= V_{DR} $\overline{CE_1} \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$			12	µA
t_{CDR}[10]	Chip Deselect to Data Retention Time		0			ns
t_R[11]	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform[12]



Notes

11. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC}(min) ≥ 100 µs or stable at V_{CC}(min) ≥ 100 µs.
12. $\overline{BHE}$. $\overline{BLE}$ is the AND of $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling the chip enable signals or by disabling $\overline{BHE}$ and $\overline{BLE}$.

Switching Characteristics

Over the Operating Range[13, 14]

Parameter	Description	45 ns		Unit
		Min	Max	
READ CYCLE				
t_{RC}	Read Cycle Time	45		ns
t_{AA}	Address to Data Valid		45	ns
t_{OHA}	Data Hold from Address Change	10		ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Data Valid		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		22	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW-Z[15]	5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[15, 16]		18	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low-Z[15]	10		ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to High-Z[15, 16]		18	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to Power Up	0		ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to Power Down		45	ns
t_{DBE}	BLE/BHE LOW to Data Valid		45	ns
t_{LZBE}	$\overline{BLE}/\overline{BHE}$ LOW to Low-Z[15]	10		ns
t_{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to HIGH-Z[15, 16]		18	ns
WRITE CYCLE[17]				
t_{WC}	Write Cycle Time	45		ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Write End	35		ns
t_{AW}	Address Setup to Write End	35		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Setup to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	35		ns
t_{BW}	$\overline{BLE}/\overline{BHE}$ LOW to Write End	35		ns
t_{SD}	Data Setup to Write End	25		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[15, 16]		18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[15]	10		ns

Notes

13. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 V/ns, timing reference levels of V_{CC}(typ)/2, input pulse levels of 0 to V_{CC}(typ), and output loading of the specified I_{OL}/I_{OH} as shown in "AC Test Loads and Waveforms" on page 4.
14. AC timing parameters are subject to byte enable signals ($\overline{BHE}$ or $\overline{BLE}$) not switching when chip is disabled. See application note AN13842 for further clarification.
15. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
16. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
17. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 1 shows address transition controlled read cycle waveforms.[18, 19]

Figure 1. Read Cycle No. 1

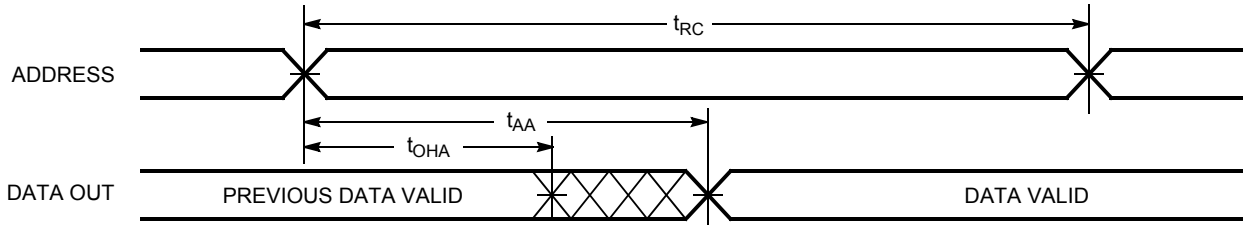
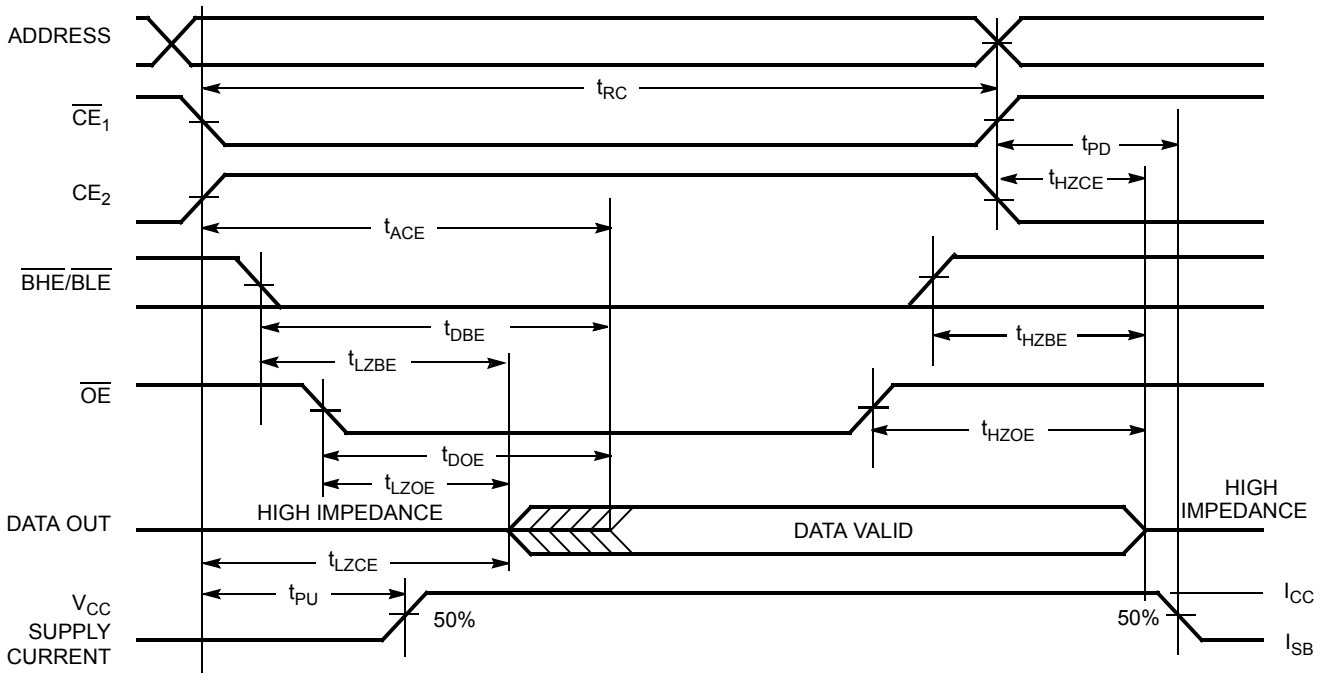


Figure 2 shows $\overline{OE}$ controlled read cycle waveforms.[19, 20]

Figure 2. Read Cycle No. 2

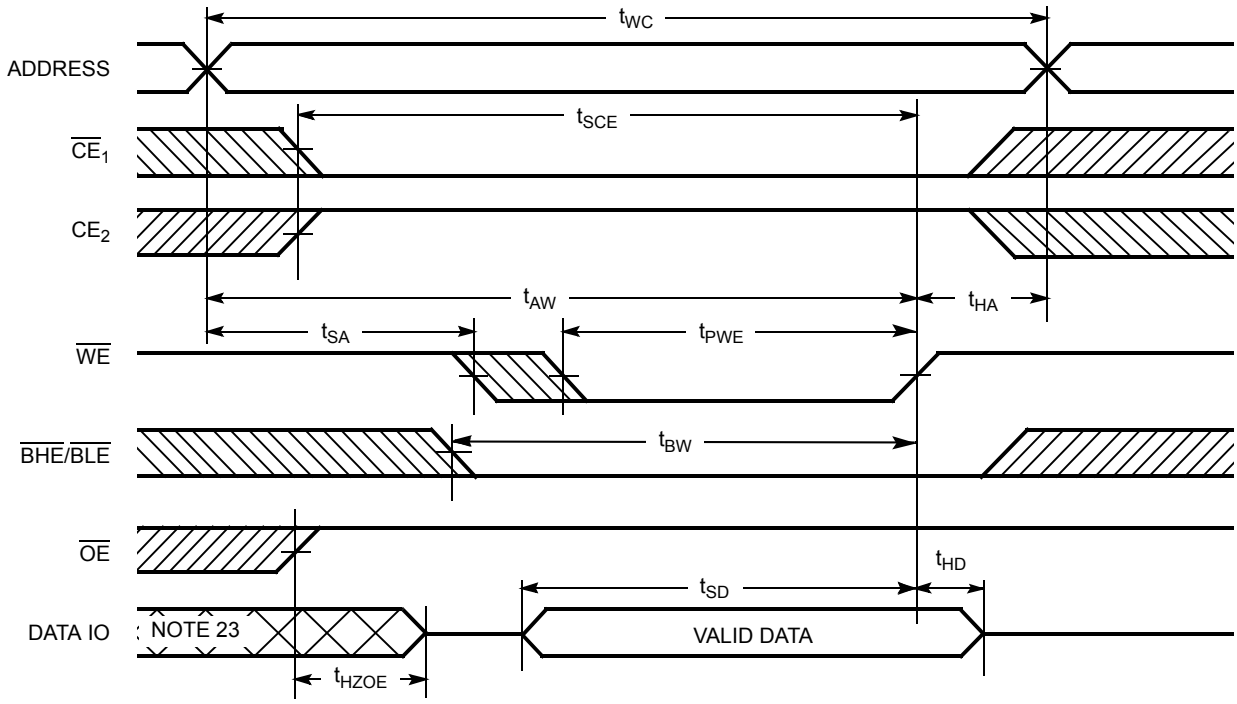


Notes
18. The device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}.
19. $\overline{WE}$ is HIGH for read cycle.
20. Address valid before or similar to $\overline{CE_1}$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 3 shows $\overline{WE}$ controlled write cycle waveforms.[17, 21, 22]

Figure 3. Write Cycle No. 1



Notes
21. Data IO is high impedance if $\overline{OE}$ = V_{IH}.
22. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
23. During this period the IOs are in output state and input signals must not be applied.

Switching Waveforms (continued)

Figure 4 shows $\overline{CE}_1$ or CE_2 controlled write cycle waveforms.[17, 21, 22]

Figure 4. Write Cycle No. 2

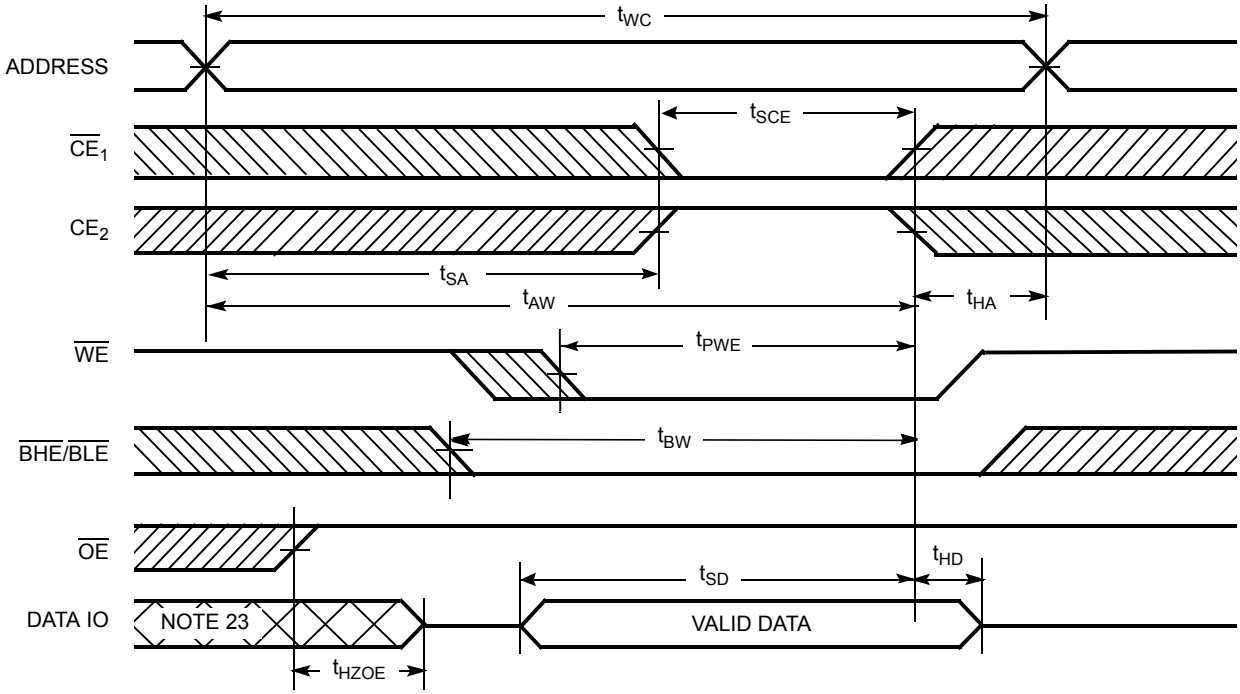
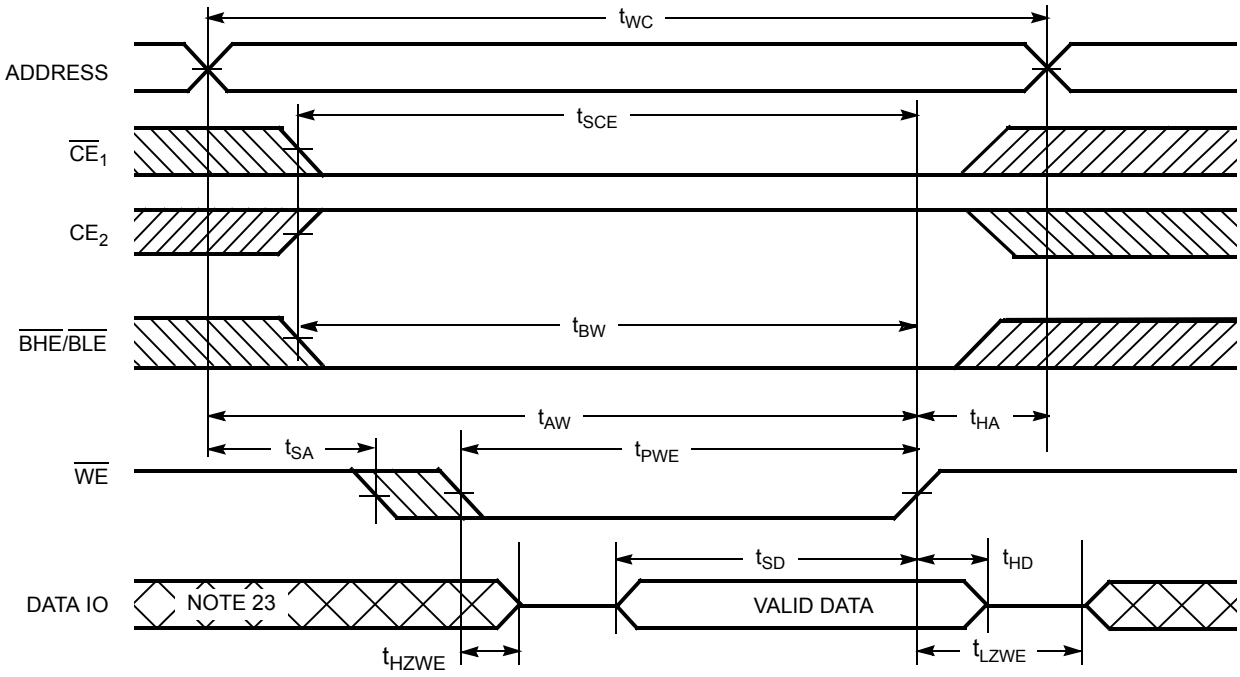


Figure 5 shows $\overline{WE}$ controlled, $\overline{OE}$ LOW write cycle waveforms.[22]

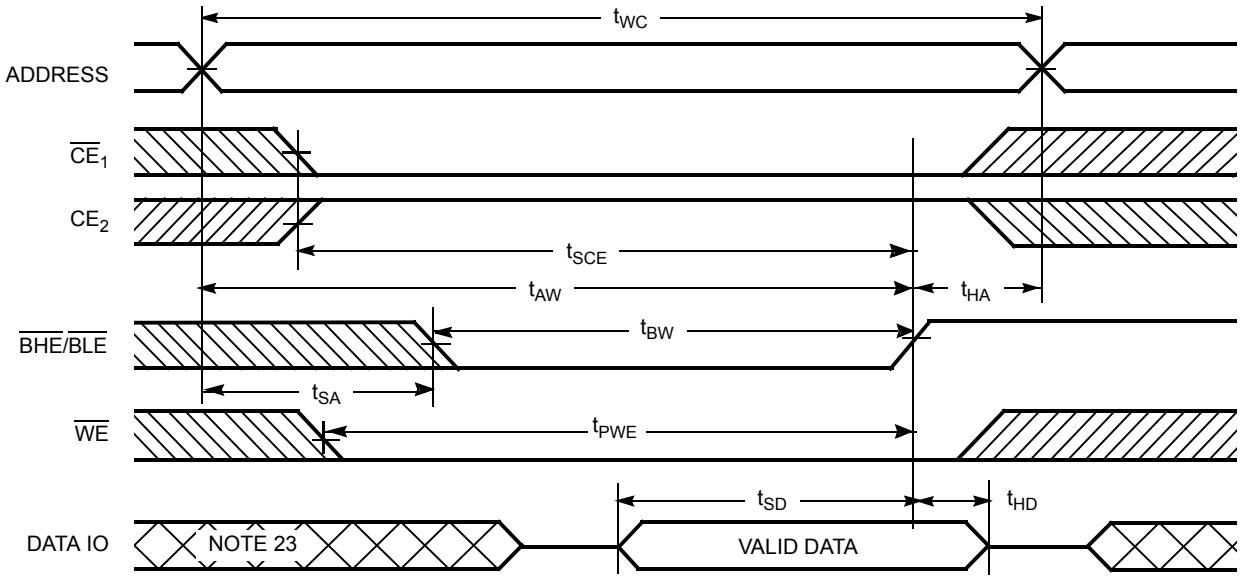
Figure 5. Write Cycle No. 3



Switching Waveforms (continued)

Figure 6 shows $\overline{BHE}/\overline{BLE}$ controlled, $\overline{OE}$ LOW write cycle waveforms.[22]

Figure 6. Write Cycle No. 4



Truth Table

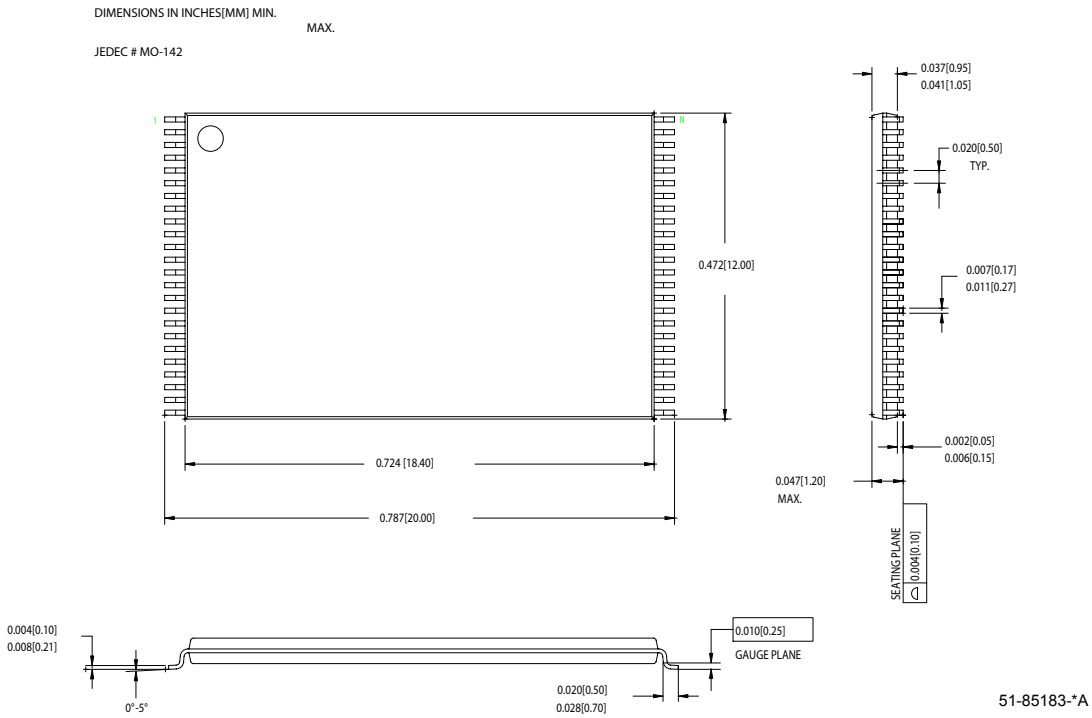
$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs Outputs	Mode	Power
H	X	X	X	X	X	High-Z	Deselect/Power Down	Standby (I_{SB})
X	L	X	X	X	X	High-Z	Deselect/Power Down	Standby (I_{SB})
X	X	X	X	H	H	High-Z	Deselect/Power Down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (IO_0–IO_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	Data Out (IO_0–IO_7); High-Z (IO_8–IO_{15})	Read	Active (I_{CC})
L	H	H	L	L	H	High-Z (IO_0–IO_7); Data Out (IO_8–IO_{15})	Read	Active (I_{CC})
L	H	H	H	L	H	High-Z	Output Disabled	Active (I_{CC})
L	H	H	H	H	L	High-Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	L	High-Z	Output Disabled	Active (I_{CC})
L	H	L	X	L	L	Data In (IO_0–IO_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	Data In (IO_0–IO_7); High-Z (IO_8–IO_{15})	Write	Active (I_{CC})
L	H	L	X	L	H	High-Z (IO_0–IO_7); Data In (IO_8–IO_{15})	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62167ELL-45ZXI	51-85183	48-pin TSOP I (Pb-free)	Industrial

Package Diagram

Figure 7. 48-Pin TSOP I (12 mm x 18.4 mm x 1.0 mm), 51-85183



Document History Page

Document Title: CY62167E MoBL® 16-Mbit (1M x 16 / 2M x 8) Static RAM Document Number: 001-15607				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	1103145	See ECN	VKN	New Data Sheet
*A	1138903	See ECN	VKN	Converted from preliminary to final Changed $I_{CC(max)}$ spec from 2.8 mA to 4.0 mA for f=1MHz Changed $I_{CC(typ)}$ spec from 22 mA to 25 mA for f=f_{max} Changed $I_{CC(max)}$ spec from 25 mA to 30 mA for f=f_{max} Added footnote# 8 related to V_{IL} Changed I_{CCDR} spec from 10 µA to 12 µA Added footnote# 14 related to AC timing parameters