HM5116400L Series Low Power Version

Product Preview

4,194,304-Word x 4-Bit Dynamic Random Access Memory

T-46-23-18

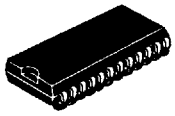
■ DESCRIPTION

The Hitachi HM5116400 is a CMOS dynamic RAM organized 4,194,304 words x 4 bits. It employs the most advanced CMOS technology for high performance and low power. The HM5116400 offers Fast Page Mode as a high speed access mode.

■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time .....60 ns/70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode .....495 mW/440 mW/385 mW/330 mW (max)
  - Standby Mode .....11 mW (max)
- Fast Page Mode Capability
- Long Refresh Period
  - 4,096 Refresh Cycles .....(256 ms)
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- Battery Back Up Operation

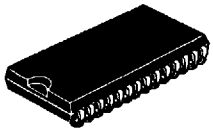
HM5116400LJ Series



3DCP24D

(CP-24D)

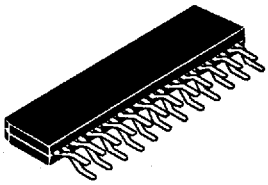
HM5116400LJ Series



3DCP28D

(CP-28D)

HM5116400LZ Series



3DZP24

(ZP-24)

■ ORDERING INFORMATION

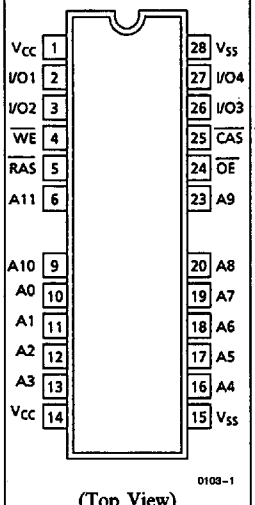
Part No.	Access Time	Package
HM5116400LJ-6	60 ns	400 mil 24-pin Plastic SOJ (CP-24D)
HM5116400LJ-7	70 ns	
HM5116400LJ-8	80 ns	
HM5116400LJ-10	100 ns	
HM5116400LZ-6	60 ns	475 mil 24-pin Plastic ZIP (ZP-24)
HM5116400LZ-7	70 ns	
HM5116400LZ-8	80 ns	
HM5116400LZ-10	100 ns	

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{11}	Address Input
A_0–A_{11}	Refresh Address Input
I/O_0–I/O_4	Data-input/Data-output
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply (+ 5V)
V_{SS}	Ground
NC	No Connection

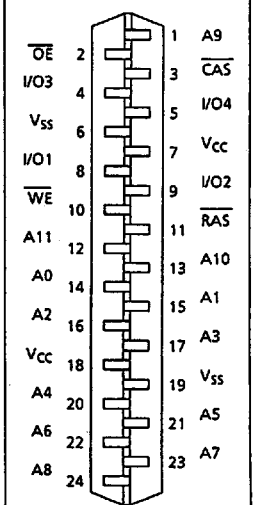
■ PIN OUT

HM5116400LJ Series



(Top View)

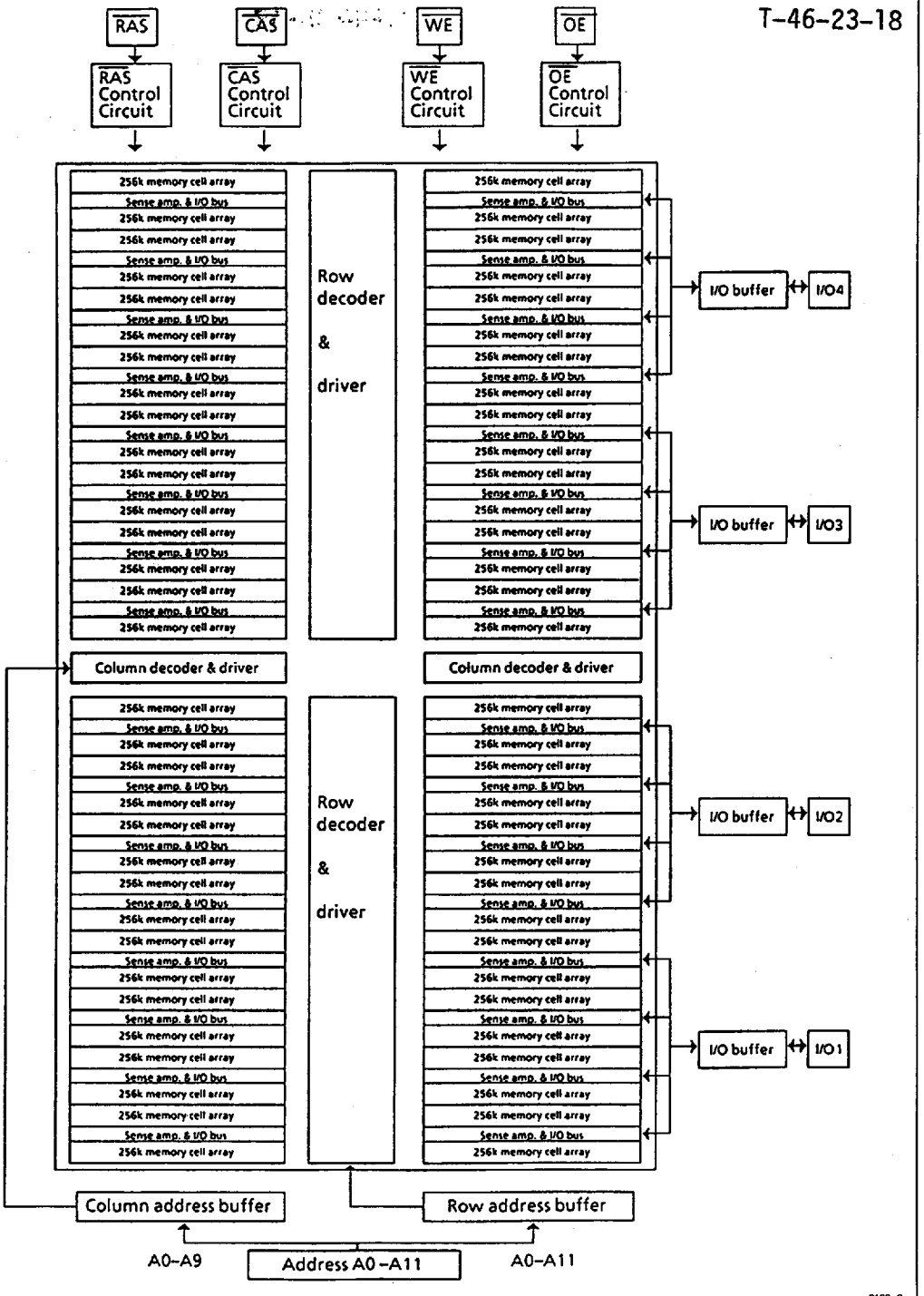
HM5116400LZ Series



(Bottom View)

■ BLOCK DIAGRAM

T-46-23-18



T-46-23-18

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

HITACHI/ LOGIC/ARRAYS/MEM

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM5116400-6		HM5116400-7		HM5116400-8		HM5116400-10		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	90	—	80	—	70	—	60	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High-Z	
		—	300	—	300	—	300	—	300	μA	CMOS Interface, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ > V_{CC} − 0.2V or ≤ 6.5V Address and D_{in} = stable D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	90	—	80	—	70	—	60	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	5	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{out} = Enable	1, 4
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	90	—	80	—	70	—	60	mA	t_{RC} = Min	4
Fast Page Mode Current	I_{CC7}	—	70	—	60	—	50	—	45	mA	t_{PC} = Min	1, 3
Battery Back Up Operating Current (Standby with CBR Refresh)	I_{CC10}	—	500	—	500	—	500	—	500	μA	Standby: CMOS Interface CBR Refresh: t_{RC} = 62.5 μs t_{RAS} ≤ 1 μs Address and D_{in} = Stable D_{out} = High-Z	5
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	−10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	−10	10	μA	0V ≤ V_{out} ≤ 7V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = −5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. Clock voltages ($\overline{RAS}$ and $\overline{CAS}$) must be applied simultaneously with or prior to applying supply voltage.
5. V_{CC} − 0.2V ≤ V_{IH} ≤ 6.5V, 0V ≤ V_{IL} ≤ 0.2V.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-in, Data-out)	C_O	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 2, 3, 19, 20]

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM5116400-6		HM5116400-7		HM5116400-8		HM5116400-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	110	—	130	—	150	—	180	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	60	—	70	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10000	18	10000	20	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	10	—	10	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	52	20	60	20	75	ns	4
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	15	40	15	55	ns	5
$\overline{RAS}$ Hold Time	t_{RSH}	15	—	18	—	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	5	—	5	—	5	—	ns	
$\overline{OE}$ to D_{in} Delay Time	t_{OED}	15	—	18	—	20	—	25	—	ns	6
$\overline{OE}$ Delay Time from D_{in}	t_{DZO}	0	—	0	—	0	—	0	—	ns	7
$\overline{CAS}$ Delay Time from D_{in}	t_{DZC}	0	—	0	—	0	—	0	—	ns	7
Transition Time (Rise and Fall)	t_T	3	30	3	30	3	30	3	30	ns	8

Read Cycle

Parameter	Symbol	HM5116400-6		HM5116400-7		HM5116400-8		HM5116400-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	9, 10, 21
Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	18	—	20	—	25	ns	10, 11, 21
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	ns	10, 12, 21
Access Time from $\overline{OE}$	t_{OEA}	—	15	—	18	—	20	—	25	ns	10, 21
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	ns	13
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	5	—	5	—	5	—	5	—	ns	13
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	45	—	ns	
Column Address to $\overline{CAS}$ Lead Time	t_{CAL}	30	—	35	—	40	—	45	—	ns	
$\overline{CAS}$ to Output in Low-Z	t_{CLZ}	0	—	0	—	0	—	0	—	ns	
Output Data Hold Time	t_{OH}	3	—	3	—	3	—	3	—	ns	
Output Data Hold Time from $\overline{OE}$	t_{OH0}	3	—	3	—	3	—	3	—	ns	
Output Buffer Turn-off Time	t_{OFF}	—	15	0	18	—	20	—	25	ns	14
Output Buffer Turn-off to $\overline{OE}$	t_{OEZ}	—	15	—	18	—	20	—	25	ns	14
$\overline{CAS}$ to D_{in} Delay Time	t_{CDD}	15	—	18	—	20	—	25	—	ns	6

Write Cycle

Parameter	Symbol	HM5116400-6		HM5116400-7		HM5116400-8		HM5116400-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	ns	15
Write Command Hold Time	t_{WCH}	15	—	15	—	15	—	15	—	ns	
Write Command Pulse Width	t_{WP}	15	—	15	—	15	—	15	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15	—	18	—	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15	—	18	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	ns	16
Data-in Hold Time	t_{DH}	15	—	15	—	15	—	15	—	ns	16

Read-Modify-Write Cycle

Parameter	Symbol	HM5116400-6		HM5116400-7		HM5116400-8		HM5116400-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	150	—	176	—	200	—	245	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	80	—	93	—	105	—	135	—	ns	15
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	35	—	41	—	45	—	60	—	ns	15
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	50	—	58	—	65	—	80	—	ns	15
$\overline{OE}$ Hold Time from $\overline{WE}$	t_{OEH}	15	—	18	—	20	—	25	—	ns	

Refresh Cycle

Parameter	Symbol	HM5116400-6		HM5116400-7		HM5116400-8		HM5116400-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time (CBR Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time (CBR Refresh Cycle)	t_{CHR}	20	—	20	—	20	—	20	—	ns	
$\overline{WE}$ Setup Time (CBR Refresh Cycle)	t_{WRP}	10	—	10	—	10	—	10	—	ns	
$\overline{WE}$ Hold Time (CBR Refresh Cycle)	t_{WRH}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0	—	0	—	0	—	0	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM5116400-6		HM5116400-7		HM5116400-8		HM5116400-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	40	—	45	—	50	—	55	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASP}	—	100000	—	100000	—	100000	—	100000	ns	17
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	35	—	40	—	45	—	50	ns	18, 21
$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	t_{CPW}	55	—	63	—	70	—	85	—	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{CPRH}	35	—	40	—	45	—	50	—	ns	

Fast Page Mode Read-Modify-Write Cycle

Parameter	Symbol	HM5116400-6		HM5116400-7		HM5116400-8		HM5116400-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Read-Modify-Write Cycle Time	t_{PRWC}	80	—	91	—	100	—	110	—	ns	

Test Mode Cycle

Parameter	Symbol	HM5116400-6		HM5116400-7		HM5116400-8		HM5116400-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Test Mode $\overline{WE}$ Setup Time	t_{WTS}	10	—	10	—	10	—	10	—	ns	
Test Mode $\overline{WE}$ Hold Time	t_{WTH}	10	—	10	—	10	—	10	—	ns	

Counter Test Cycle

Parameter	Symbol	HM5116400-6		HM5116400-7		HM5116400-8		HM5116400-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	TBD	—	TBD	—	TBD	—	TBD	—	ns	

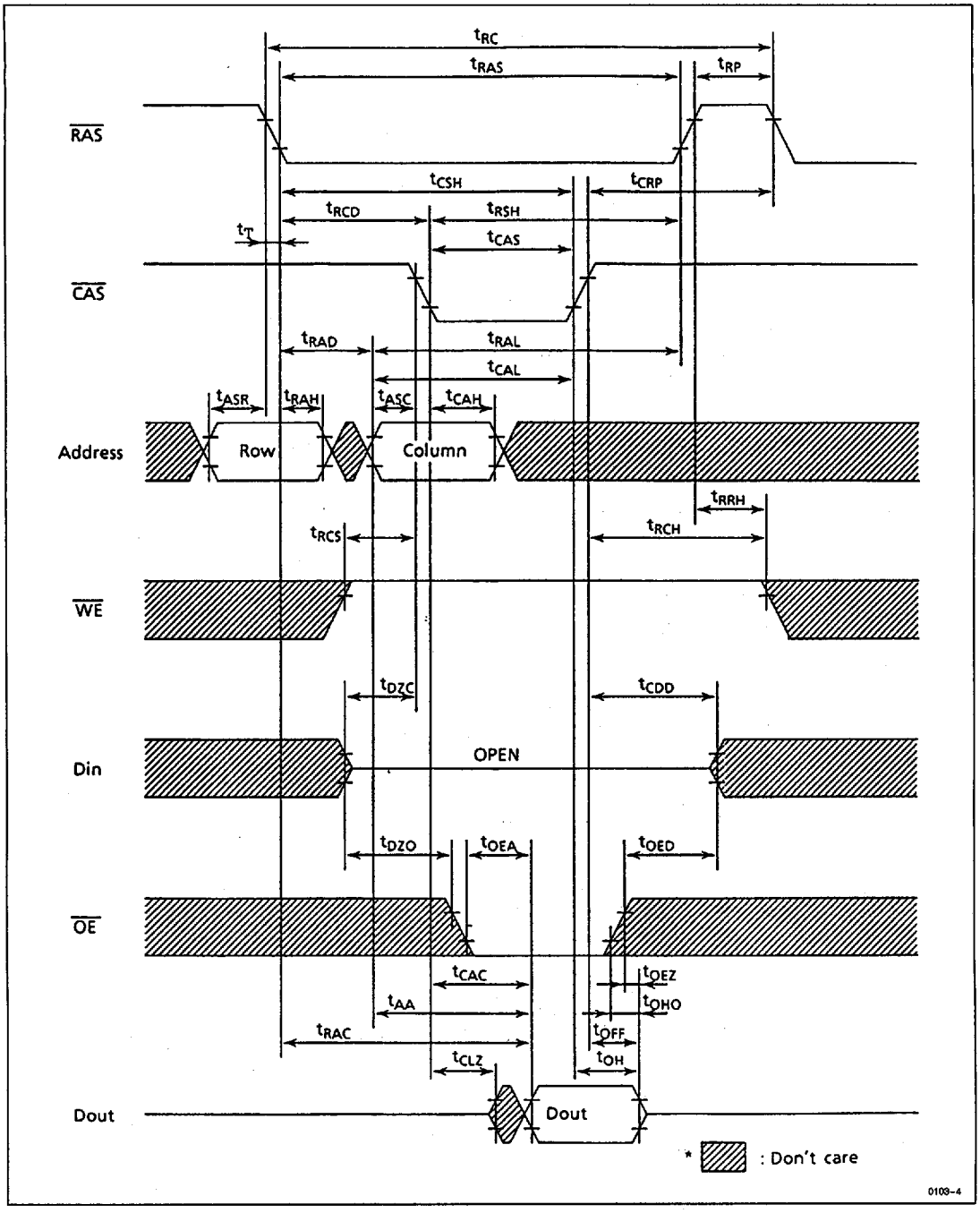
Refresh (T_J = 85°C, V_{CC} = 5V ±10%)

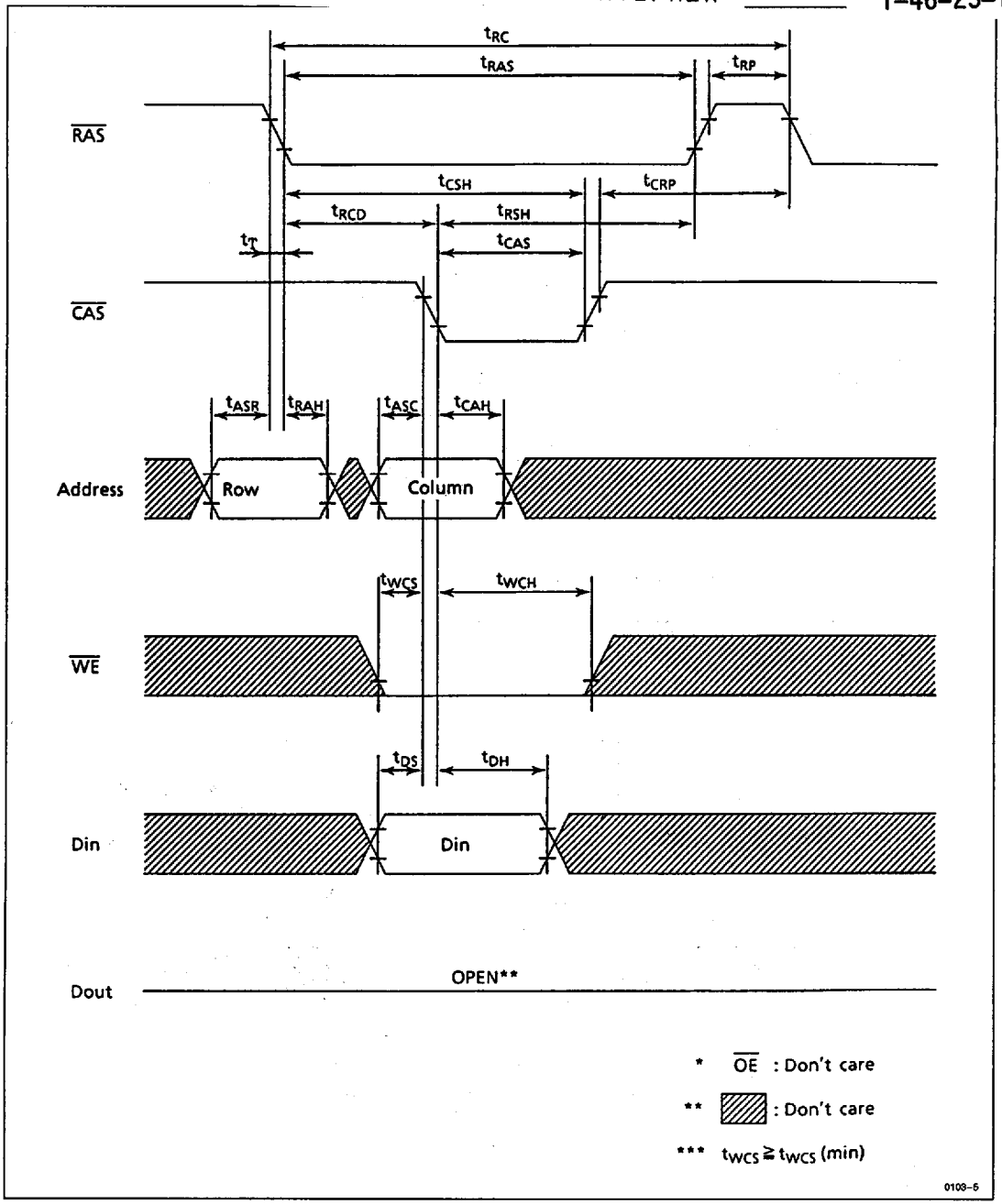
Parameter	Symbol	Max	Unit	Note
Refresh Period	t_{REF}	256	ms	4096 Cycles

Notes:
1. AC measurements assume t_T = 5 ns.
2. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required.
3. Only row address is indispensable on address A10 and A11.
4. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
5. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
6. Either t_{ODD} or T_{CDD} must be satisfied.
7. Either t_{DZO} or T_{DZC} must be satisfied.
8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
9. Assumes that $t_{RCD} < t_{RCD}$ (max) and $t_{RAD} < t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
10. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
11. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
12. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
13. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
14. t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
15. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min) the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
16. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
17. t_{RASP} defines $\overline{RAS}$ pulse width in fast page mode cycles.
18. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CPA}.
19. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
20. Test mode operation specified in this data sheet is 16 bits test function controlled by compression addresses — CA0 and CA1. This test mode operation can be performed by $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of four test bits on each I/O accord with each other, the state of the output data on the I/O is high level. When the state of four test bits on the I/O do not accord with each other, the state of the output data on the I/O is low level. Data input and output pins are I/O-1 to I/O-4. If any refresh cycle is occurred, the test mode is reset.
21. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} and t_{CPA} is delayed by 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

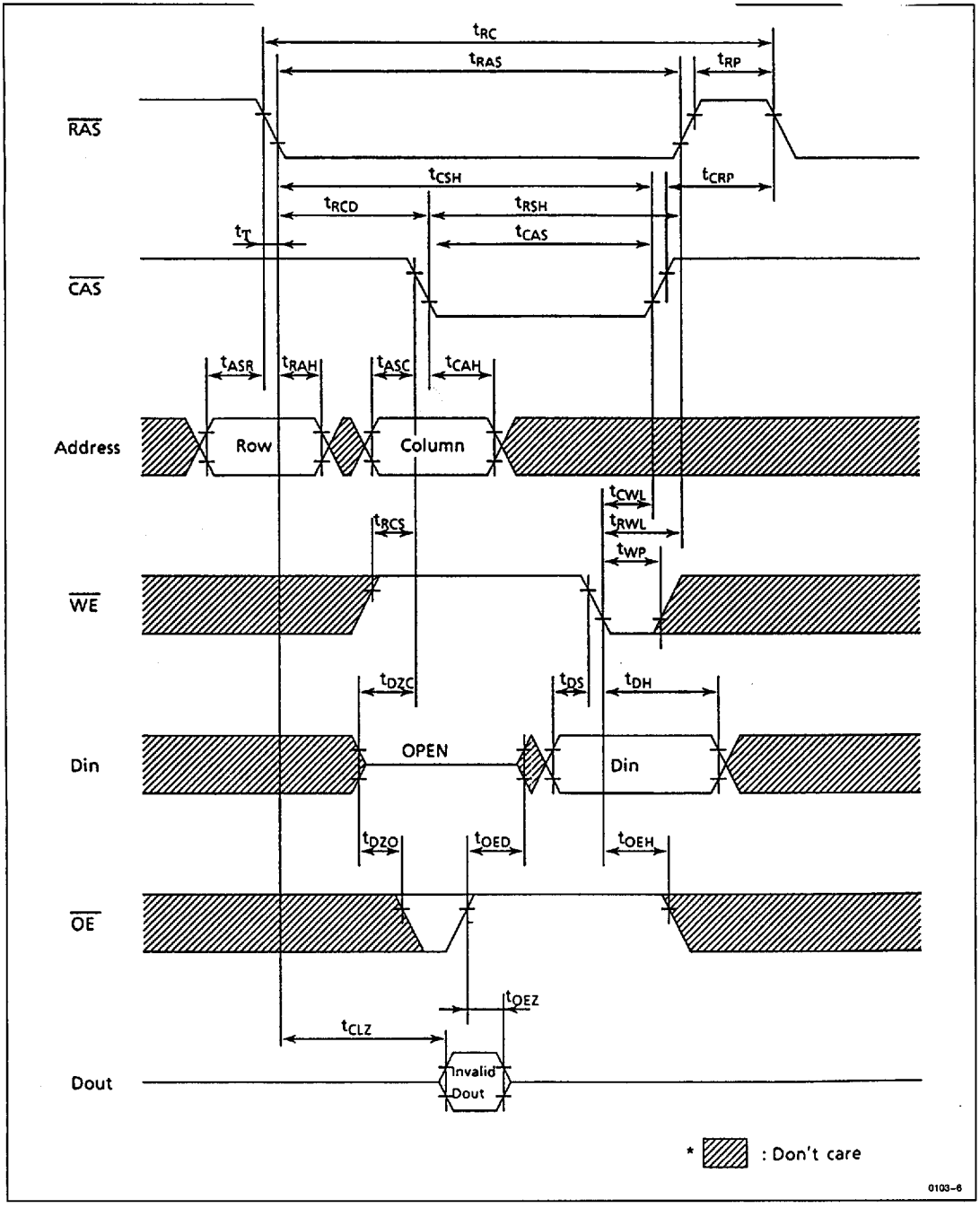
■ TIMING WAVEFORMS

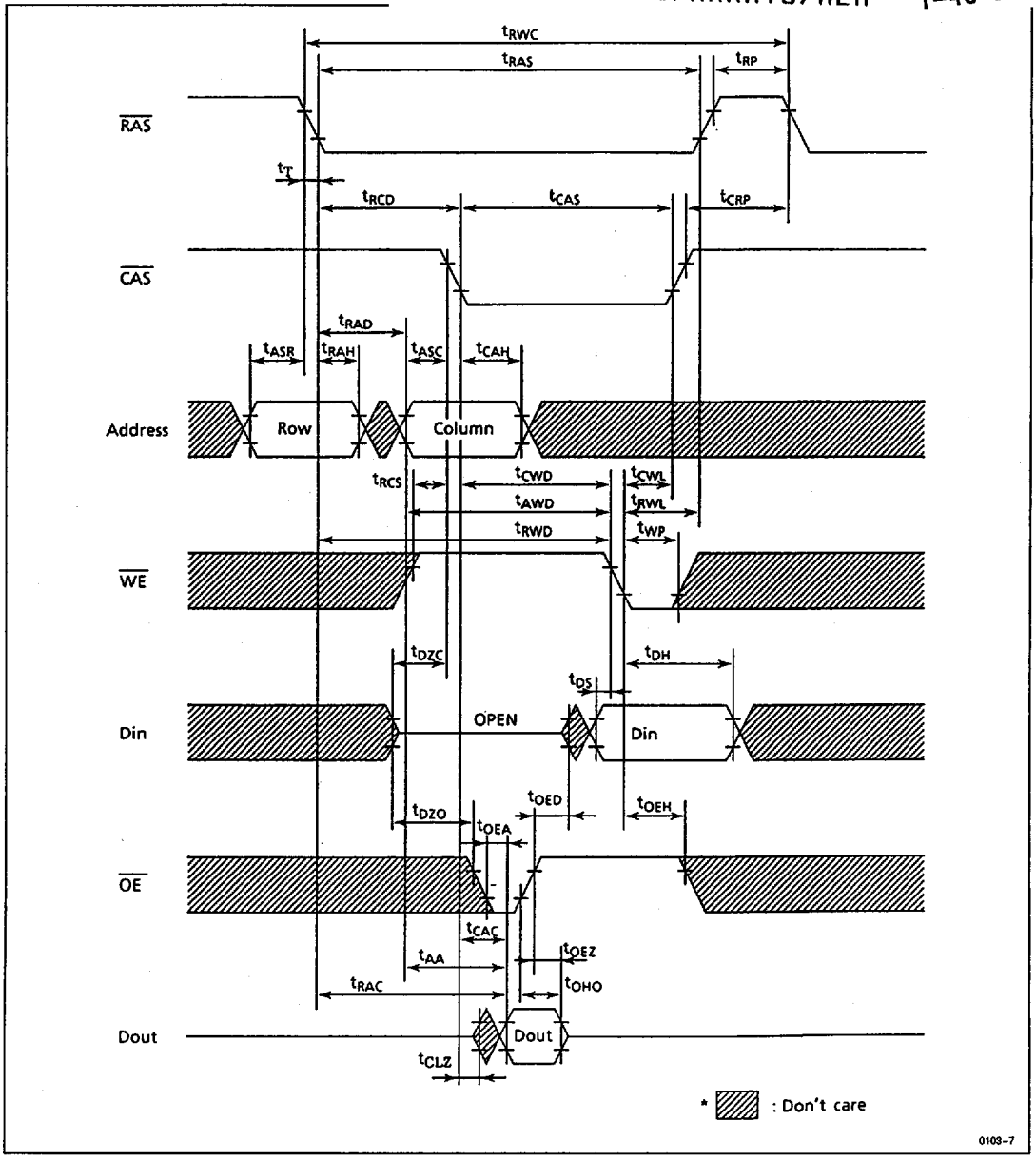
• Read Cycle



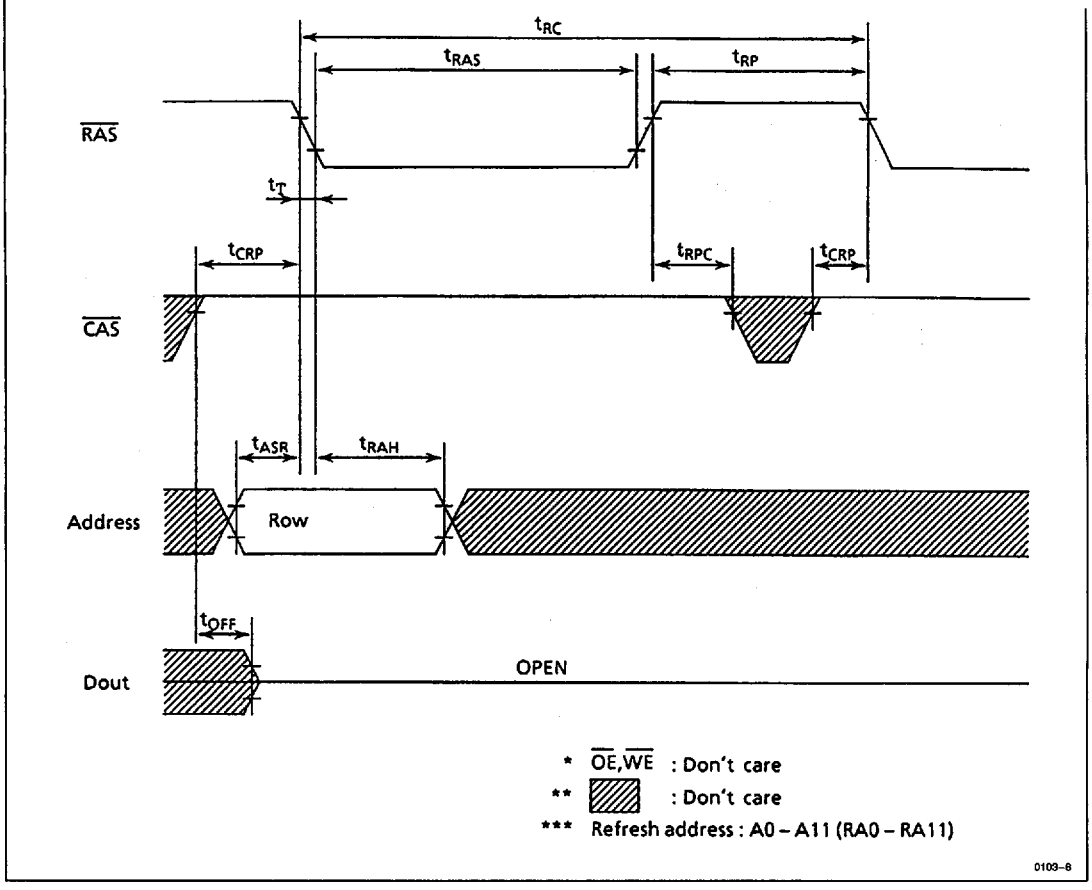

tRC
tRAS
tRP
RAS
tCSH
tCRP
tRCD
tRSH
tT
tCAS
CAS
tASR
tRAH
tASC
tCAH
Address
Row
Column
tWCS
tWCH
WE
tDS
tDH
Din
Din
Dout
OPEN**
* OE : Don't care
** : Don't care
*** tWCS ≧ tWCS (min)
0109-5

• Delayed Write Cycle




tRWC
tRAS
tRP
RAS
tT
tRCD
tCAS
tCRP
CAS
tRAD
tASR
tRAH
tASC
tCAH
Address
Row
Column
tRCS
tCWD
tCWL
tAWD
tRWL
tRWD
tWP
WE
tDZC
tDH
tDS
Din
OPEN
Din
tDZO
tOED
tOEH
tOEA
OE
tCAC
tAA
tOEZ
tRAC
tOHO
Dout
Dout
tCLZ
* : Don't care
0103-7

• $\overline{RAS}$ Only Refresh Cycle



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

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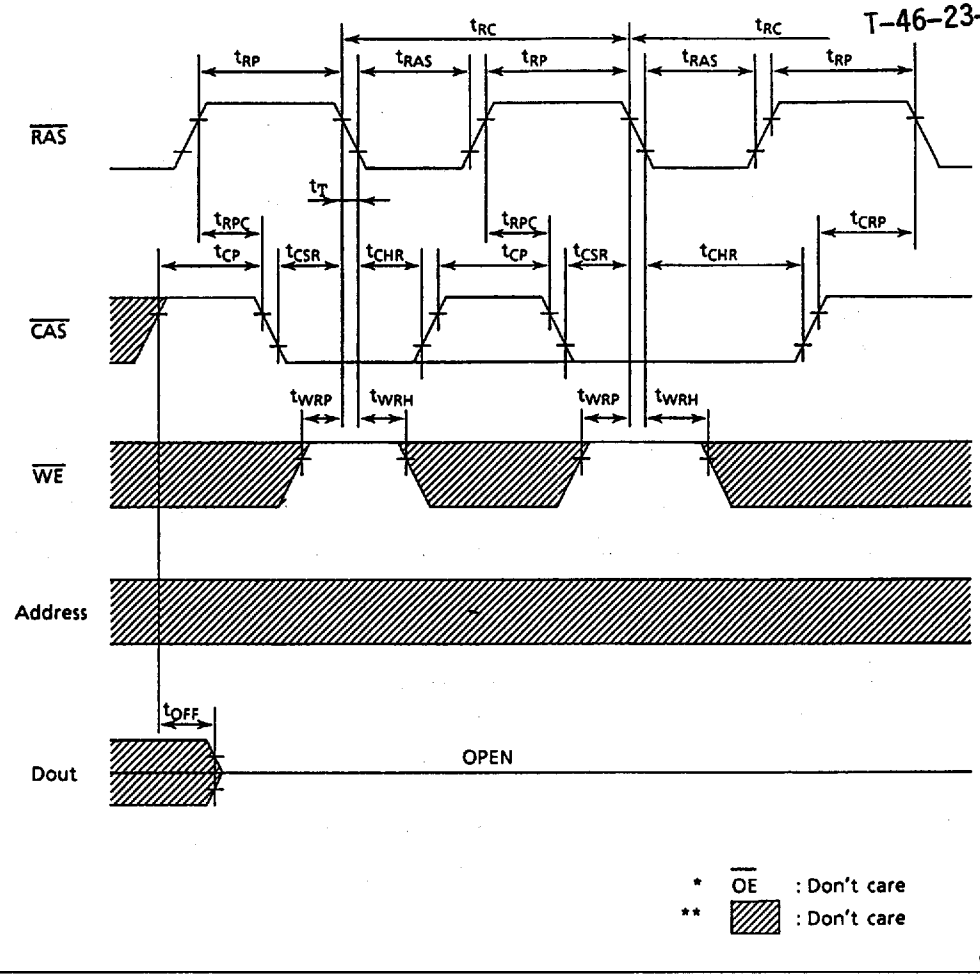
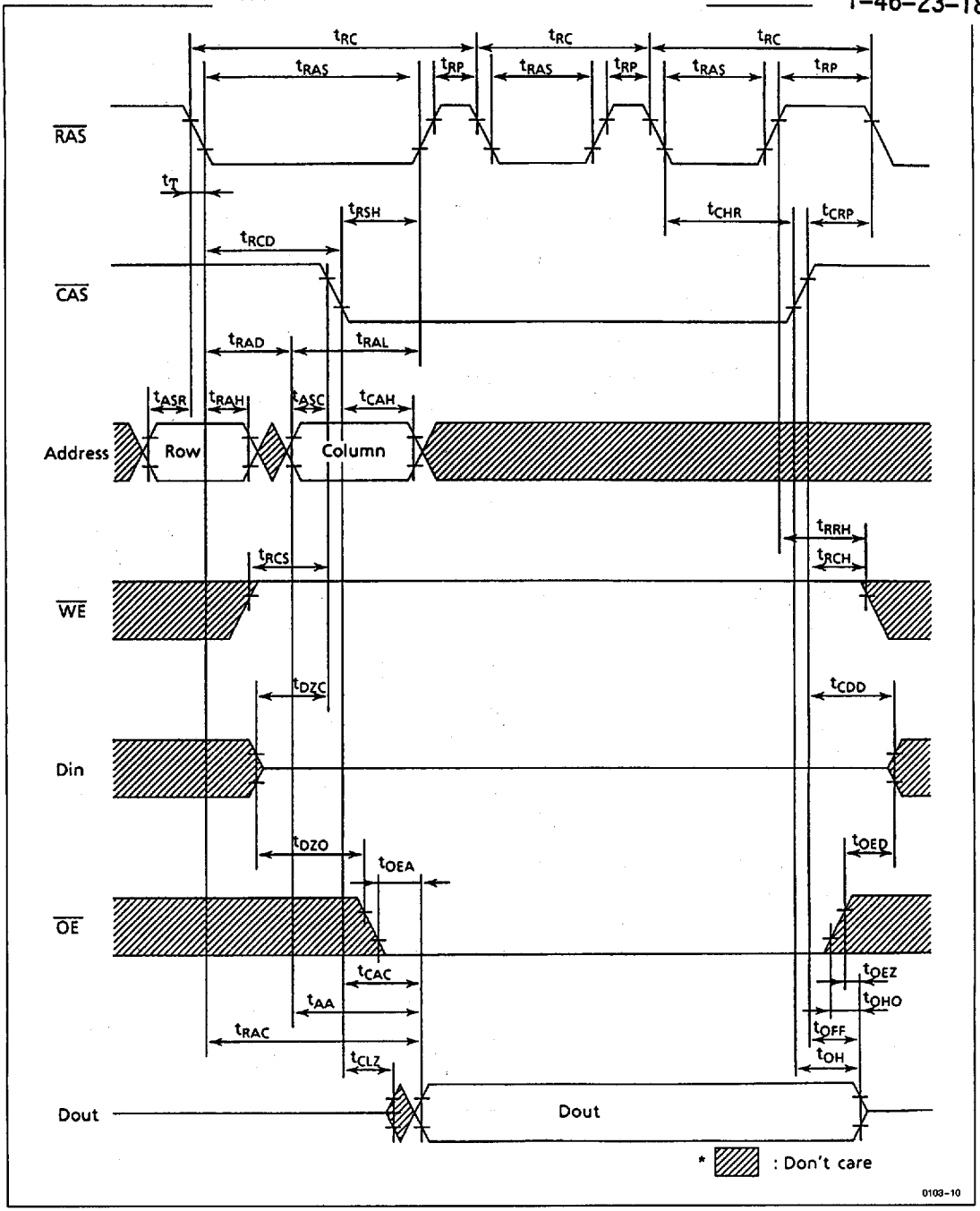
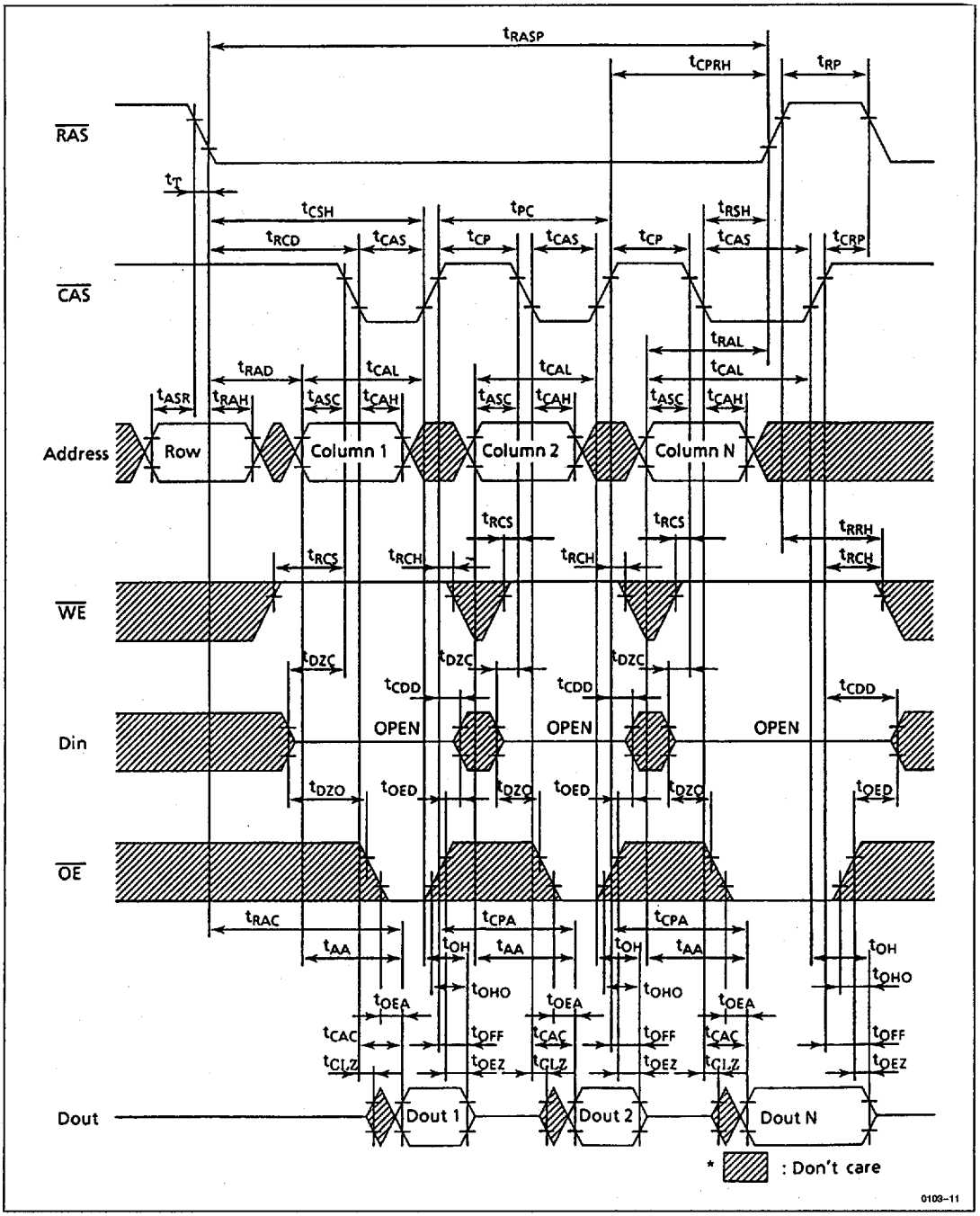


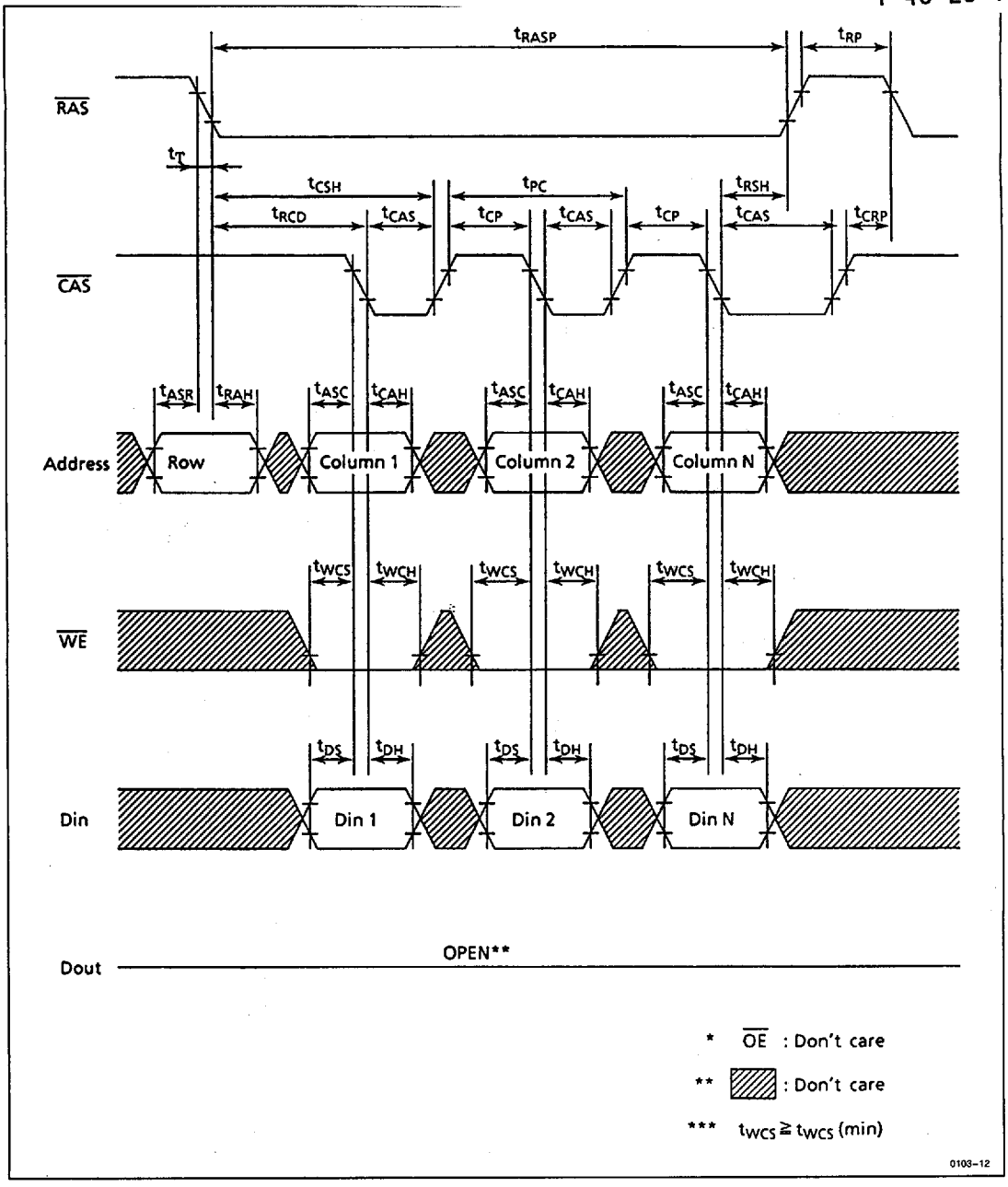
• Hidden Refresh Cycle



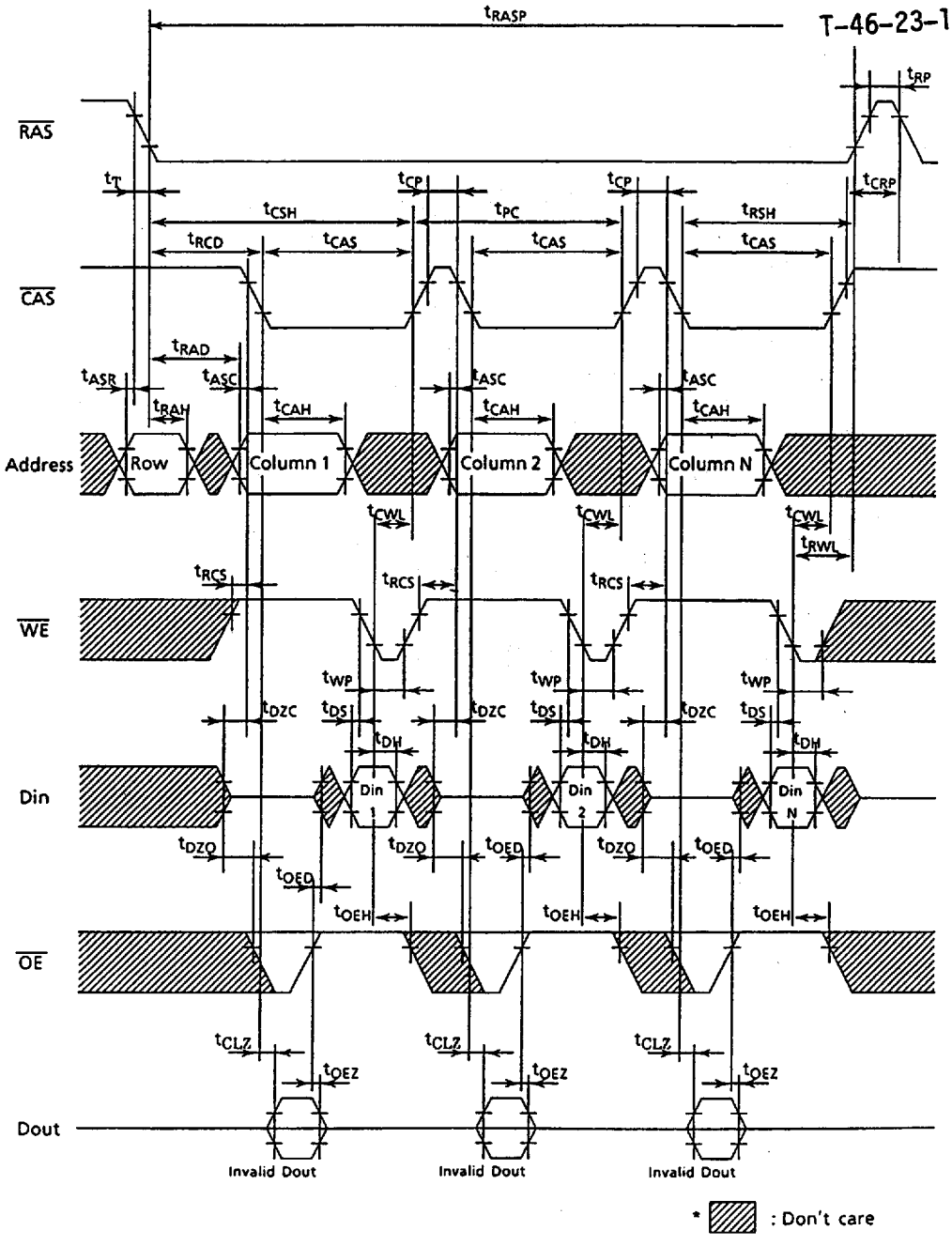
• Fast Page Mode Read Cycle



• **Fast Page Mode Early Write Cycle**

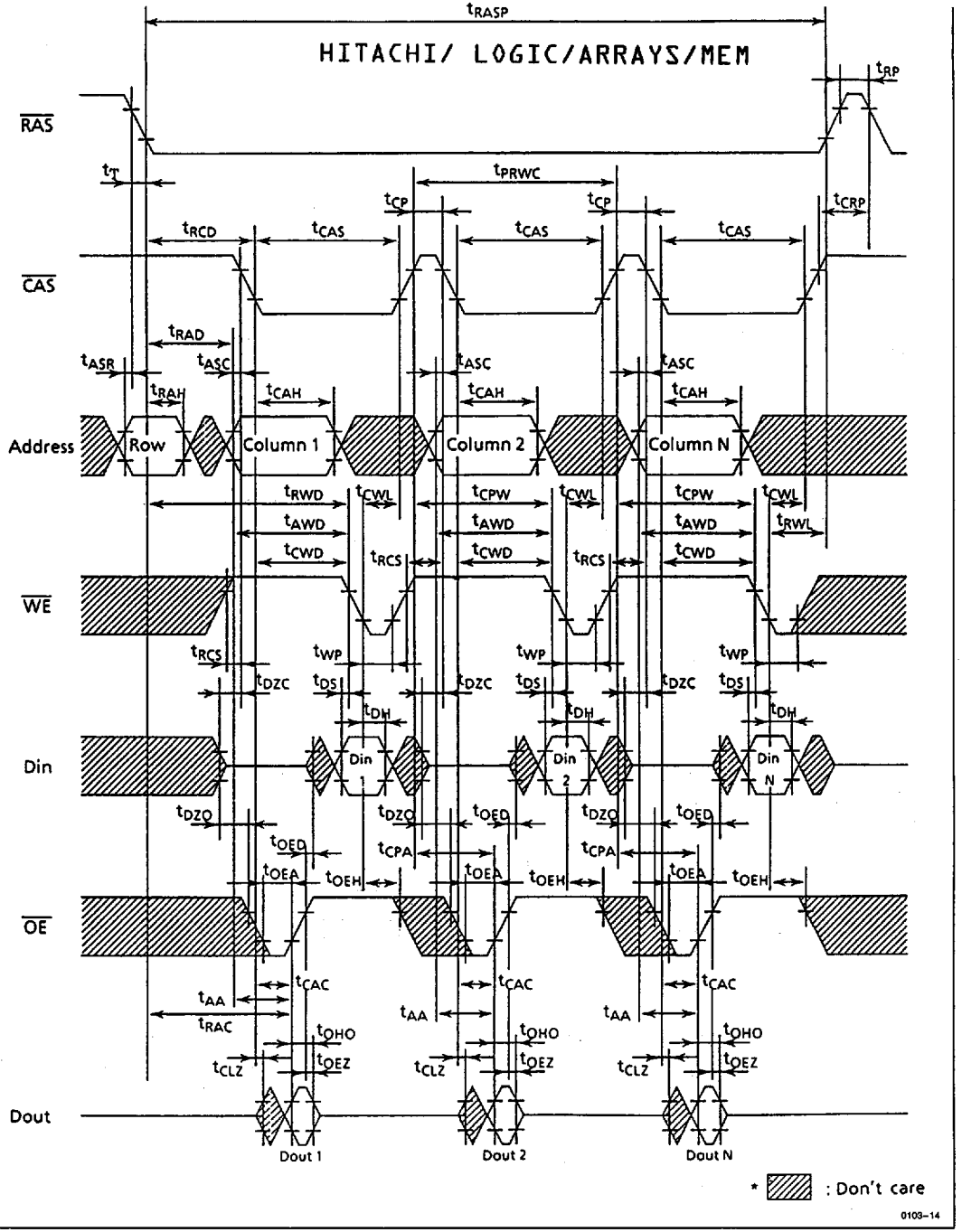


T-46-23-18


tRASP
tRP
RAS
tT
tCP
tCP
tCRP
tCSH
tPC
tRSH
tRCD
tCAS
tCAS
tCAS
CAS
tRAD
tASR
tASC
tASC
tASC
tRAH
tCAH
tCAH
tCAH
Address
Row
Column 1
Column 2
Column N
tCWL
tCWL
tCWL
tRWL
tRCS
tRCS
tRCS
WE
tWP
tWP
tWP
tDZC
tDS
tDZC
tDS
tDZC
tDS
tDH
tDH
tDH
Din
Din 1
Din 2
Din N
tDZO
tDZO
tOED
tDZO
tOED
tOED
tOEH
tOEH
tOEH
OE
tCLZ
tCLZ
tCLZ
tOEZ
tOEZ
tOEZ
Dout
Invalid Dout
Invalid Dout
Invalid Dout
* : Don't care
0103-13

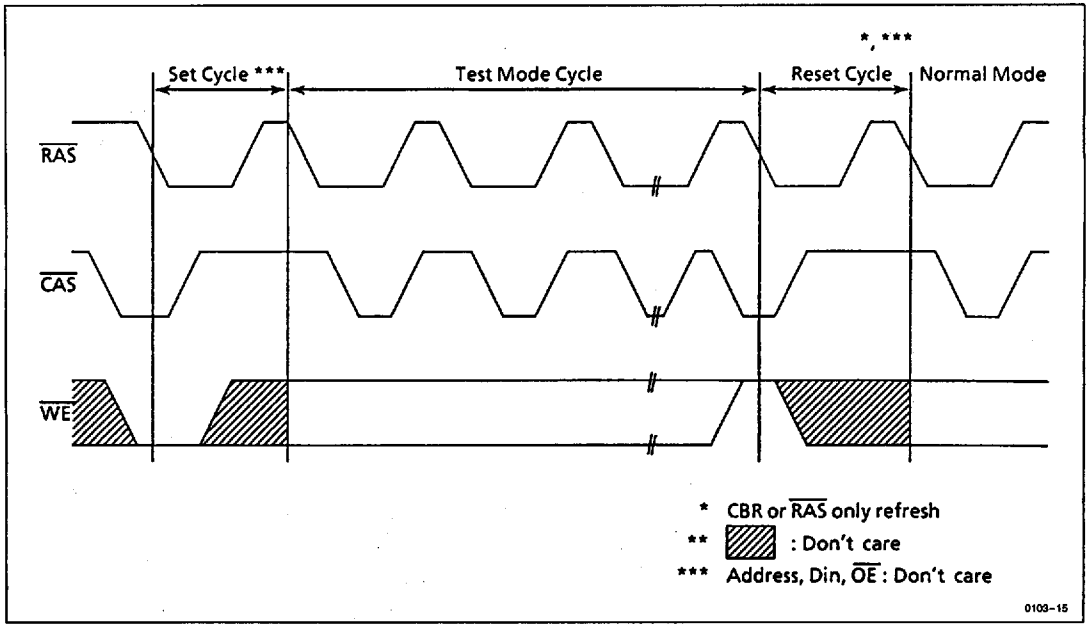
• **Fast Page Mode Read-Modify-Write Cycle**

T-46-23-18

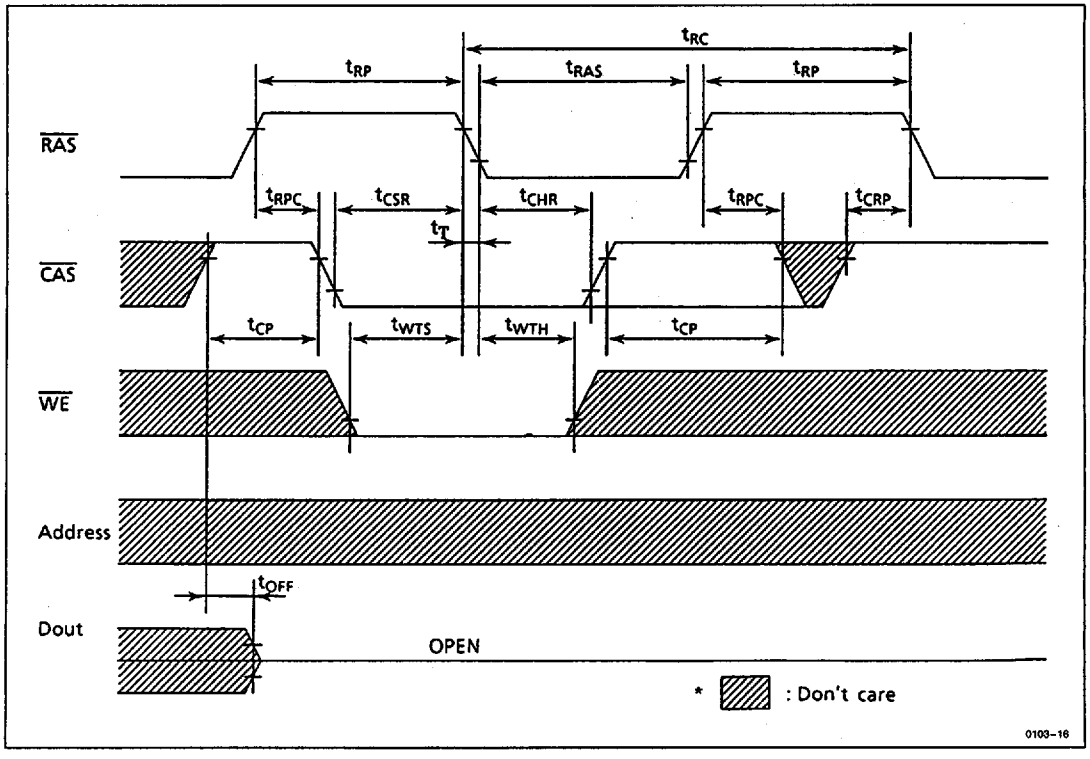


T-46-23-18

• **Test Mode Cycle**



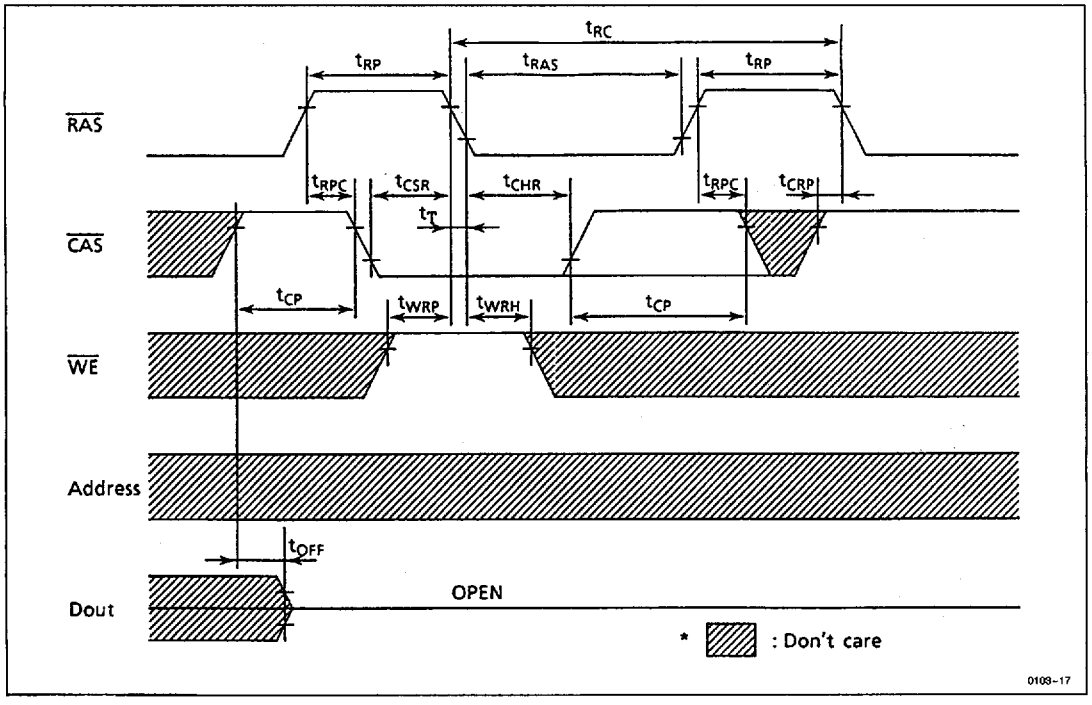
• **Test Mode Set Cycle**



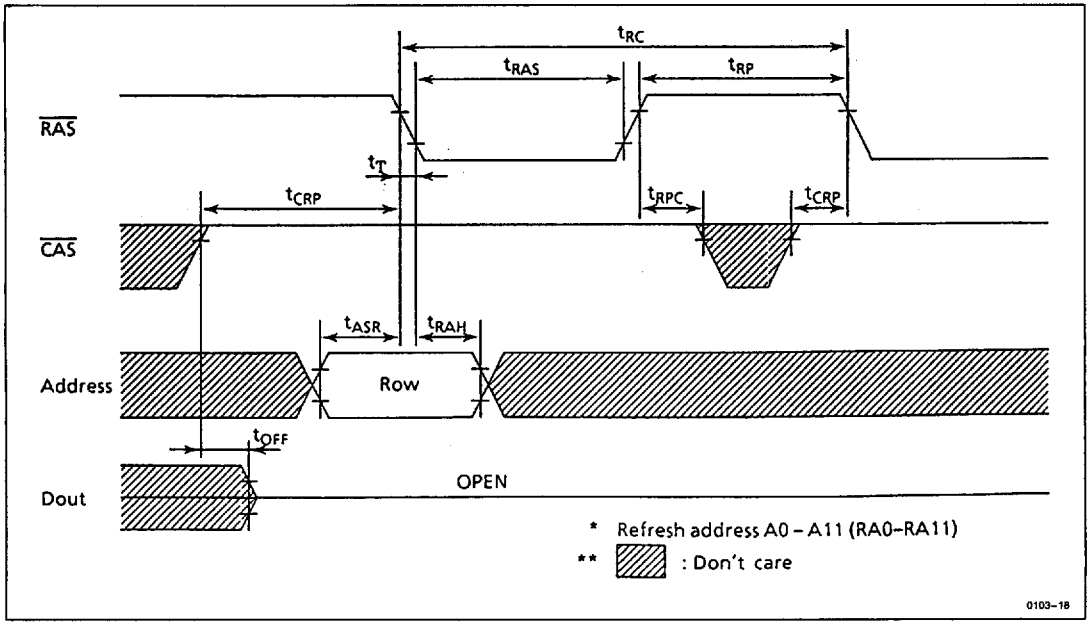
T-46-23-18

• **Test Mode Reset Cycle**

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Cycle

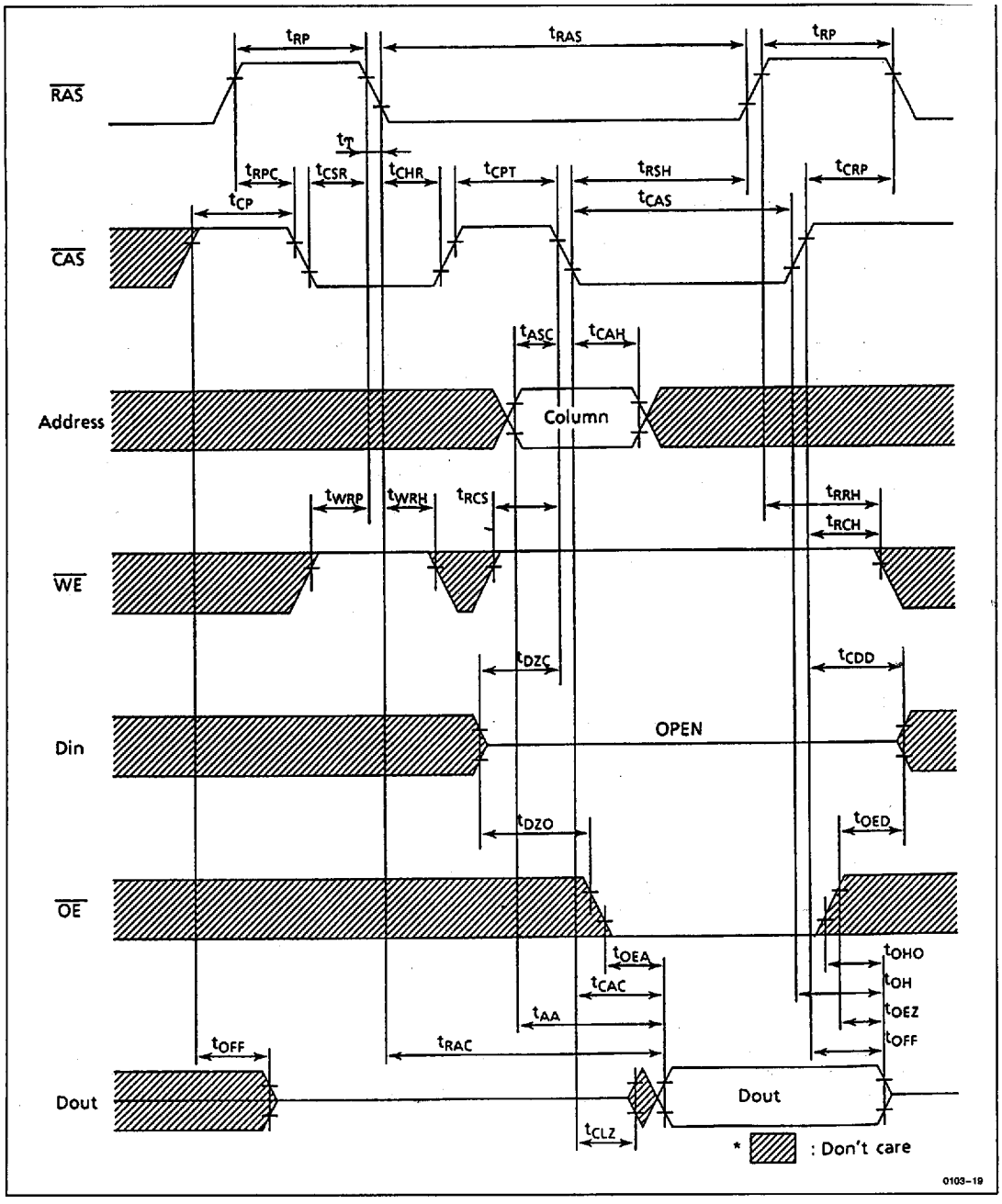


• **$\overline{RAS}$ Only Refresh Cycle**



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Read)

T-46-23-18



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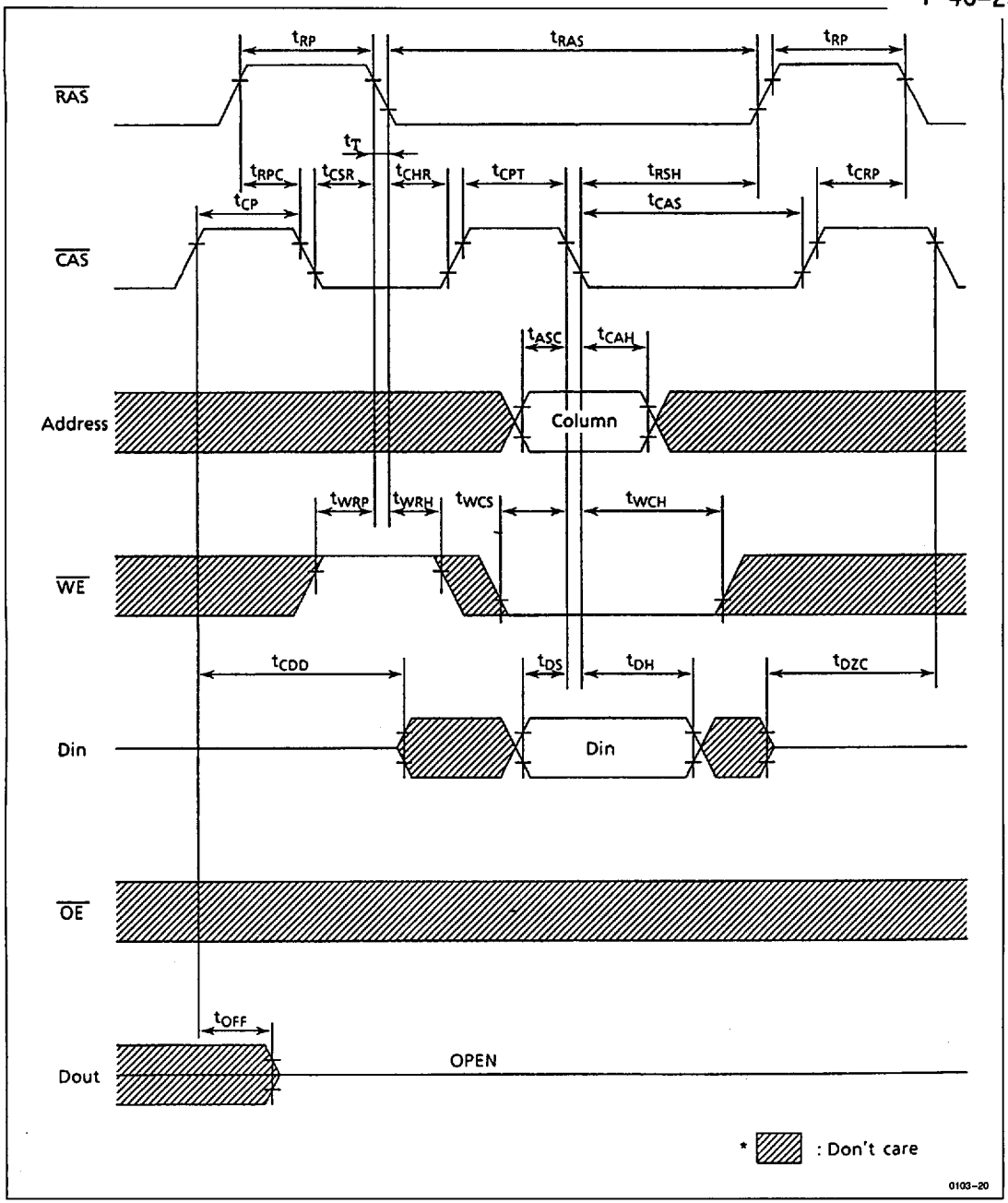
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Write)

T-46-23-18



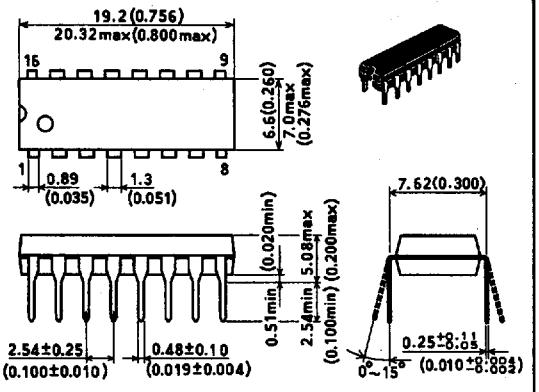
PACKAGE INFORMATION

T-90-20

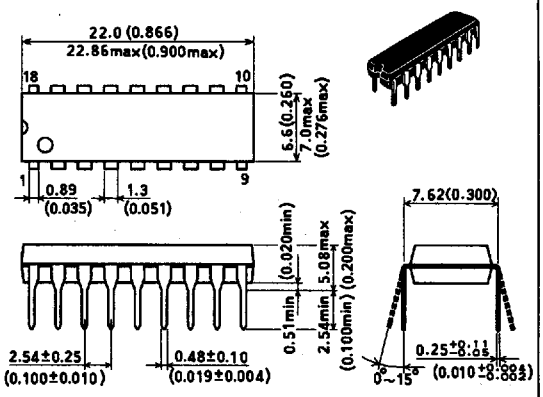
• Dual-in-line Plastic

Unit: mm (inch) Scale 3/2

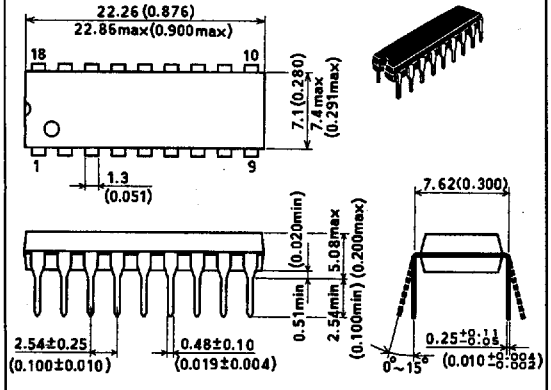
• DP-16B



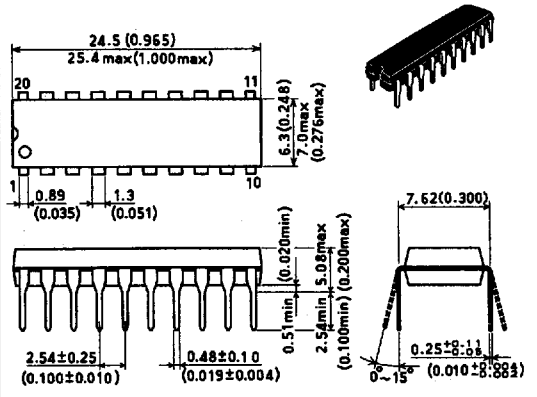
• DP-18B



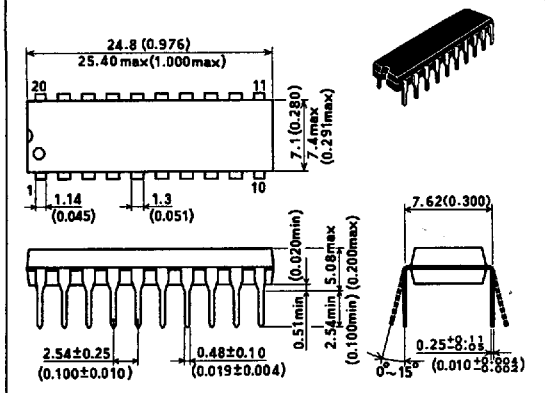
• DP-18C



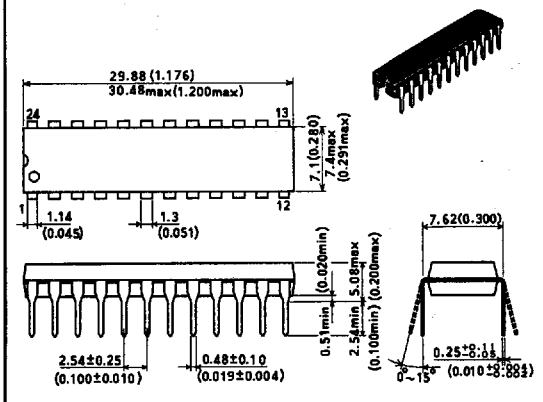
• DP-20N



• DP-20NA



• DP-20NC

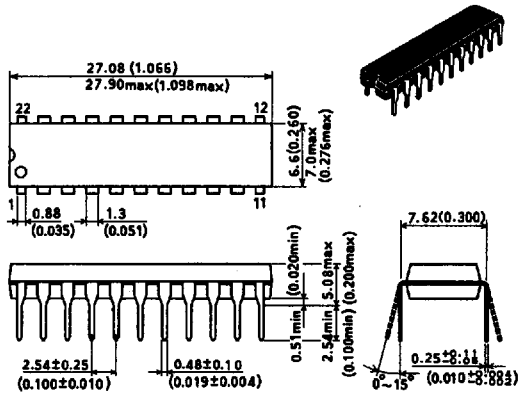


• Dual-in-line Plastic

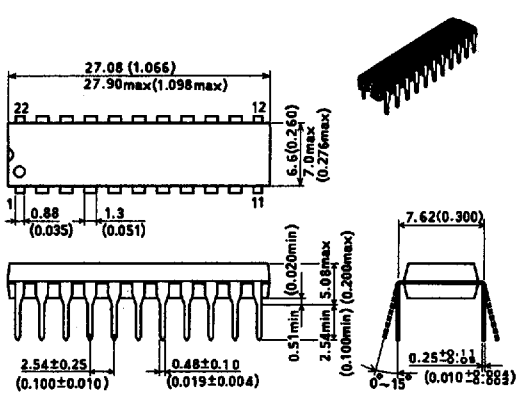
Unit: mm (inch) Scale 3/2

T-90-20

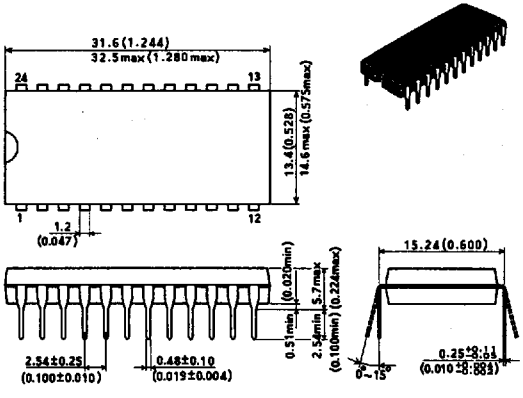
• DP-22N



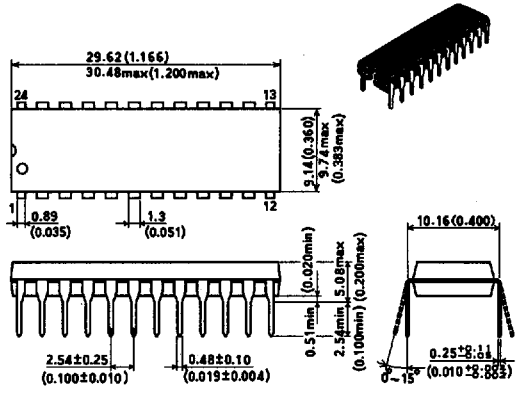
• DP-22NB



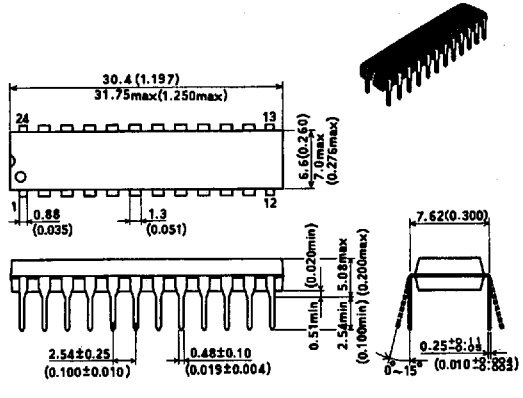
• DP-24



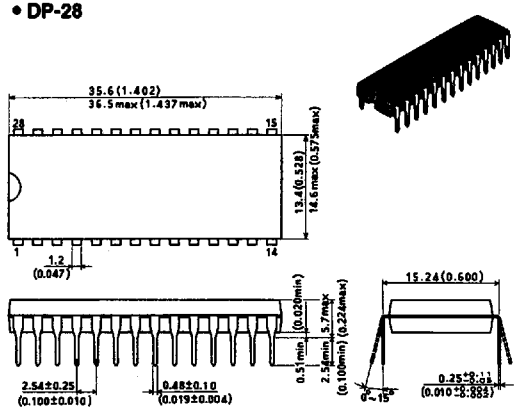
• DP-24A



• DP-24N



• DP-28



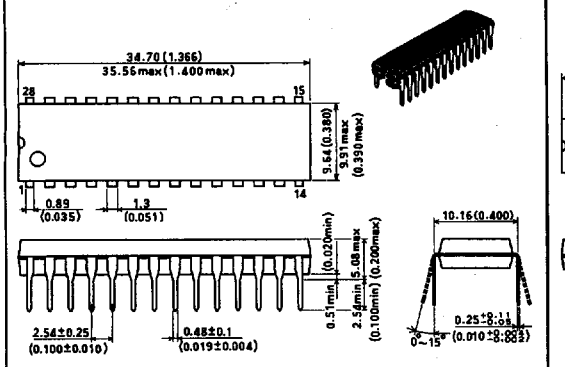
• Dual-in-line Plastic

HITACHI/ LOGIC/ARRAYS/MEM

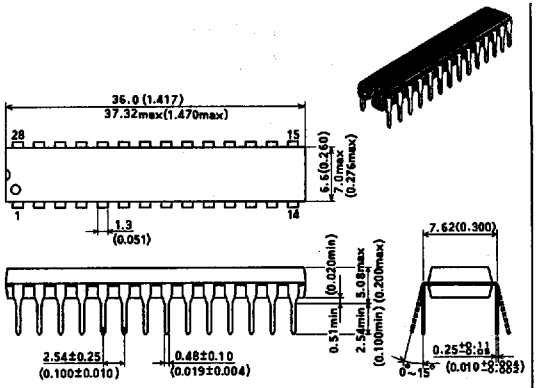
Unit: mm (inch) Scale 3/2

T-90-20

• DP-28C



• DP-28N

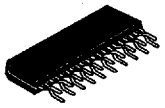


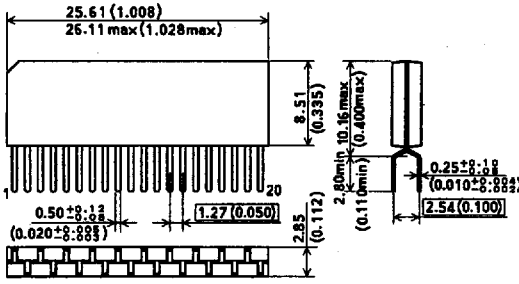
• Zigzag-in-line Plastic HITACHI/ LOGIC/ARRAYS/MEM

Unit: mm (inch) Scale 3/2

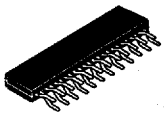
T-90-20

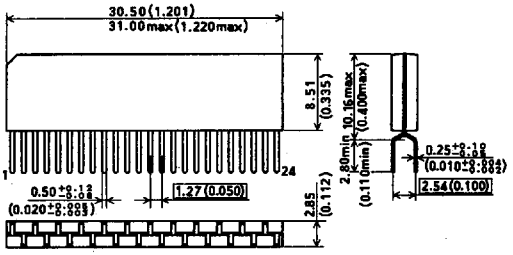
• ZP-20



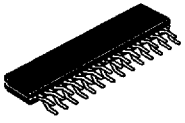


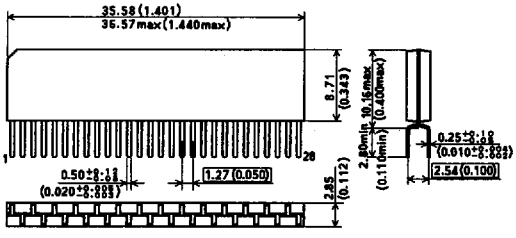
• ZP-24



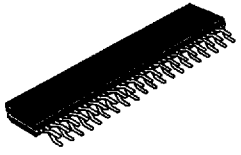


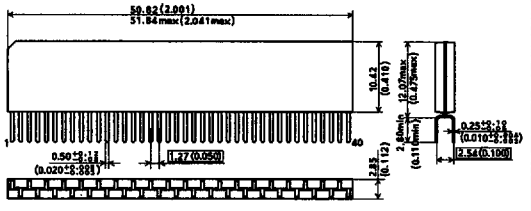
• ZP-28





• ZP-40





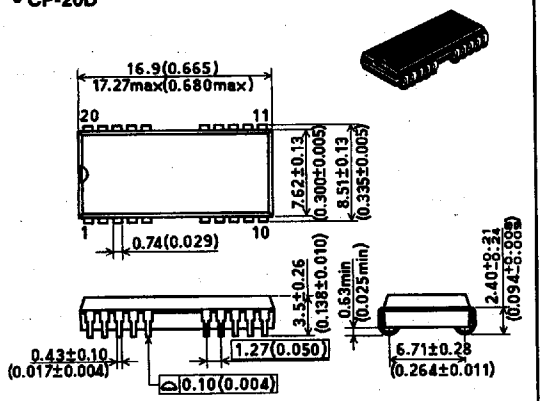
• Flat Package (J-bend Leads)

HITACHI/ LOGIC/ARRAYS/MEM

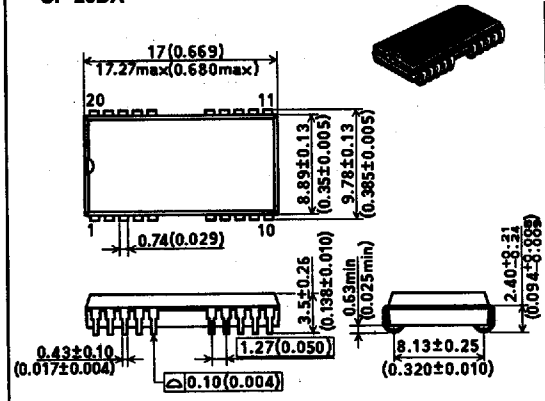
Unit: mm (inch) Scale 3/2

T-90-20

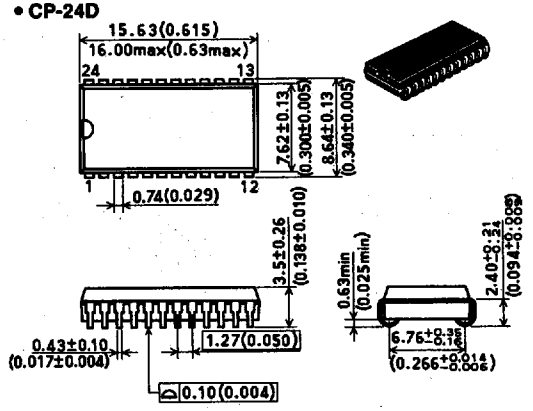
• CP-20D



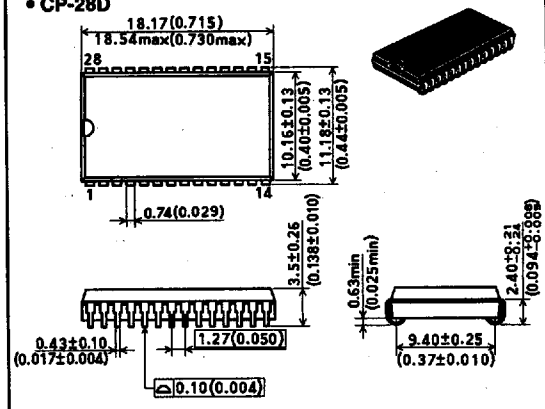
• CP-20DA



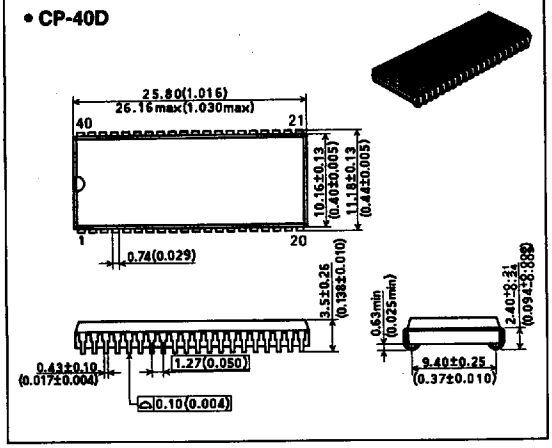
• CP-24D



• CP-28D



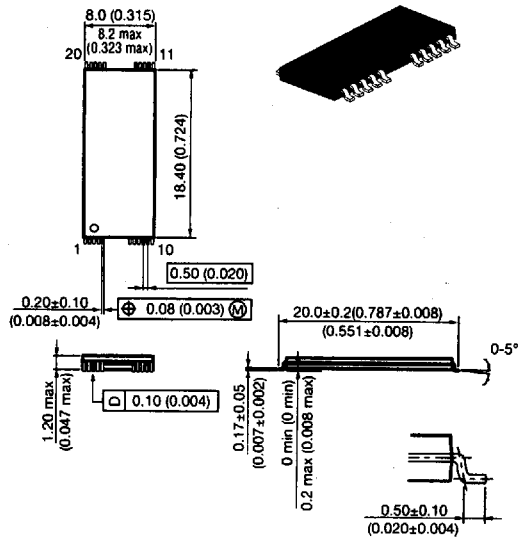
• CP-40D



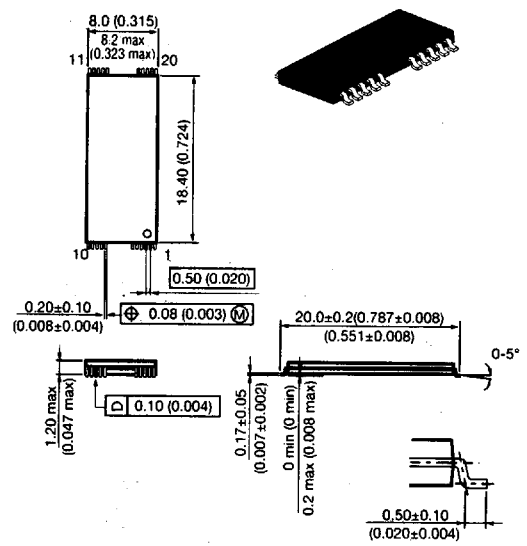
• TSOP (Thin Small Outline Package)

Unit: mm (inch) Scale 3/2

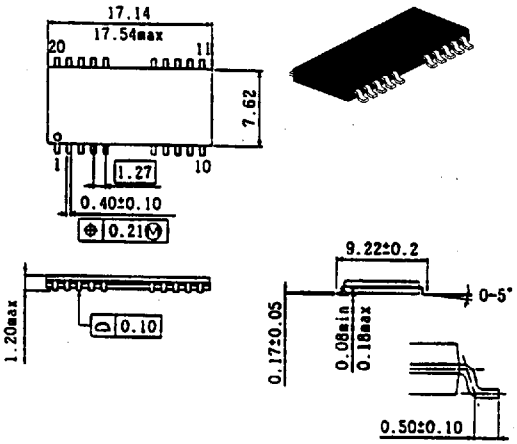
• TFP-20DA



• TFP-20DAR



• TTP-20D



• TTP-20DR