DESCRIPTION

The NN5116405B / NN5117405B series is a high performance CMOS Dynamic Random Access Memory organized as 4,194,304 words by 4-bits. The NN5116405B / NN5117405B series is fabricated with advanced CMOS technology and designed with innovative design techniques resulting in high speed, extremely low power and wide operating margins at both component and system levels.

The NN5116405B / NN5117405B series features an EDO (Hyper page) mode operation in which a high speed read, write or read-write is performed on any column address along a row address.

An extremely short row address capture time and an asynchronous column address decoder relax the timing constraints associated with address multiplexing.

Refresh is accomplished by performing $\overline{RAS}$ only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or normal read or write cycles on the 4,096 address combinations of A0 to A11 during a 64 ms period for the NN5117405A series. (2,048 address combinations of A0 to A10 during a 32 ms period for the NN5117405B series.)

Multiplexed address inputs permit The NN5116405B / NN5117405B series to be packaged in a standard 26-pin plastic SOJ, 26-pin TSOP TYPE II. The package sizes provide high system bit densities and are compatible with widely available automated testing and insertion equipment. System level features include single power supply of 5V ±10% tolerance and direct interface with high performance TTL logic families.

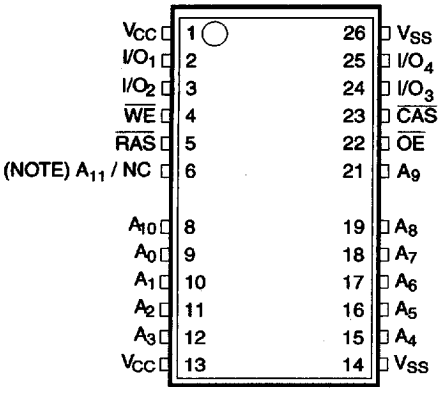
FEATURES

- 4,194,304 × 4 bit Organization
- Single 5V ±10% Power Supply
- Performance Ranges

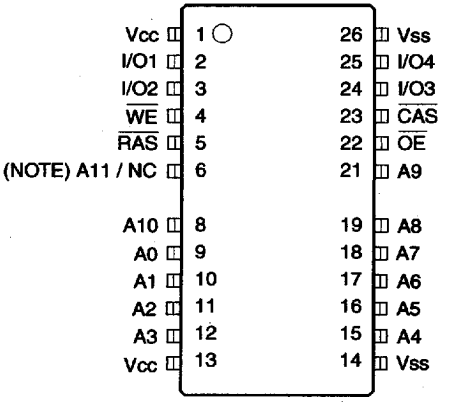
Parameter	-40	-50	-60
Max. $\overline{RAS}$ Access Time (t_{RAC})	40ns	50ns	60ns
Max. $\overline{CAS}$ Access Time (t_{CAC})	11ns	13ns	15ns
Max. Column Address Access Time (t_{AA})	20ns	25ns	30ns
Min.Read/Write Cycle Time (t_{RC})	80ns	90ns	110ns

- EDO (Hyper Page) Mode Operation
- Low Power Operation
  Low Standby Current (CMOS level inputs)
  – Standard 1mA
  – L version 150µA
- NN5116405B : 4,096 Refresh Cycles
  NN5117405B* : 2,048 Refresh Cycles
  – Standard distributed across 64ms/32ms*
  – L version distributed across 128ms
- Self Refresh Mode
  (L version)
- All inputs/Outputs and Clocks
  fully TTL and CMOS compatible
- Refresh Modes
  $\overline{RAS}$ only
  $\overline{CAS}$ before $\overline{RAS}$
  Hidden Refresh
- 16bit Parallel Test Mode
- High Reliability Packages
  Plastic 26pin SOJ (P26/24SJ-2A-L)
  Plastic 26pin TSOP TYPE II (P26/24TP-2A-L)

PIN CONFIGURATION (TOP VIEW)



26/24-pin SOJ (300 mil)
P26/24SJ-2A-L



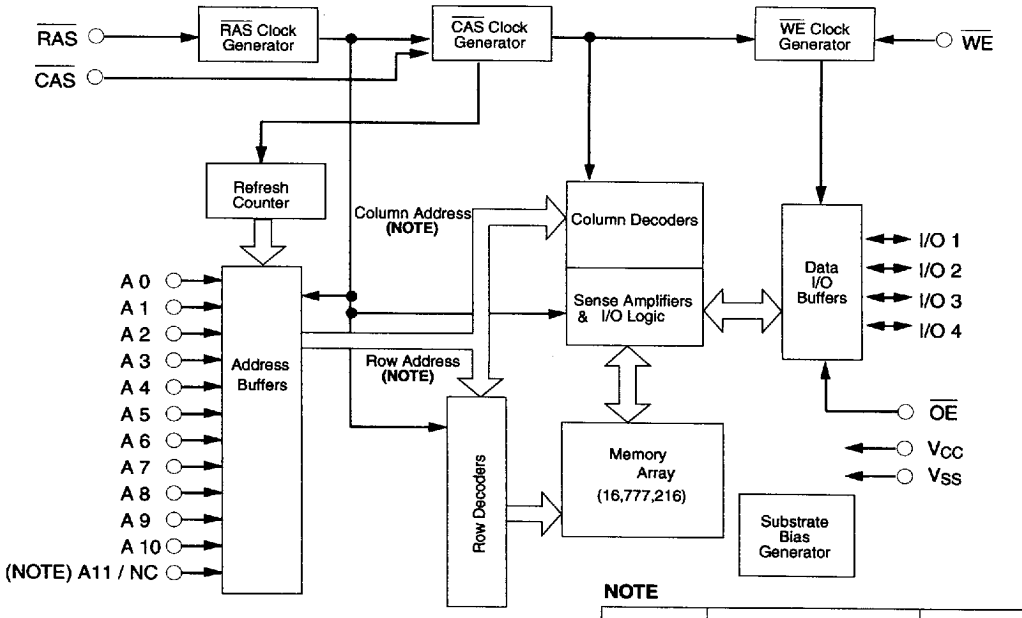
26/24-pin TSOP TYPE (II) (300 mil)
P26/24TP-2A-L

NOTE A_{11} : NN5116405B
NC : NN5117405B

PIN NAMES

A0 - A11	Address Inputs (NOTE)
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{OE}$	Output Enable
I/O1~I/O4	Data-in / Data-out
$\overline{WE}$	Write Enable
V_{CC}	+5V Supply
V_{SS}	Ground

FUNCTIONAL BLOCK DIAGRAM



NOTE

	Address / Row Address	ColumnAddress
NN5116405B	A0 - A11	A0 - A9
NN5117405B	A0 - A10	A0 - A10

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
Voltage on Any Pin Relative to V_{SS}	Vin, Vout	−1 to 7	V
Voltage on Vcc Relative to V_{SS}	V_{CC}	−1 to 7	V
Storage Temperature (Plastic)	Tstg	−55 to +125	°C
Power Dissipation	Pd	1.0	W
Ambient Operating Temperature	Ta	0 to + 70	°C
Short Circuit Output Current	Iout	50	mA

Permanent device damage can occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage, All Inputs	2.4	—	6.5	V
V_{IL}	Input Low Voltage, All Inputs	−1.0	—	0.8	V

Note: All voltage values in this data sheet are with respect to V_{SS} unless otherwise specified.

DC ELECTRICAL CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	SPEED	MIN.	MAX.	UNIT	TEST CONDITIONS	NOTES
I_{CC1}	Operating Current	-40 -50 -60		110/130* 100/120* 90/110*	mA mA mA	t_{RC} = t_{RC} (min.) $\overline{RAS}$, $\overline{CAS}$, Address cycling	1, 2, 3
I_{CC2}	Standby Current			1.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ (V_{CC} - 0.2V)	
				2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH}	
	Standby Current (L version)			150	µA	$\overline{RAS}$ = $\overline{CAS}$ ≥ (V_{CC} - 0.2V) All other inputs are stable at (V_{CC} - 0.2V) or (V_{SS} + 0.2V)	
I_{CC3}	Refresh Current ($\overline{RAS}$ only refresh)	-40 -50 -60		110/130* 100/120* 90/110*	mA mA mA	t_{RC} = t_{RC} (min.) $\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}	1, 3
I_{CC4}	EDO (Hyper) Page Mode Current	-40 -50 -60		110 100 90	mA mA mA	t_{HPC} = t_{HPC} (min.) $\overline{RAS}$ = V_{IL} $\overline{CAS}$, Address cycling	1, 2
I_{CC5}	Refresh Current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	-40 -50 -60		110/130* 100/120* 90/110*	mA mA mA	t_{RC} = t_{RC} (min.) $\overline{RAS}$, $\overline{CAS}$ cycling	1, 3
I_{CC6}	Refresh Current $\overline{CAS}$ before $\overline{RAS}$ refresh)			500	µA	4,096 (2,048*) cycles / 128ms t_{RAS} ≤ 200ns, $\overline{WE}$ ≥ (V_{CC} - 0.2V) All other inputs are stable at (V_{CC} - 0.2V) or (V_{SS} + 0.2V)	3
I_{CC7}	Self Refresh Mode Current			300	µA	$\overline{RAS}$ =$\overline{CAS}$ ≤ (V_{SS} + 0.2V) All other input high levels are (V_{CC} - 0.2V) or input low levels are (V_{SS} + 0.2V)	
$\|I_{LI}\|$	Input Leakage Current (Any input pin)		-10	10	µA	0V ≤ V_{IH} ≤ 5.5V, Others = 0V	
$\|I_{LO}\|$	Output Leakage Current (For high impedance state)		-10	10	µA	$\overline{RAS}$ ≥ V_{IH}(min), $\overline{CAS}$ ≥ V_{IH}(min) 0V ≤ V_{OUT} ≤ 5.5V	
V_{OH}	Output High Voltage		2.4		V	I_{OH} = –5.0 mA	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.2 mA	

Notes: 1. I_{CC1} , I_{CC3} , I_{CC4} and I_{CC5} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the outputs open.
3. * indicates NN5117405 series' characteristis.

CAPACITANCE (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ±10%, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{IN1}	Address A0 ~ A11 : NN5116405B	—	5	pF
	A0 ~ A10 : NN5117405B	—	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$,$\overline{OE}$	—	5	pF
C_{OUT}	I/O1,I/O2,I/O3,I/O4	—	7	pF

AC ELECTRICAL CHARACTERISTICS

Test conditions : V_{IH} / V_{IL} = 2.4V / 0.8V V_{OH} / V_{OL} = 2.4V / 0.4V output loading C_L = 100pF + 2TTL

Operating conditions : (0 °C≤Ta≤70°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V) (NOTES 3, 4, 5)

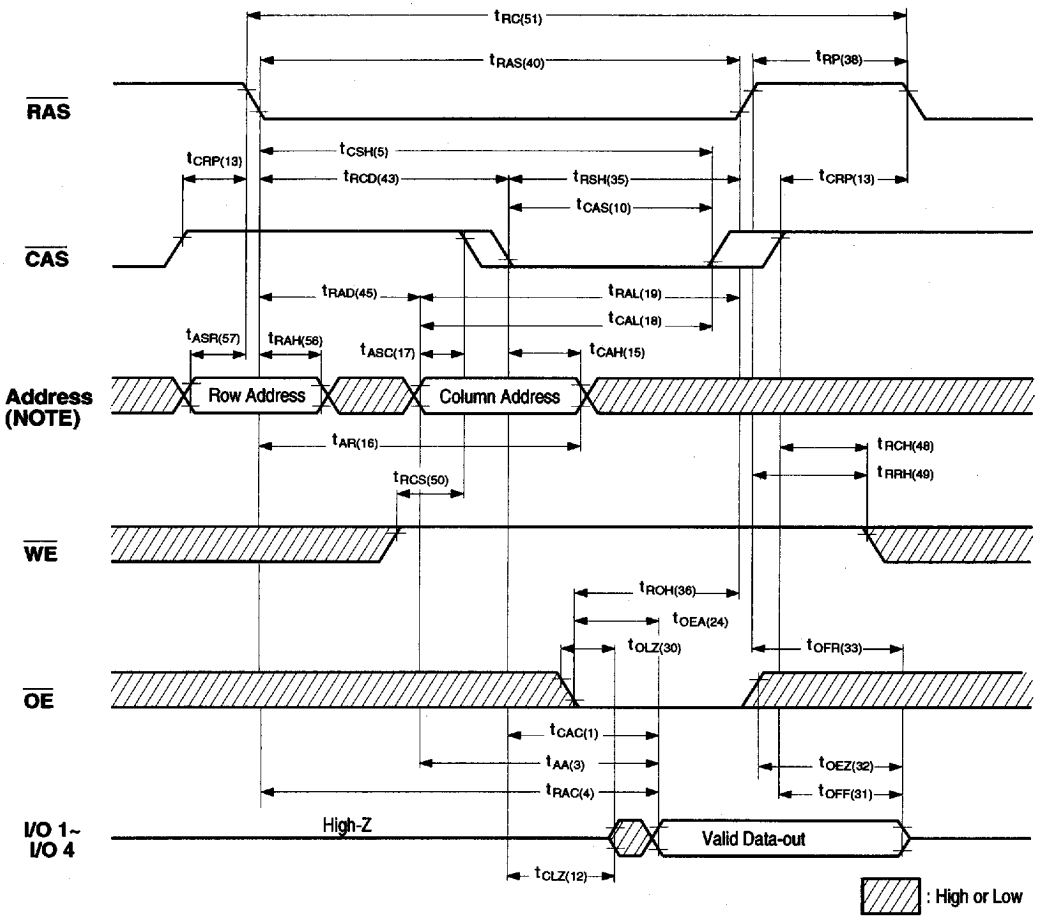
NO.	NOTES		PARAMETER	-40		-50		-60		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$	—	11	—	13	—	15	ns	6,13
2	t_{CH2QV}	t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	25	—	30	—	35	ns	13,14
3	t_{AVQV}	t_{AA}	Access Time from Column Address	—	20	—	25	—	30	ns	7,13
4	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$	—	40	—	50	—	60	ns	6,7
5	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	30	—	35	—	40	—	ns	
6	t_{RL1CX}	t_{CHS}	$\overline{CAS}$ Hold Time (Self Refresh Mode)	-50	—	-50	—	-50	—	ns	
7	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	10	—	10	—	10	—	ns	
8	t_{CH2CL2}	t_{CPN}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	7	—	7	—	10	—	ns	
9	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	5	—	5	—	5	—	ns	14
10	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	8	100K	8	100K	10	100K	ns	
11	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	5	—	5	—	5	—	ns	
12	t_{CL1QX}	t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	0	—	ns	8
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	5	—	ns	
14	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	32	—	32	—	37	—	ns	11
15	t_{CL1AX}	t_{CAH}	Column Address Hold Time	7	—	7	—	10	—	ns	
16	t_{RL1AX}	t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	30	—	35	—	40	—	ns	
17	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0	—	0	—	0	—	ns	14
18	t_{AVCH1}	t_{CAL}	Column Address to CAS Lead Time	10	—	13	—	18	—	ns	
19	t_{AVRH1}	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	20	—	25	—	30	—	ns	
20	t_{AVWL2}	t_{AWD}	Column Address to $\overline{WE}$ Delay Time	39	—	39	—	47	—	ns	11
21	t_{CL1DX} t_{WL1DX}	t_{DH}	Data Hold Time	7	—	7	—	10	—	ns	12
22	t_{CL2QX}	t_{DHC}	Data Output Hold Time	0	—	0	—	0	—	ns	
23	t_{DVCL2} t_{DVWL2}	t_{DS}	Data Setup Time	0	—	0	—	0	—	ns	12
24	t_{OL1QV}	t_{OEA}	$\overline{OE}$ Access Time	—	11	—	13	—	15	ns	
25	t_{WL1OL2}	t_{OEH}	$\overline{OE}$ Command Hold Time	10	—	13	—	15	—	ns	
26	t_{GH2GL2}	t_{OPZ}	$\overline{OE}$ Pulse Width for Output Disable When $\overline{CAS}$ High	7	—	7	—	7	—	ns	
27	t_{GL1CH1}	t_{OCS}	OE Setup Time to $\overline{CAS}$ High	7	—	7	—	7	—	ns	
28	t_{GL1RH1}	t_{ORS}	$\overline{OE}$ Setup Time to $\overline{RAS}$ High	7	—	7	—	7	—	ns	
29	t_{CH2QV}	t_{OED}	$\overline{OE}$ to Data Delay Time	10	—	15	—	15	—	ns	
30	t_{GL2QX}	t_{OLZ}	$\overline{OE}$ to Output in low-Z	0	—	0	—	0	—	ns	
31	t_{CH2QZ}	t_{OFF}	Output Buffer Turn-off Delay Time	0	13	0	13	0	15	ns	10,17
32	t_{OH2QX}	t_{OEZ}	Output Buffer Turn-off Delay Time Referenced to $\overline{OE}$	0	13	0	13	0	15	ns	
33	t_{RHQZ}	t_{OFR}	Output Buffer Turn-off Delay Time Referenced to $\overline{RAS}$	0	13	0	13	0	15	ns	16
34	t_{WL2QZ}	t_{WEZ}	Output Buffer Turn-off Delay Time Referenced to $\overline{WE}$	0	13	0	13	0	15	ns	

NO.	SYMBOL		PARAMETER	-40		-50		-60		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
35	t_{CL1RH1}	t_{RSH}	$\overline{RAS}$ Hold Time	10	—	13	—	15	—	ns	
36	t_{OL1RH1}	t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	10	—	10	—	10	—	ns	
37	t_{CH2RH1}	t_{RHCP}	$\overline{RAS}$ Hold Time Referenced $\overline{CAS}$ Precharge	25	—	30	—	35	—	ns	
38	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	25	—	25	—	30	—	ns	
39	t_{RH2RL2}	t_{RPS}	$\overline{RAS}$ Precharge Time (Self Refresh Mode)	72	—	90	—	110	—	ns	
40	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	40	100K	50	100K	60	100K	ns	
41	t_{RL1RH1}	t_{RASS}	$\overline{RAS}$ Pulse Width (Self Refresh Mode)	300	—	300	—	300	—	µs	
42	t_{RL1RH1}	t_{RASP}	$\overline{RAS}$ Pulse Width (EDO (Hyper Page) Mode)	40	100K	50	100K	60	100K	ns	
43	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	10	27	13	35	13	45	ns	6
44	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	—	5	—	5	—	ns	
45	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	9	25	11	25	11	30	ns	7
46	t_{RL2QX}	t_{RLZ}	$\overline{RAS}$ To Output in Low-Z	0	—	0	—	0	—	ns	
47	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	60	—	64	—	77	—	ns	11
48	t_{CH2WL2}	t_{RCH}	Read Command Hold Time	0	—	0	—	0	—	ns	9
49	t_{RH2WL2}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	—	0	—	0	—	ns	9
50	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0	—	0	—	0	—	ns	
51	t_{RL2RL2}	t_{RC}	Random Read or Write Cycle Time	80	—	90	—	110	—	ns	
52	t_{CL2CL2}	t_{HPC}	Read or Write Cycle Time (EDO (Hyper Page) Mode)	16	—	20	—	25	—	ns	13,14
53	t_{RL2RL2}	t_{RMW}	Read-Modify-Write Cycle Time	110	—	120	—	140	—	ns	
54	t_{CL2CL2}	t_{PRMW}	Read-Modify-Write Cycle Time (EDO (Hyper Page) Mode)	52	—	55	—	65	—	ns	13,14
55	t_{REF}	t_{REF}	Refresh Period NN5116405B	—	64	—	64	—	64	ms	15
			Refresh Period NN5117405B	—	32	—	32	—	32	ms	15
56	t_{RL1AX}	t_{RAH}	Row Address Hold Time	6	—	8	—	8	—	ns	
57	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0	—	0	—	0	—	ns	
58	t_T	t_T	Transition Time (Rise and Fall)	1	50	1	50	1	50	ns	4,5
59	t_{WL1WH1}	t_{WPZ}	$\overline{WE}$ Pulse Width for Disable When $\overline{CAS}$ High	7	—	7	—	7	—	ns	
60	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	7	—	10	—	10	—	ns	
61	t_{WL1WH1}	t_{WP}	Write Command Pulse Width	7	—	10	—	10	—	ns	
62	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0	—	0	—	0	—	ns	11
63	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	7	—	7	—	10	—	ns	
64	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	7	—	7	—	10	—	ns	
65	t_{WL1RL2}	t_{WSR}	Write Command Setup Time (Test Mode)	10	—	10	—	10	—	ns	
66	t_{RL1WH1}	t_{WHR}	Write Command Hold Time (Test Mode)	10	—	10	—	10	—	ns	
67	t_{WH2RL2}	t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time (CAS before RAS)	10	—	10	—	10	—	ns	
68	t_{RL1WH2}	t_{WRH}	$\overline{WE}$ to RAS Hold Time (CAS before RAS)	10	—	10	—	10	—	ns	

Notes:

3. Eight Initialization Cycles are required following a 200μs pause after Power Up. These Initialization Cycles may consist of any combination of the following : $\overline{RAS}$ only refresh Cycles, Read Cycles, Write Cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh Cycles.
4. AC measurements assume t_T=2ns.
5. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
6. Operation within the t_{RCD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
7. Operation within the t_{RAD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
8. Assumes three state test load (5pF and a 220 ohm to 1.3V Thevenin equivalent).
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. t_{OFF}(max.) defines the time at which the output achieves an open circuit condition and is not referenced to output voltage levels. t_{OFF} only applies when $\overline{RAS}$ is high.
11. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.) , the cycle is an early write cycle and data-out pins will remain open circuit (high impedance) throughout the entire cycle. If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.) and $t_{AWD} \geq t_{AWD}$(min.), the cycle is a read-modify-write cycle and the data-out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data-out (at access time) is indeterminate.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in read-modify-write cycles.
13. Access time is determined by the longer of t_{AA}, t_{CAC}, or t_{CPA}.
14. $t_{ASC} \geq t_{CP}$ to achieve t_{PC}(min.) and t_{CPA}(max.) values.
15. t_{REF}=128msec for Long Refresh version (L version).
16. t_{OFR} applies only when $\overline{CAS}$ is high.
17. Output buffers turn into Hi-Z by the later rising edge of $\overline{RAS}$ or $\overline{CAS}$, Therefore t_{OFF} and t_{OFR} are determined by the later rising edge of $\overline{RAS}$ or $\overline{CAS}$.

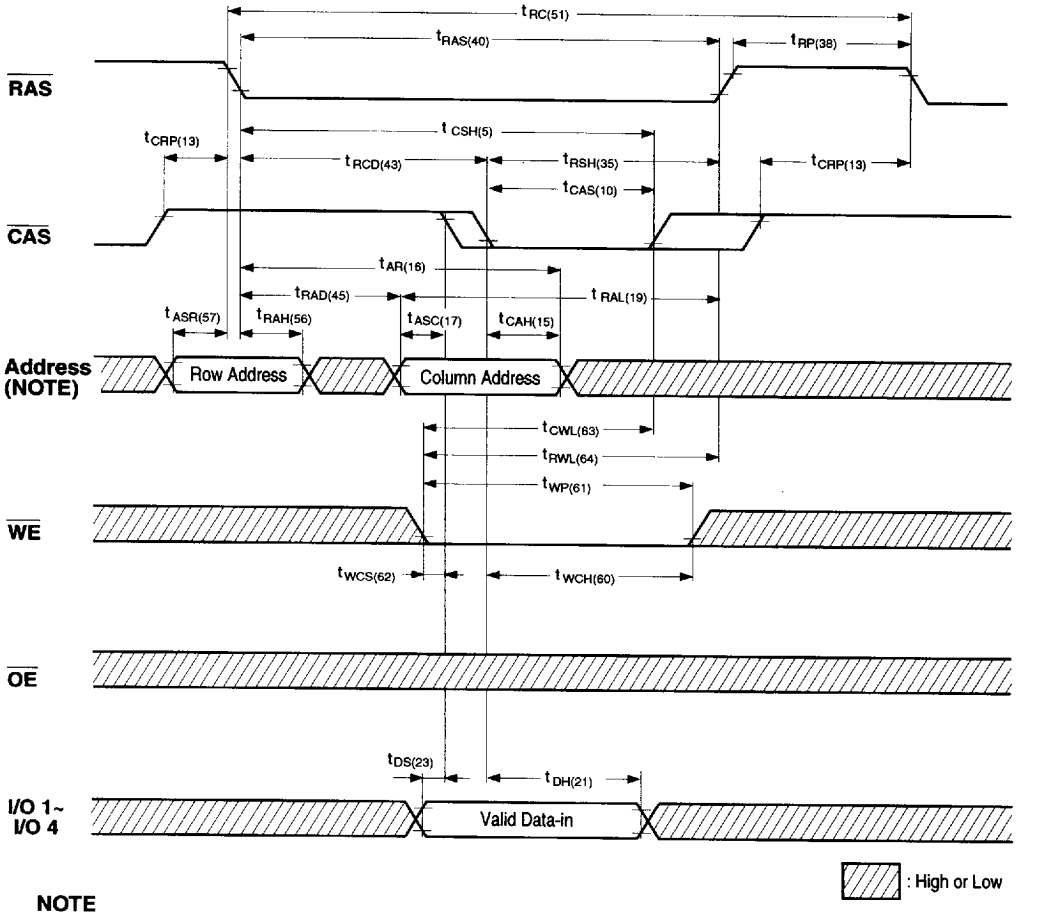
READ CYCLE



NOTE

Address A0 - A11 : NN5116405B
A0 - A10 : NN5117405B

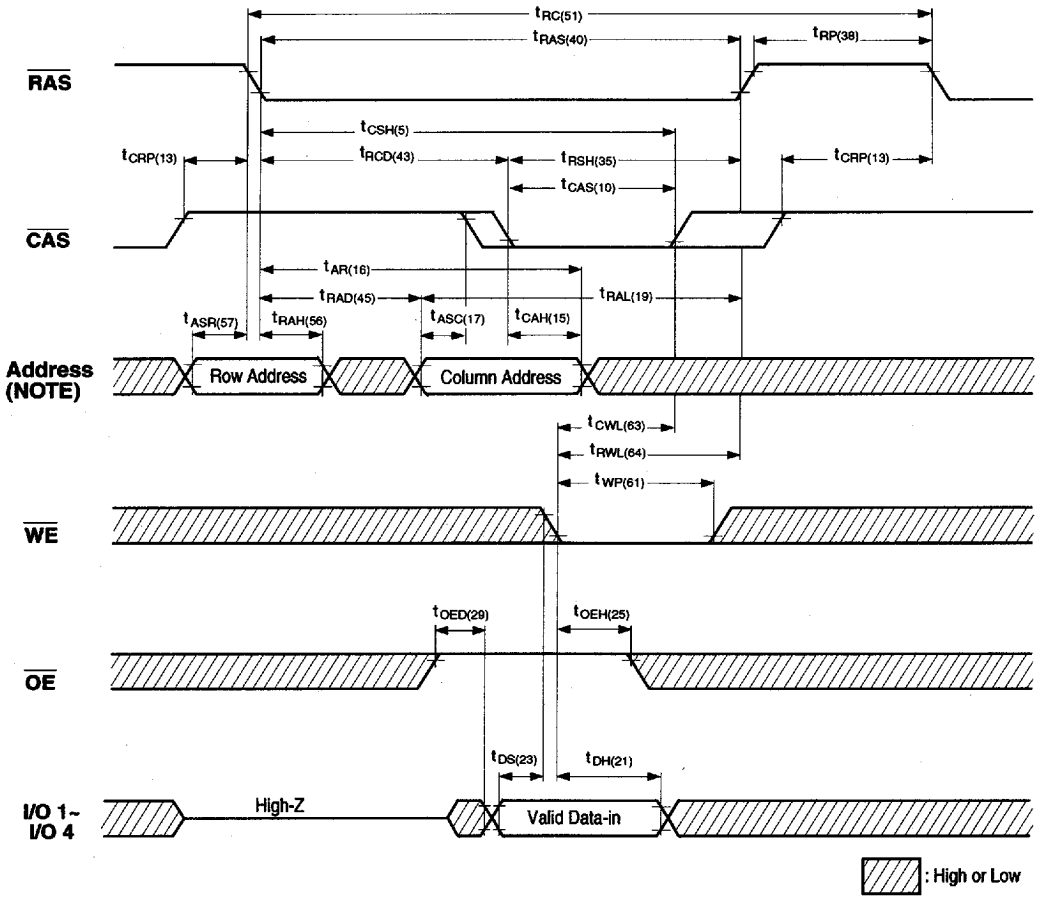
WRITE CYCLE (EARLY WRITE)



NOTE

Address A0 - A11 : NN5116405B
A0 - A10 : NN5117405B

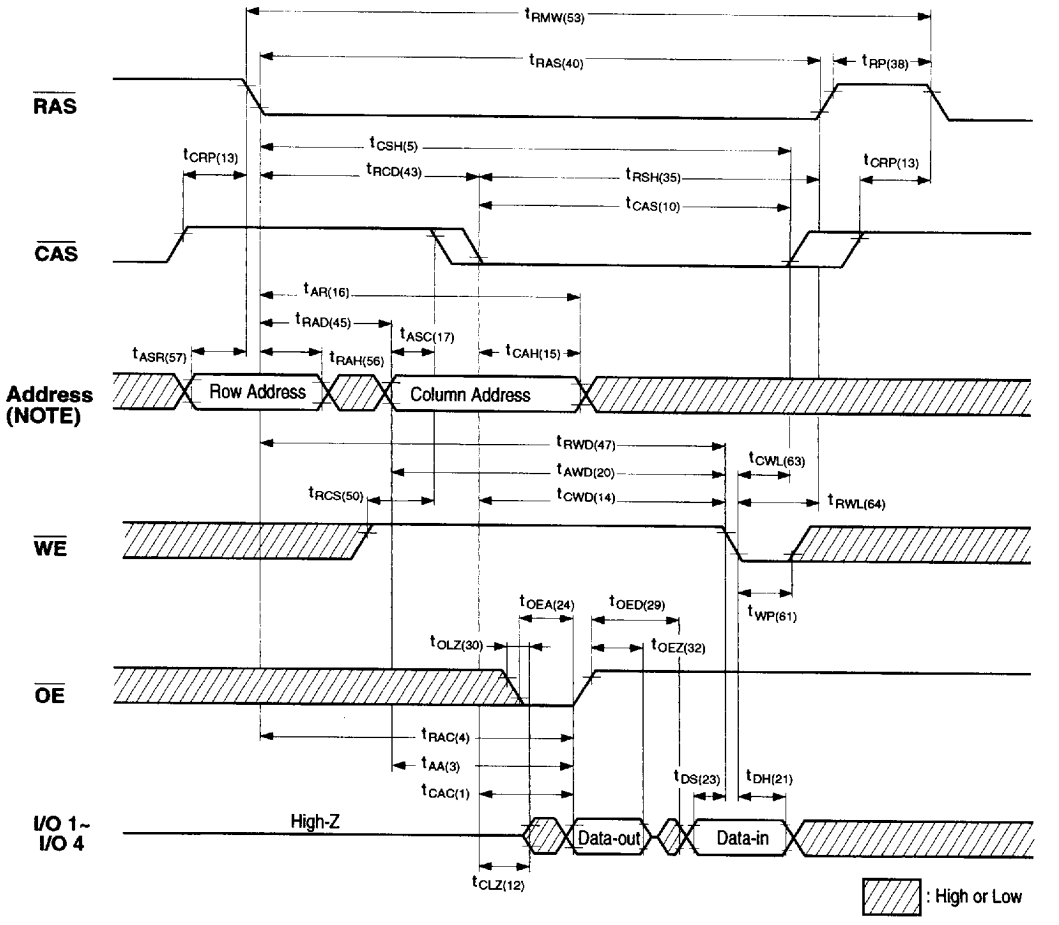
WRITE CYCLE (OE-CONTROLLED WRITE)



NOTE

Address A0 - A11 : NN5116405B
A0 - A10 : NN5117405B

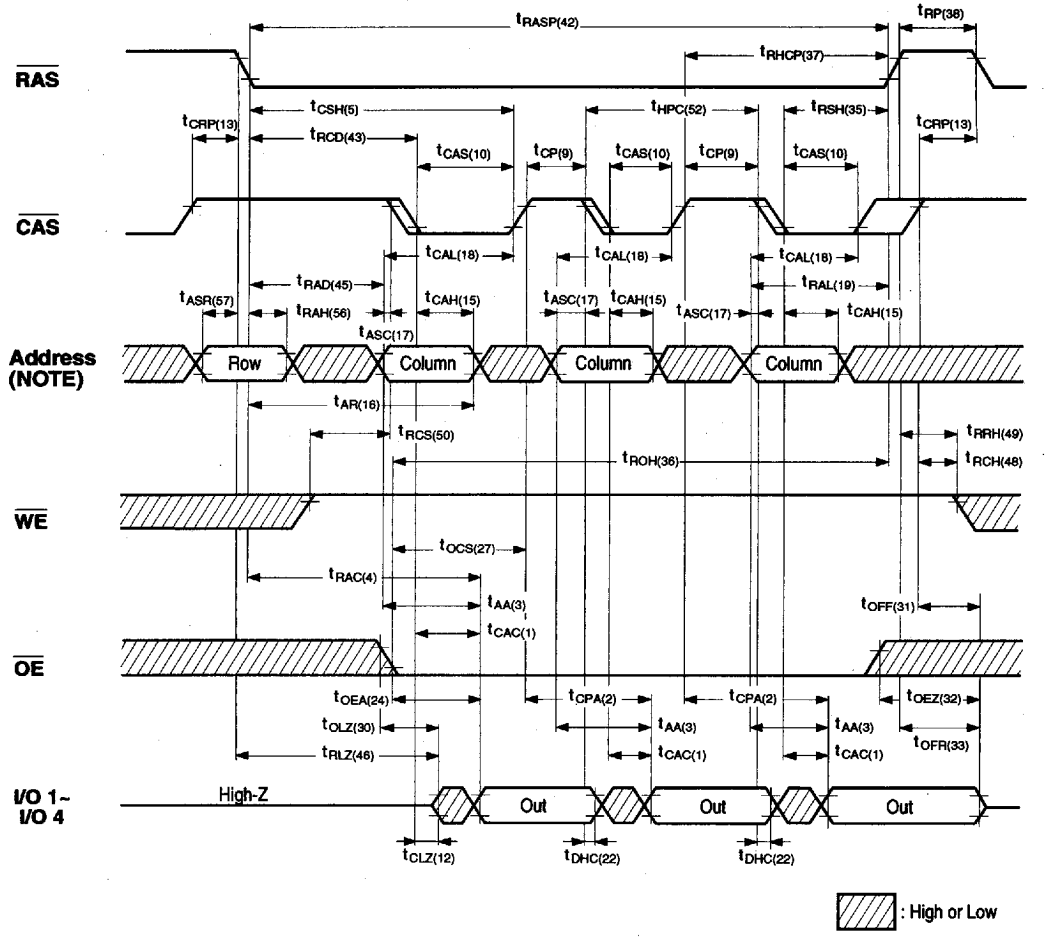
READ-MODIFY-WRITE CYCLE



NOTE

Address A0 - A11 : NN5116405B
A0 - A10 : NN5117405B

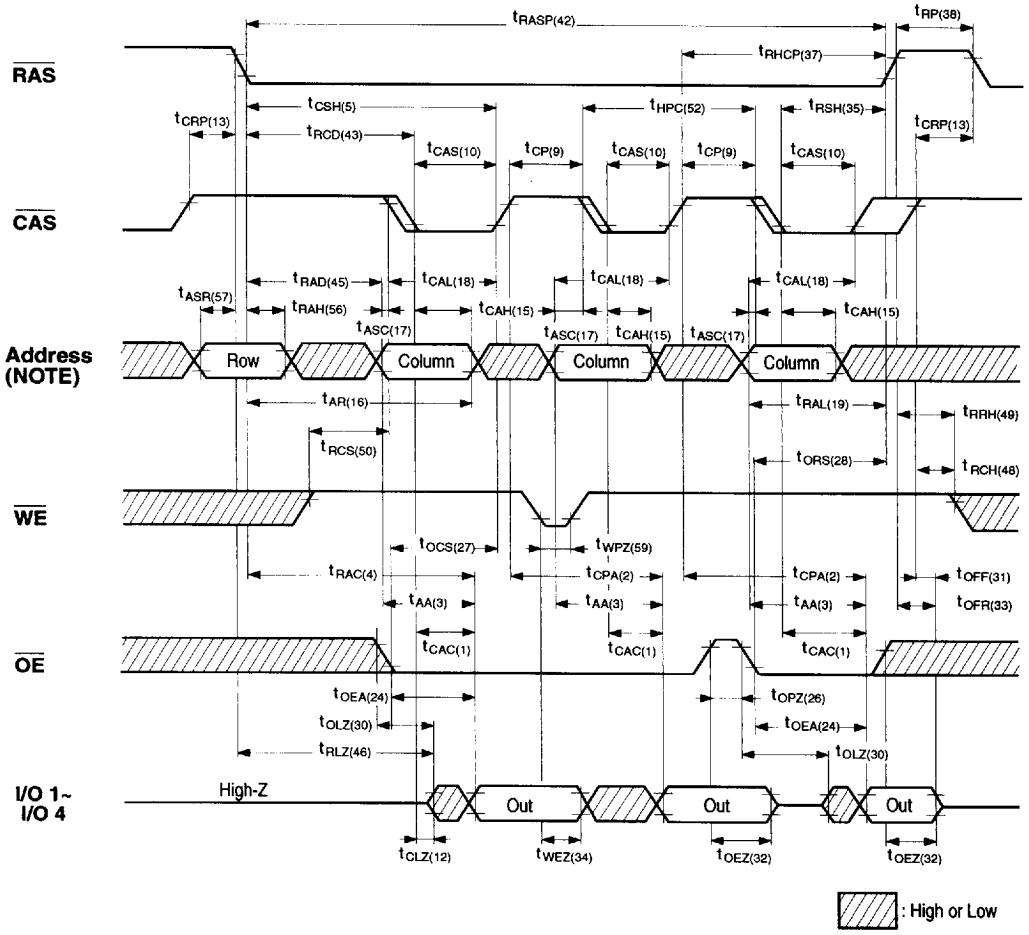
EDO (HYPER PAGE) MODE READ CYCLE



NOTE

Address A0 - A11 : NN5116405B
A0 - A10 : NN5117405B

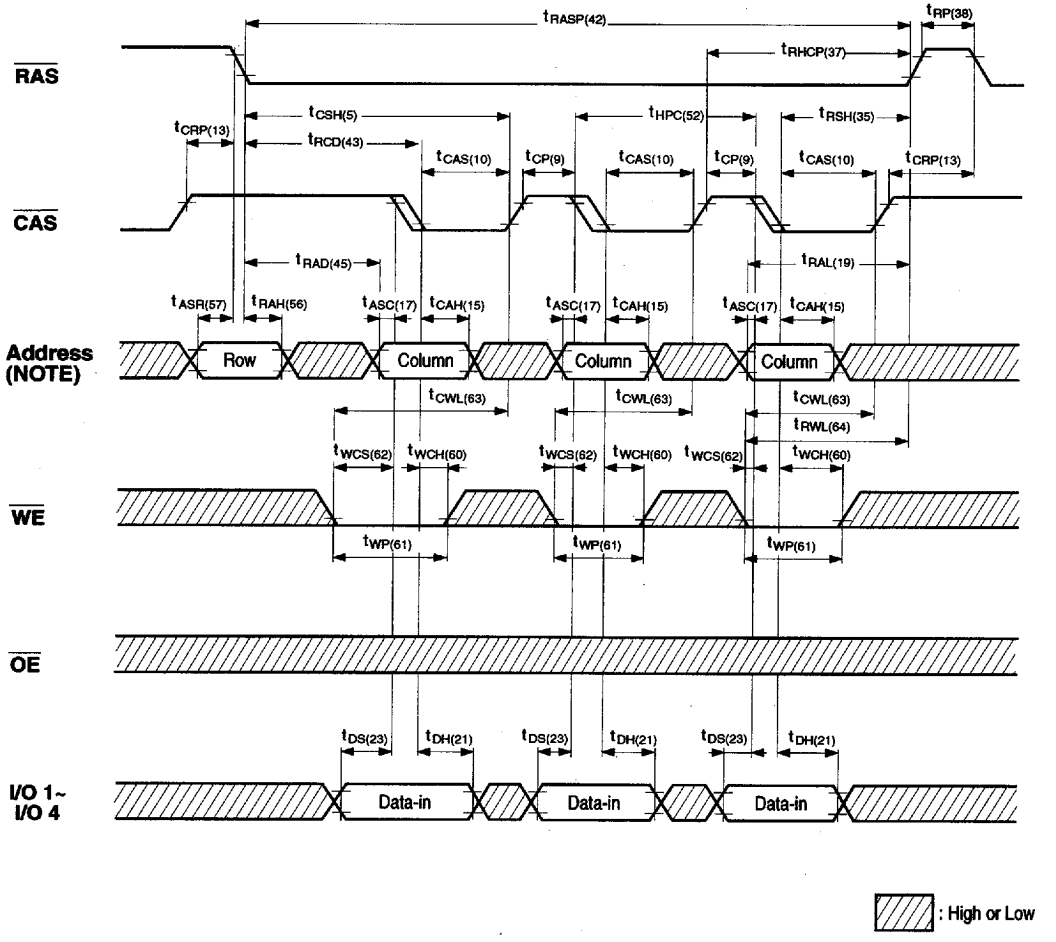
EDO (HYPER PAGE) MODE READ CYCLE ($\overline{OE}$ AND $\overline{WE}$ CONTROLLED OUTPUT)



NOTE

Address A0 - A11 : NN5116405B
A0 - A10 : NN5117405B

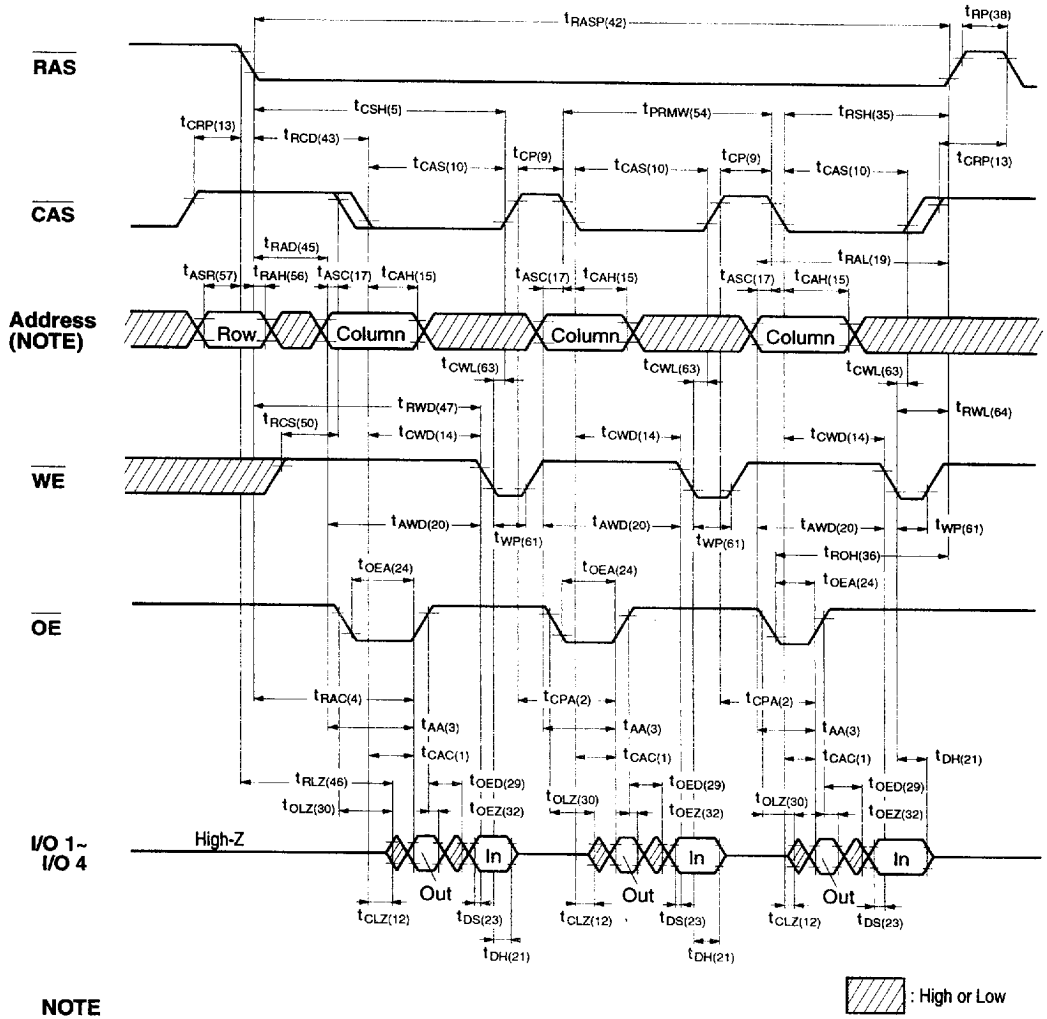
EDO (HYPER PAGE) MODE EARLY WRITE CYCLE



NOTE

Address A0 - A11 : NN5116405B
A0 - A10 : NN5117405B

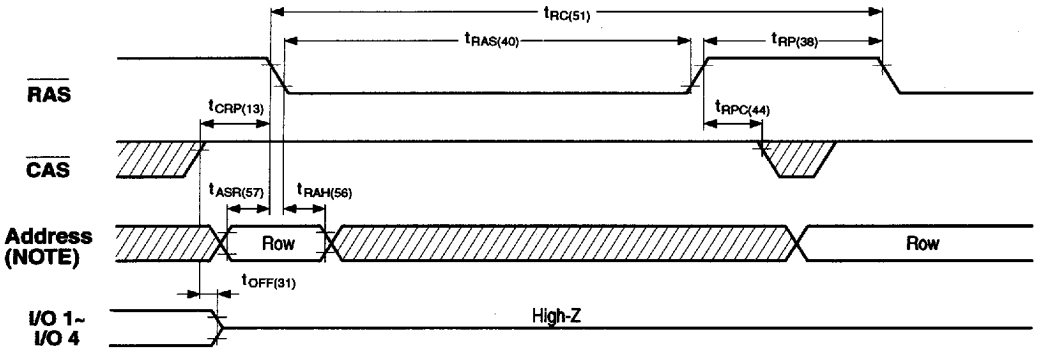
EDO (HYPER PAGE) MODE READ-MODIFY-WRITE CYCLE



NOTE

Address A0 - A11 : NN5116405B
A0 - A10 : NN5117405B

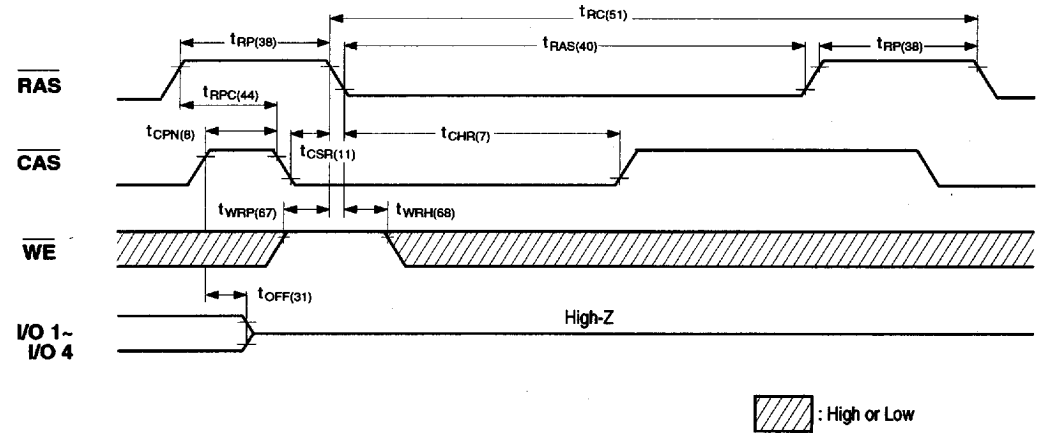
$\overline{RAS}$ ONLY REFRESH CYCLE



NOTE

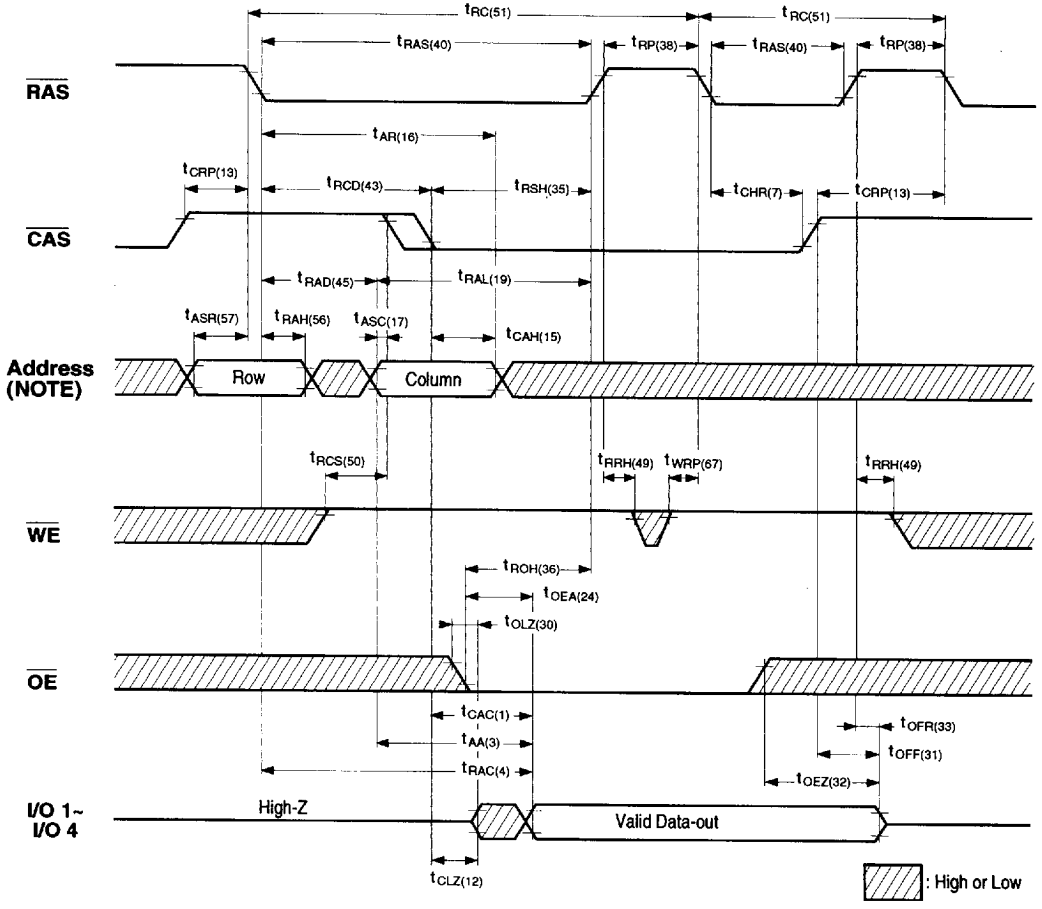
Address A0 - A11 : NN5116405B
A0 - A10 : NN5117405B

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: $\overline{OE}$, A0~A11 = Don't care.
$\overline{WE}$ must be high at the falling edge of $\overline{RAS}$ in order to prevent from entering test mode.

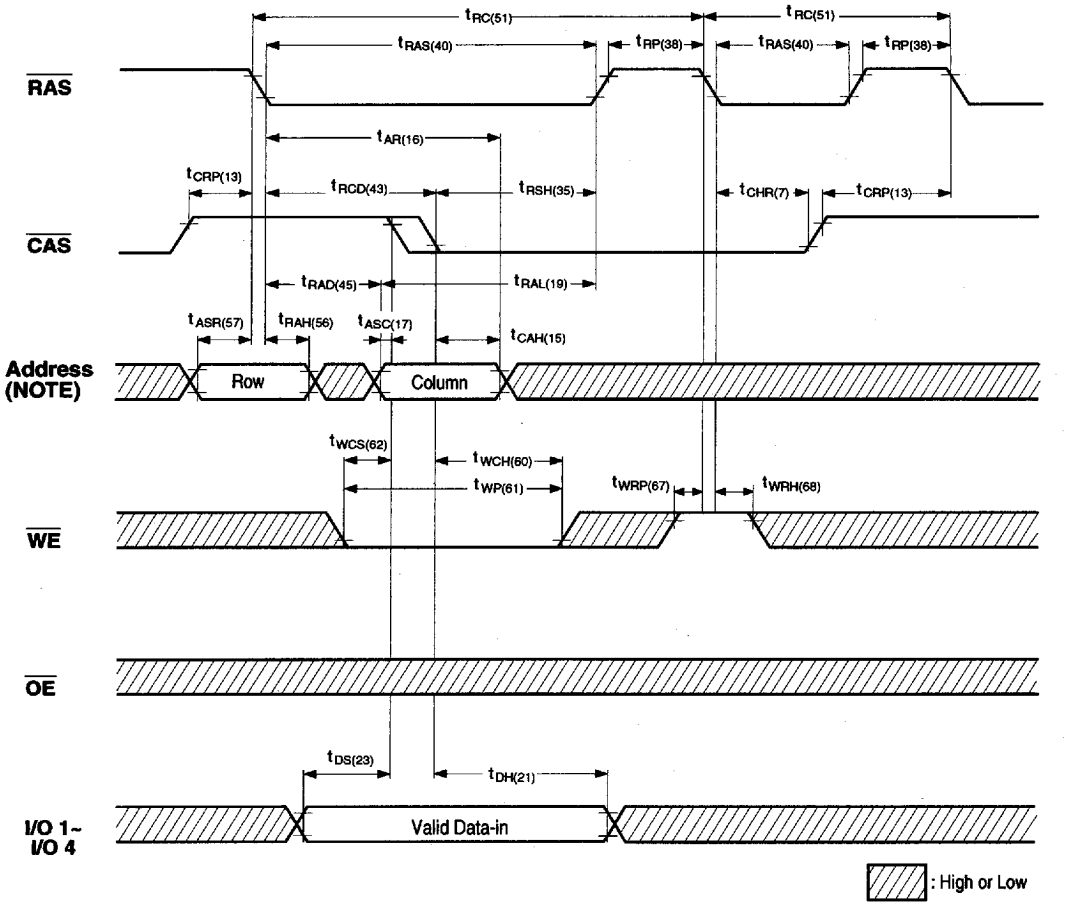
HIDDEN REFRESH CYCLE (READ)



NOTE

Address A0 - A11 : NN5116405B
A0 - A10 : NN5117405B

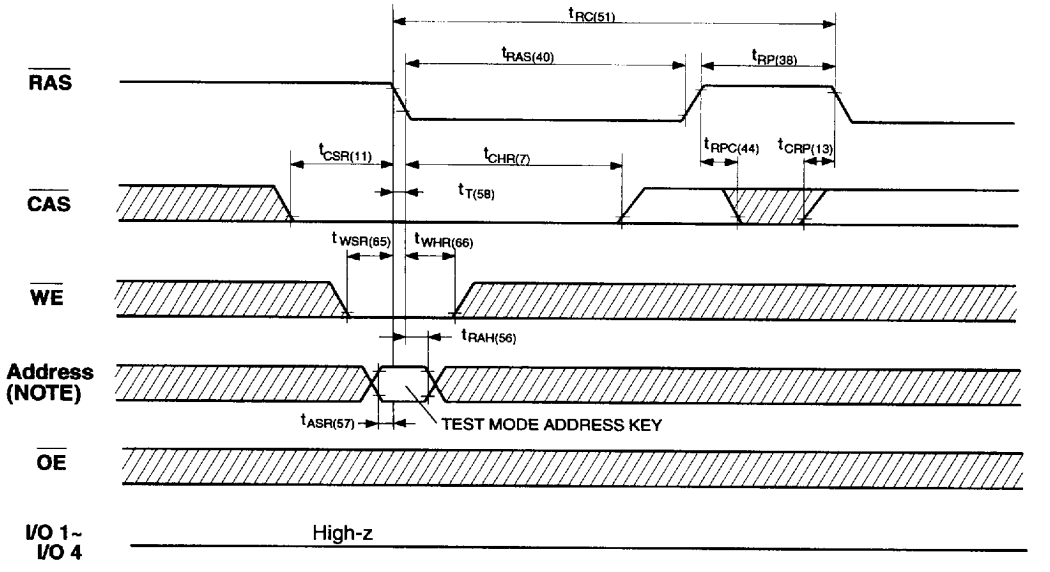
HIDDEN REFRESH CYCLE (EARLY WRITE)



NOTE

Address A0 - A11 : NN5116405B
A0 - A10 : NN5117405B

TEST MODE SET CYCLE ($\overline{WE}$, $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE)



NOTE :TEST MODE ADDRESS KEY
A5 and A6 must be "High".
A4 and A7 must be "Low".
All other address are "Don't care".

: High or Low

Address A0 - A11 : NN5116405B
A0 - A10 : NN5117405B

■ The NN5116405B / NN5117405B has a 16 bit parallel Test Mode Function for reducing test time. In the Test Mode, memory configuration is 1M x 16 bits and the Column address A0 and A1 address is ignored.

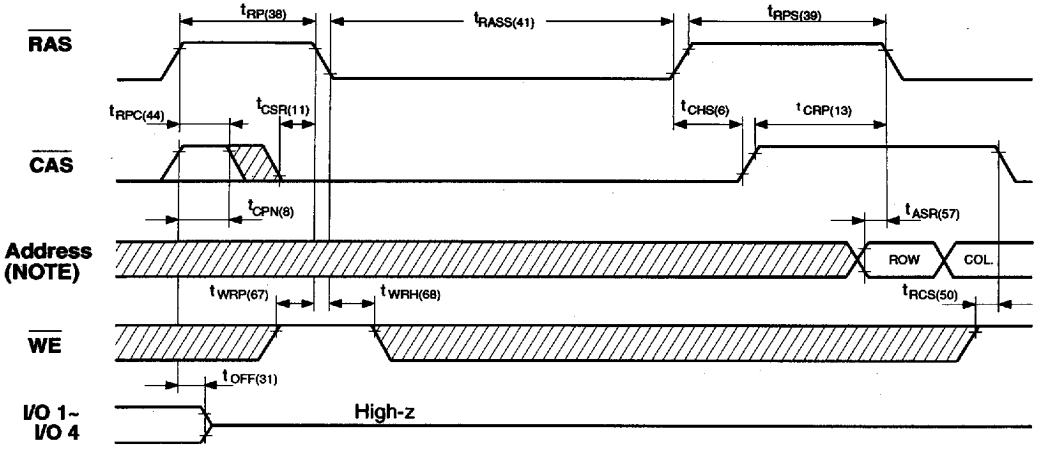
a. Entering the test mode:
The NN5116405B / NN5117405B test mode is entered by using the test mode set cycle ($\overline{WE}$,$\overline{CAS}$ before $\overline{RAS}$ cycle).

b. Read/Write operation in test mode:
For Write cycle, data input from each I/O (I/O1~I/O4) is written to 4 bit memory cells (total 16bits) at the same time.
During the read cycle, if the 4 bits of data are equal then a "1" is output from each I/O.
If there is a difference in the read data for a given 4 bit combination, a "0" will be output from that I/O.

c. Exiting the test mode:
The NN5116405B / NN5117405B will exit the test mode by either a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle width $\overline{WE}$ "high".

d. Refresh during test mode:
During test mode refresh must be executed by a normal Read cycle or a $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

SELF REFRESH MODE



NOTE

Address A0 - A11 : NN5116405B
A0 - A10 : NN5117405B

: High or Low

■ The NN5116405BL / NN5117405BL version has a Self Refresh Mode.

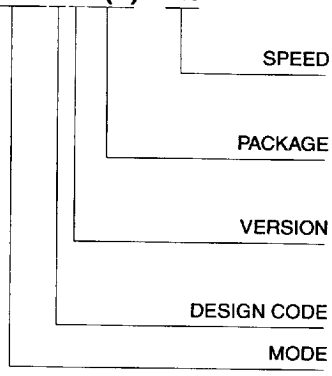
a. Entering the Self Refresh Mode:
The NN5116405BL / NN5117405BL Self Refresh Mode is entered by using $\overline{CAS}$ before $\overline{RAS}$ cycle with $\overline{WE}$ " high " and holding $\overline{RAS}$ and $\overline{CAS}$ signal " low " longer than 300μs.

b. Continuing the Self Refresh Mode:
The Self Refresh Mode is continued by holding $\overline{RAS}$ " low " after entering the Self Refresh Mode.
It does not depend on $\overline{CAS}$ being " high " or " low " after entering the Self Refresh Mode for to continue the Self Refresh Mode.

c. Exiting the Self Refresh Mode:
The NN5116405BL / NN5117405BL exits the Self Refresh Mode when the $\overline{RAS}$ signal is brought " high ".

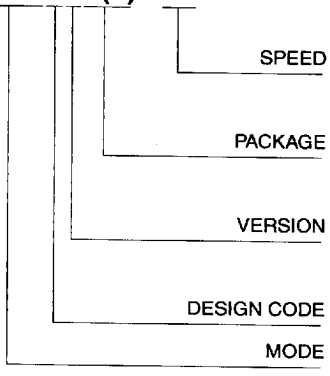
ORDERING INFORMATION

NN5116405BXX(X) - XX



SPEED	40	: 40ns
	50	: 50ns
	60	: 60ns
PACKAGE	J	: Plastic SOJ
	TT	: Plastic TSOP TYPE II
VERSION	BLANK:	Standard Version
	L	: Long Refresh Version 128ms Refresh
DESIGN CODE	B	
MODE	16405 :	EDO (Hyper Page) Mode 4M x 4 4,096 Refresh Cycle

NN5117405BXX(X) - XX



SPEED	40	: 50ns
	50	: 60ns
	60	: 70ns
PACKAGE	J	: Plastic SOJ
	TT	: Plastic TSOP TYPE II
VERSION	BLANK:	Standard Version
	L	: Long Refresh Version 128ms Refresh
DESIGN CODE	B	
MODE	17405 :	EDO (Hyper Page) Mode 4M x 4 2,048 Refresh Cycle