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DM54ALS273/DM74ALS273

Octal D-Type Edge-Triggered Flip-Flop with Clear

General Description

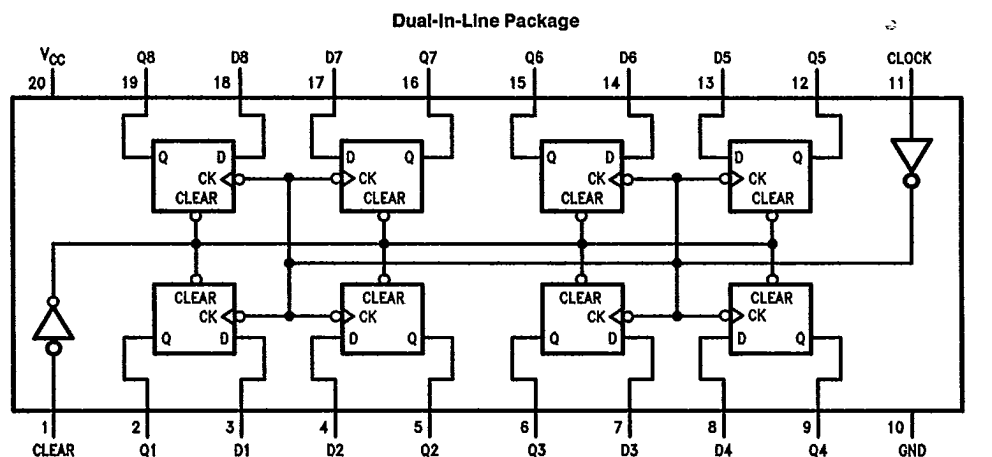
These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input.

Information at the D inputs meeting the setup requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Buffer-type outputs and improved AC offer significant advantage over 'LS273.
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with 'LS273.

Connection Diagram



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Order Number DM54ALS273J, DM74ALS273WM, DM74ALS273N or DM74ALS273SJ
See NS Package Number J20A, M20, M20D or N20A

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Absolute Maximum Ratings

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If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	-55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Typical θ_{JA}	
N Package	57.0°C/W
M Package	76.0°C/W

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	DM54ALS273			DM74ALS273			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			-1			-2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
f_{CLK}	Clock Frequency	0		30	0		35	MHz
$t_{W(CLK)}$	Width of Clock Pulse	High	16.5		14			ns
		Low	16.5		14			ns
t_W	Width of Clear Pulse	Low	10		10			ns
t_{SU}	Data Setup Time	10 $\uparrow$			10 $\uparrow$			ns
	Clear Inactive	15 $\uparrow$			15 $\uparrow$			
t_H	Data Hold Time	0 $\uparrow$			0 $\uparrow$			ns
T_A	Free Air Operating Temperature	-55		125	0		70	°C

The ($\uparrow$) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at $V_{CC} = 5V$, $T_A = 25^\circ C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18 mA$			-1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$	54ALS $I_{OH} = -1 mA$	2.4	3.2	V
			74ALS $I_{OH} = -2.6 mA$	2.4	3.3	V
		$I_{OH} = -400 \mu A$	54/74ALS	$V_{CC} - 2$		V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$	54/74ALS $I_{OL} = 12 mA$	0.25	0.4	V
			74ALS $I_{OL} = 24 mA$	0.35	0.5	V
I_I	Input Current @ Max. Input Voltage	$V_{CC} = 5.5V$, $V_{IH} = 7V$			0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$			20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$			-0.2	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_O = 2.25V$	-30		-112	mA
I_{CC}	Supply Current	$V_{CC} = 5.5V$	Outputs High	11	20	mA
		Outputs Open	Outputs Low	19	29	mA

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Switching Characteristics over recommended operating free air temperature range (Note 1).

Symbol	Parameter	Conditions	From	To	DM54ALS273		DM74ALS273		Units
					Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 4.5V$ to $5.5V$ $R_L = 500\Omega$ $C_L = 50 pF$			30		35		MHz
t_{PHL}	Propagation Delay Time High to Low Level Output		Clear	Any Q	4	21.5	4	18	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Any Q	2	16.5	2	12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Any Q	3	16.5	3	15	ns

Note 1: See Section 1 for test waveforms and output load.

Function Table (Each Flip-Flop)

Inputs			Output Q
Clear	Clock	D	
L	X	X	L
H	$\uparrow$	H	H
H	$\uparrow$	L	L
H	L	X	Q_0

L = Low State, H = High State, X = Don't Care

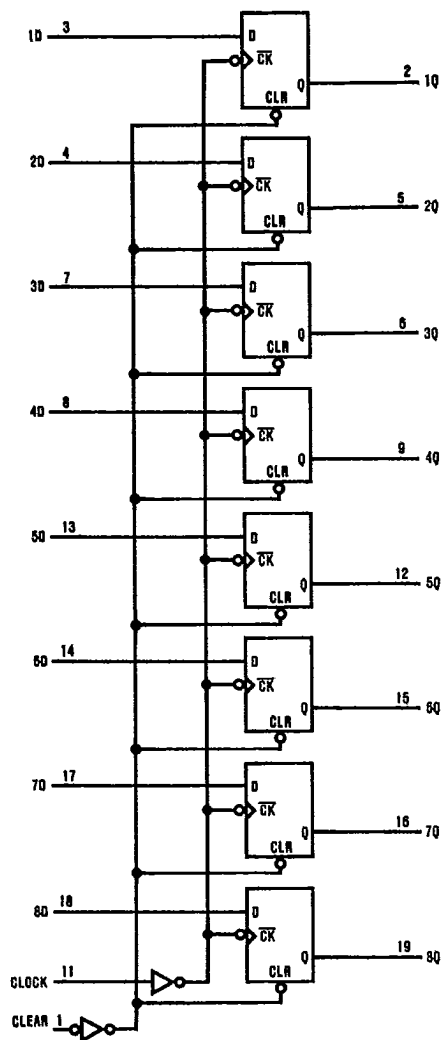
 $\uparrow$ = Positive Edge Transition, Q_0 = Previous Condition of Q

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Logic Diagram

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