

54VHC/74VHC373 • 54VHCT/74VHCT373 Octal D-Type Latch with TRI-STATE® Outputs

General Description

The VHC/VHCT373 is an advanced high speed CMOS octal D-type latch with TRI-STATE output fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. This 8-bit D-type latch is controlled by a latch enable input (LE) and an output enable input ($\overline{OE}$). The latches appear transparent to data when latch enable (LE) is HIGH. When LE is low, the data that meets the setup time is latched. When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

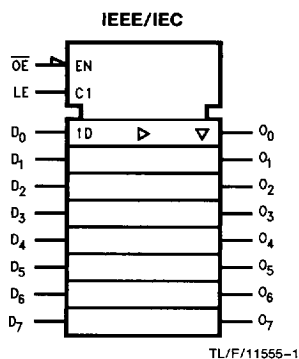
An input protection circuit ensures that 0V–7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

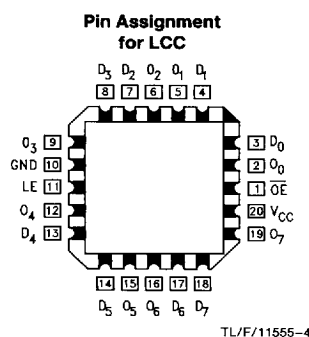
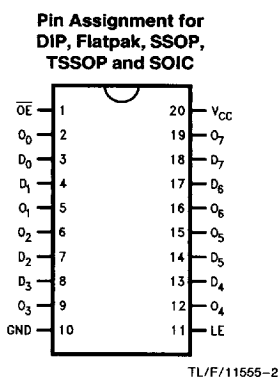
- High speed:
VHC $t_{PD} = 5.0$ ns (typ) @ $V_{CC} = 5V$
VHCT $t_{PD} = 5.1$ ns (typ) @ $V_{CC} = 5V$
- High Noise Immunity:
VHC $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min)
VHCT $V_{IH} = 2.0V$, $V_{IL} = 0.8V$
- Operating Voltage:
VHC V_{CC} (opr) = 2V ~ 5.5V
VHCT V_{CC} (opr) = 4.5V–5.5V
- Power Down Protection:
VHC Inputs Only
VHCT Inputs and Outputs
- Low Noise:
VHC $V_{OLP} = 0.6V$ (typ)
VHCT $V_{OLP} = 0.8V$ (typ)
- Low Power Dissipation:
 $I_{CC} = 4 \mu A$ (Max) @ $T_a = 25^\circ C$
- Balanced Propagation Delays: $t_{PLH} \approx t_{PHL}$
- Pin and Function Compatible with 74HC/HCT373

NOTE: MILITARY SPECIFICATIONS ARE PRELIMINARY

Logic Symbol



Connection Diagrams



Pin Names	Description
D ₀ –D ₇	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
Q ₀ –Q ₇	TRI-STATE Outputs

TRI-STATE® is a registered trademark of National Semiconductor Corporation

Functional Description

The VHC/VHCT373 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
LE	$\overline{OE}$	D_n	O_n
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = HIGH Voltage Level

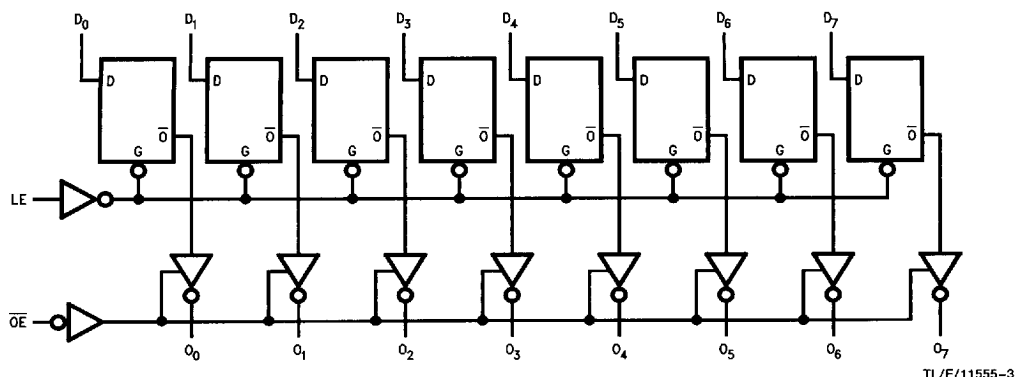
L = LOW Voltage Level

Z = High Impedance

X = Immaterial

O_0 = Previous O_0 before HIGH to Low transition of Latch Enable

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

TL/F/11555-3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Voltage (V_{IN})	-0.5V to +7.0V
DC Output Voltage (V_{OUT})	
VHC	-0.5V to $V_{CC} + 0.5V$
VHCT*	-0.5V to +7.0V
Input Diode Current (I_{IK})	-20 mA
Output Diode Current (VHC)	± 20 mA
(VHCT)	-20 mA
DC Output Current (I_{OUT})	± 25 mA
DC V_{CC} /GND Current (I_{CC})	± 75 mA
Storage Temperature (T_{STG})	-65°C to +150°C
Lead Temperature (T_L)	
(Soldering, 10 sec)	300°C

* $V_{OUT} > V_{CC}$ only if output is in H or Z state

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
VHC	2.0V to +5.5V
VHCT	4.5V to +5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	
54VHC/VHCT	-55°C to +125°C
74VHC/VHCT	-40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
$V_{CC} = 3.3V \pm 0.3V$ (VHC only)	0 ~ 100 ns/V
$V_{CC} = 5.0 \pm 0.5V$	0 ~ 20 ns/V

DC Characteristics for 'VHC Family Devices

Symbol	Parameter	V _{CC} (V)	74VHC			54VHC		74VHC		Units	Conditions	
			T _A = +25°C			T _A = −55°C to +125°C		T _A = −40°C to +85°C				
			Min	Typ	Max	Min	Max	Min	Max			
V _{IH}	High Level Input Voltage	2.0 3.0–5.5	1.50 0.7 V _{CC}			1.50 0.7 V _{CC}		1.50 0.7 V _{CC}		V		
V _{IL}	Low Level Input Voltage	2.0 3.0–5.5	0.50 0.3 V _{CC}			0.50 0.3 V _{CC}		0.50 0.3 V _{CC}		V		
V _{OH}	High Level Output Voltage	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V	V _{IN} = V _{IH} or V _{IL}	I _{OH} = −50 μA
		3.0 4.5	2.58 3.94			2.40 3.70		2.48 3.80		V	I _{OH} = −8 mA	I _{OH} = −4 mA
V _{OL}	Low Level Output Voltage	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 μA
		3.0 4.5			0.36 0.36		0.50 0.50		0.44 0.44	V	I _{OL} = 8 mA	I _{OL} = 4 mA
I _{OZ}	TRI-STATE Output Off-State Current	5.5	±0.25			±10.0		±2.5		μA	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	
I _{IN}	Input Leakage Current	0–5.5	±0.1			±1.0		±1.0		μA	V _{IN} = 5.5 or GND	
I _{CC}	Quiescent Supply Current	5.5	4.0			160.0		40.0		μA	V _{IN} = V _{CC} or GND	

DC Characteristics for 'VHC Family Devices

Symbol	Parameter	V _{CC} (V)	74VHC		54VHC		74VHC		Units	Conditions
			T _A = +25°C		T _A = −55°C to +125°C		T _A = −40°C to +85°C			
			Typ	Limits	Min	Max	Limits			
**V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	5.0	0.6	0.9					V	C _L = 50 pF
**V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	5.0	−0.6	−0.9					V	C _L = 50 pF
**V _{IHD}	Minimum High Level Dynamic Input Voltage	5.0		3.5					V	C _L = 50 pF
**V _{ILD}	Maximum Low Level Dynamic Input Voltage	5.0		1.5					V	C _L = 50 pF

**Parameter guaranteed by design

DC Characteristics for 'VHCT Family Devices

Symbol	Parameter	V _{CC} (V)	74VHCT			54VHCT		74VHCT		Units	Conditions	
			T _A = +25°C			T _A = -55°C to +125°C		T _A = -40°C to +85°C				
			Min	Typ	Max	Min	Max	Min	Max			
V _{IH}	High Level Input Voltage	4.5 5.5	2.0 2.0					2.0 2.0		V		
V _{IL}	Low Level Input Voltage	4.5 5.5			0.8 0.8				0.8 0.8	V		
V _{OH}	High Level Output Voltage	4.5	3.15	3.65				3.15		V	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50 μA
		4.5	2.5					2.4		V		I _{OH} = -8 mA
V _{OL}	Low Level Output Voltage	4.5		0.0	0.1				0.1	V	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 μA
		4.5			0.36				0.44	V		I _{OL} = 8 mA
I _{OZ}	TRI-STATE Output Off-State Current	5.5			±0.25				±2.5	μA	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	
I _{IN}	Input Leakage Current	0-5.5			±0.1				±1.0	μA	V _{IN} = 5.5V or GND	
I _{CC}	Quiescent Supply Current	5.5			4.0				40.0	μA	V _{IN} = V _{CC} or GND	
I _{CCT}	Maximum I _{CC} /Input	5.5			1.35				1.50	mA	V _{IN} = 3.4V Other Inputs = V _{CC} or GND	
I _{OPP}	Output Leakage Current (Power Down State)	0.0			+0.5				+0.5	μA	V _{OUT} = 5.5V	

DC Characteristics for 'VHCT Family Devices

Symbol	Parameter	V _{CC} (V)	74VHCT		54VHCT	74VHCT	Units	Conditions
			T _A = +25°C		T _A = -55°C to +125°C	T _A = -40°C to +85°C		
			Typ	Limits	Limits	Limits		
**V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	5.0	0.8	1.2			V	C _L = 50 pF
**V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	5.0	-0.8	-1.2			V	C _L = 50 pF
**V _{IHD}	Minimum High Level Dynamic Input Voltage	5.0		2.0			V	C _L = 50 pF
**V _{ILD}	Maximum Low Level Dynamic Input Voltage	5.0		0.8			V	C _L = 50 pF

**Parameter guaranteed by design.

AC Electrical Characteristics for 'VHC Family Devices

Symbol	Parameter	V _{CC} (V)	74VHC			54VHC		74VHC		Units	Conditions	
			T _A = +25°C			T _A = −55°C to +125°C		T _A = −40°C to +85°C				
			Min	Typ	Max	Min	Max	Min	Max			
t _{PLH} t _{PHL}	Propagation Delay Time (LE to O _N)	3.3 ± 0.3	7.0		11.0			1.0	13.0	ns		C _L = 15 pF
			9.5		14.5	1.0		16.5				C _L = 50 pF
		5.0 ± 0.5	4.9		7.2			1.0	8.5	ns		C _L = 15 pF
			6.4		9.2			1.0	10.5			C _L = 50 pF
t _{PLH} t _{PHL}	Propagation Delay Time (D to O _N)	3.3 ± 0.3	7.3		11.4			1.0	13.5	ns		C _L = 15 pF
			9.8		14.9	1.0		17.0				C _L = 50 pF
		5.0 ± 0.5	5.0		7.2			1.0	8.5	ns		C _L = 15 pF
			6.5		9.2			1.0	10.5			C _L = 50 pF
t _{pZL} t _{pZH}	TRI-STATE Output Enable Time	3.3 ± 0.3	7.3		11.4			1.0	13.5	ns	R _L = 1 kΩ	C _L = 15 pF
			9.8		14.9			1.0	17.0			C _L = 50 pF
		5.0 ± 0.5	5.5		8.1			1.0	9.5	ns		C _L = 15 pF
			7.0		10.1			1.0	11.5			C _L = 50 pF
t _{PLZ} t _{PHZ}	TRI-STATE Output Disable Time	3.3 ± 0.3	9.5		13.2			1.0	15.0	ns	R _L = 1 kΩ	C _L = 50 pF
		5.0 ± 0.5	6.5		9.2			1.0	10.5			C _L = 50 pF
t _{OSLH} t _{OSHL}	Output to Output Skew	3.3 ± 0.3			1.5			1.5		ns	(Note 1)	C _L = 50 pF
		5.0 ± 0.5			1.0			1.0				C _L = 50 pF
C _{IN}	Input Capacitance		4		10			10		pF	V _{CC} = Open	
C _{OUT}	Output Capacitance		6							pF	V _{CC} = 5.0V	
C _{PD}	Power Dissipation Capacitance		27							pF	(Note 2)	

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLH \max} - t_{PLH \min}|$; $t_{OSHL} = |t_{PHL \max} - t_{PHL \min}|$

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per Latch). The total C_{PD} when n pcs. of the Latch operates can be calculated by the equation: $C_{PD}(\text{total}) = 14 + 13n$

AC Operating Requirements for 'VHC Family Devices

Symbol	Parameter	V _{CC} (V)	74VHC			54VHC		74VHC		Units	Conditions
			T _A = +25°C			T _A = −55°C to +125°C		T _A = −40°C to +85°C			
			Min	Typ	Max	Min	Max	Min	Max		
t _{W(H)}	Minimum Pulse Width (LE)	3.3 ± 0.3	5.0					5.0		ns	
		5.0 ± 0.5	5.0					5.0			
t _S	Minimum Set-Up Time	3.3 ± 0.3	4.0					4.0		ns	
		5.0 ± 0.5	4.0					4.0			
t _H	Minimum Hold Time	3.3 ± 0.3	1.0					1.0		ns	
		5.0 ± 0.5	1.0					1.0			

AC Electrical Characteristics for 'VHCT Family Devices

Symbol	Parameter	V _{CC} (V)	74VHCT			54VHCT		74VHCT		Units	Conditions	
			T _A = +25°C			T _A = -55°C to +125°C		T _A = -40°C to +85°C				
			Min	Typ	Max	Min	Max	Min	Max			
t _{PLH} t _{PHL}	Propagation Delay Time (LE to O _n)	5.0 ± 0.5	7.7	12.3			1.0	13.5	ns		C _L = 15 pF	
			8.5	13.3			1.0	14.5			C _L = 50 pF	
t _{PLH} t _{PHL}	Propagation Delay Time (D to O _n)	5.0 ± 0.5	5.1	8.5			1.0	9.5	ns		C _L = 15 pF	
			5.9	9.5			1.0	10.5			C _L = 50 pF	
t _{PZL} t _{PZH}	TRI-STATE Output Enable Time	5.0 ± 0.5	6.3	10.9			1.0	12.5	ns	R _L = 1 kΩ	C _L = 15 pF	
			7.1	11.9			1.0	13.5			C _L = 50 pF	
t _{PLZ} t _{PHZ}	TRI-STATE Output Disable Time	5.0 ± 0.5	6.8	11.2			1.0	12.0	ns	R _L = 1 kΩ	C _L = 50 pF	
t _{OSLH} t _{OSHL}	Output to Output Skew	5.0 ± 0.5		1.0			1.0		ns	(Note 1)		
C _{IN}	Input Capacitance		4	10			10		pF	V _{CC} = Open		
C _{OUT}	Output Capacitance		9						pF	V _{CC} = 5.0V		
C _{PD}	Power Dissipation Capacitance		27						pF	(Note 2)		

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLH \max} - t_{PLH \min}|$; $t_{OSHL} = |t_{PHL \max} - t_{PHL \min}|$

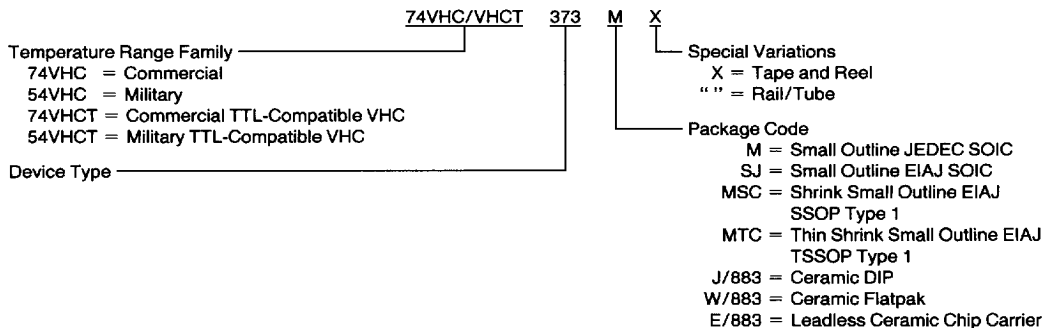
Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per F/F)

AC Operating Requirements for 'VHCT Family Devices

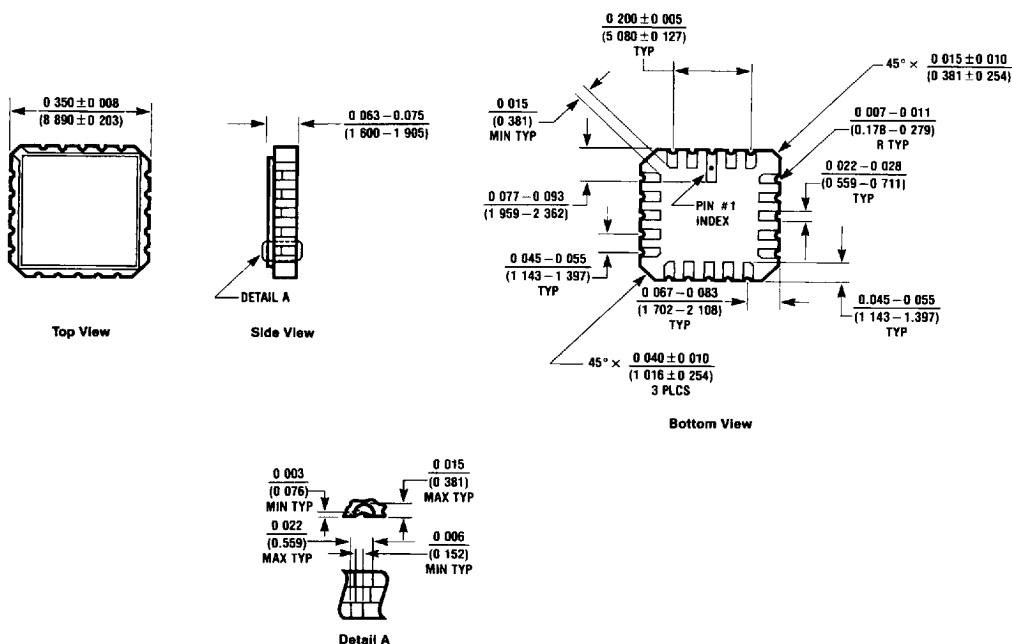
Symbol	Parameter	V _{CC} (V)	74VHCT			54VHCT		74VHCT		Units	Conditions
			T _A = +25°C			T _A = −55°C to +125°C		T _A = −40°C to +85°C			
			Min	Typ	Max	Min	Max	Min	Max		
t _{W(H)}	Minimum Pulse Width (LE)	5.0 ± 0.5	6.5					6.5		ns	
t _S	Minimum Set-Up Time	5.0 ± 0.5	1.5					1.5		ns	
t _H	Minimum Hold Time	5.0 ± 0.5	3.5					3.5		ns	

Ordering Information

The device number is used to form part of a simplified purchasing code, where the package type and temperature range are defined as follows:



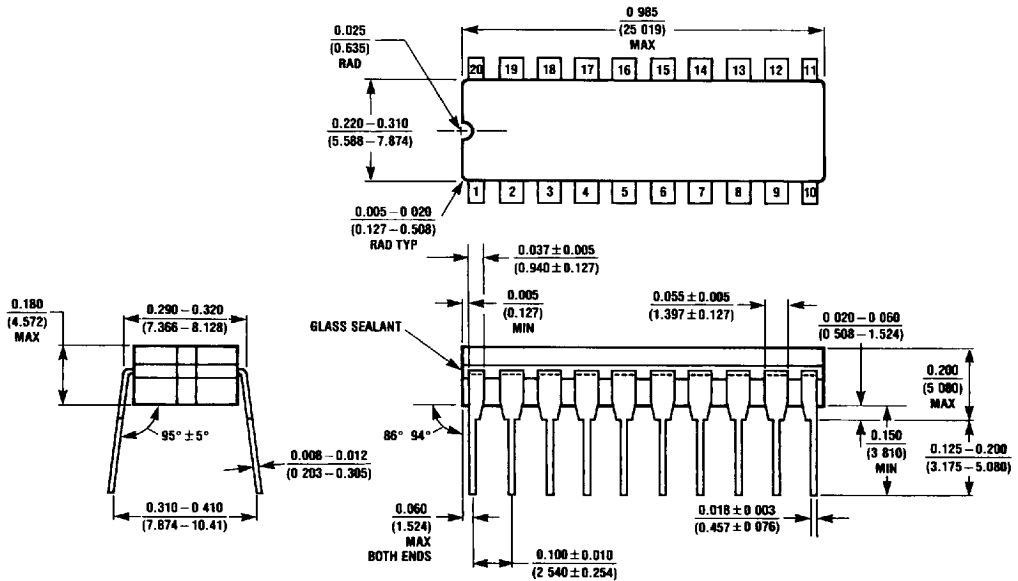
Physical Dimensions inches (millimeters)



20-Lead Ceramic Leadless Chip Carrier, Type C (L)
Order Number 54VHC373E/883 or 54VHCT373E/883
NS Package Number E20A

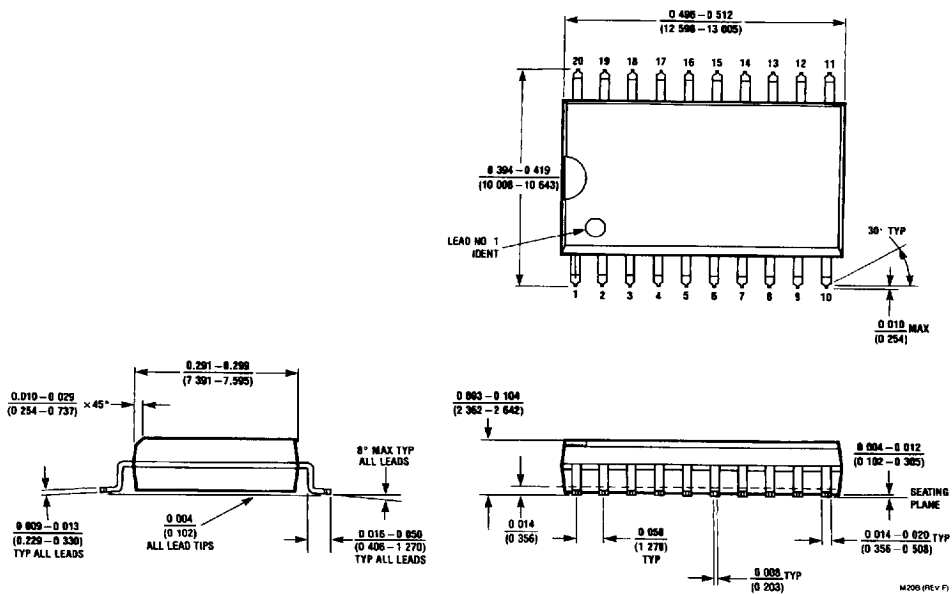
E20A (REV D)

Physical Dimensions inches (millimeters) (Continued)



J20A (REV M)

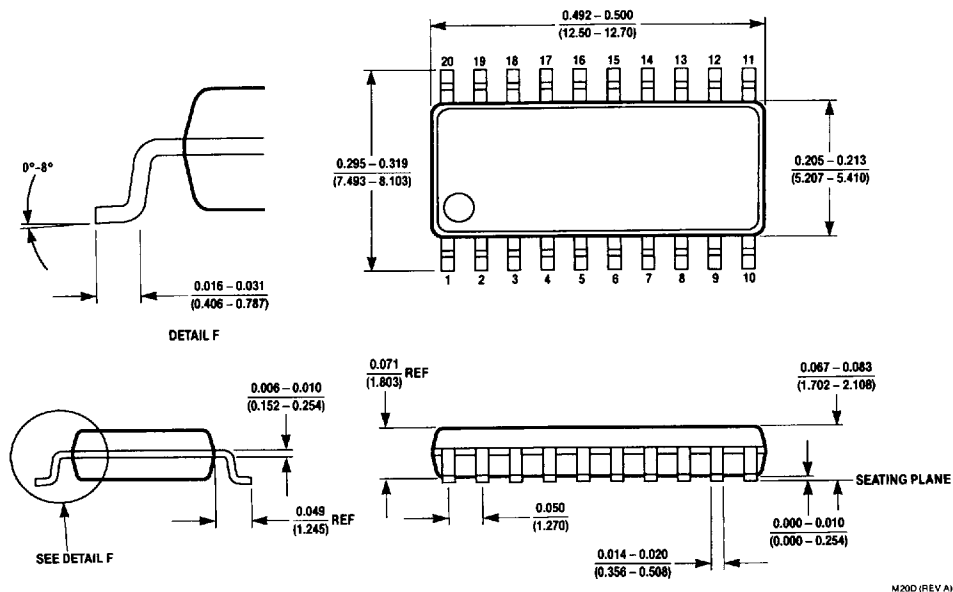
20-Lead Ceramic Dual-In-Line Package (D)
Order Number 54VHC373J/883 or 54VHCT373J/883
NS Package Number J20A



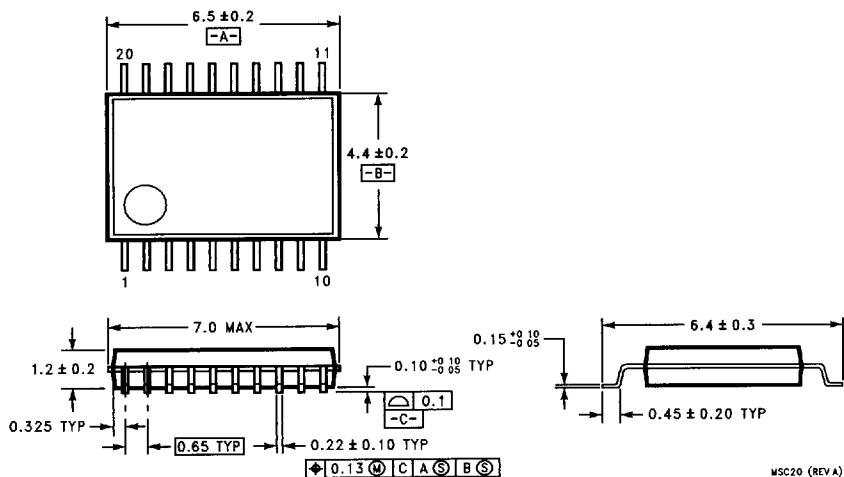
M20B (REV F)

20-Lead Small Outline Integrated Circuit—JEDEC SOIC (M)
Order Number 74VHC373M, 74VHC373MX, 74VHCT373M or 74VHCT373MX
NS Package Number M20B

Physical Dimensions inches (millimeters) (Continued)

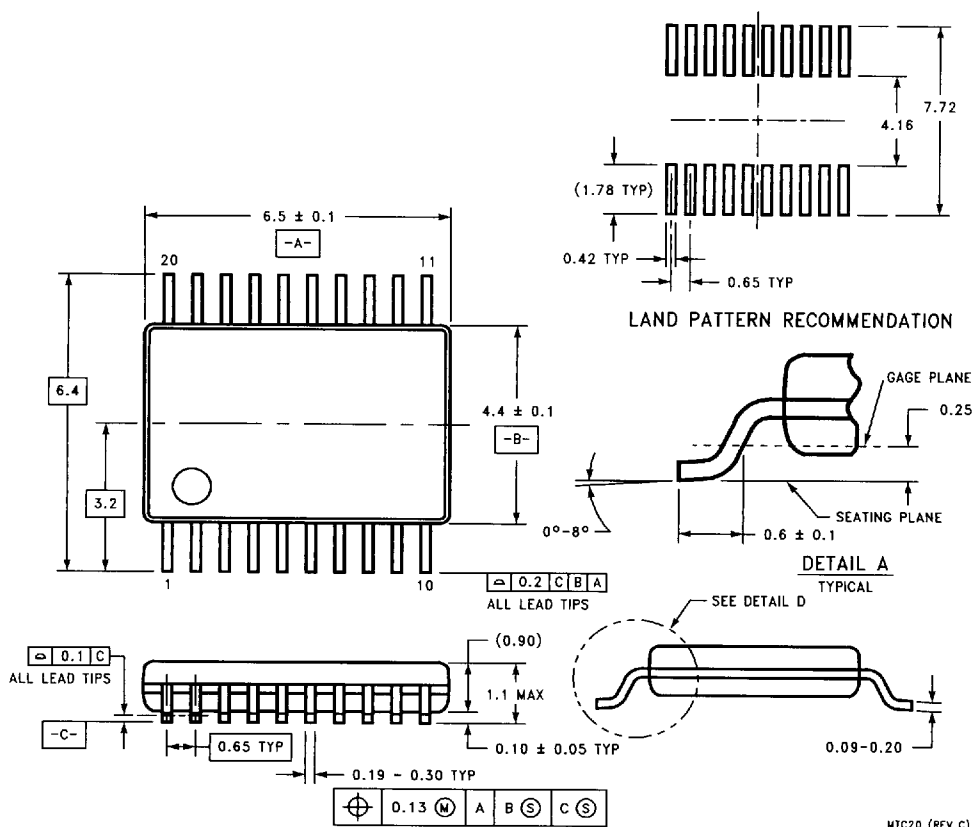


20-Lead Plastic EIAJ SOIC (SJ)
Order Number 74VHC373SJ, 74VHC373SJX, 74VHCT373SJ or 74VHCT373SJX
NS Package Number M20D



20-Lead Shrink Small Outline EIAJ SSOP Type I (MSC)
Order Number 74VHC373MSCX or 74VHCT373MSCX
NS Package Number MSC20

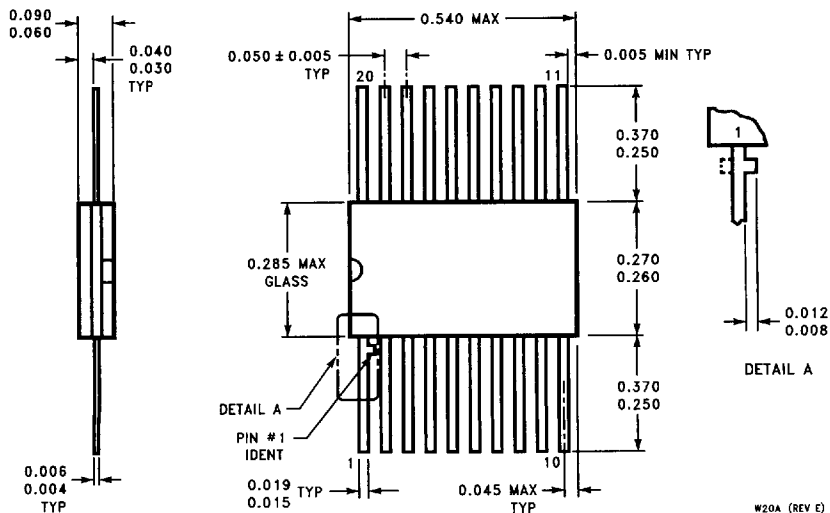
Physical Dimensions inches (millimeters) (Continued)



MTC20 (REV C)

Physical Dimensions inches (millimeters) (Continued)

Lit. # 119000-002



20-Lead Cerpack
Order Number 54VHC373W/883 or 54VHCT373W/883
NS Package Number W20A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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