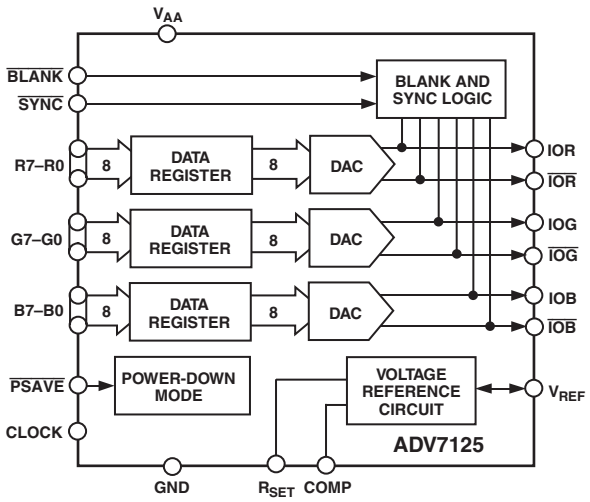
CMOS, 330 MHz Triple 8-Bit High Speed Video DAC

ADV7125

FEATURES
330 MSPS Throughput Rate
Triple 8-Bit DACs
RS-343A/RS-170 Compatible Output
Complementary Outputs
DAC Output Current Range 2 to 26 mA
TTL Compatible Inputs
Internal Reference (1.23 V)
Single-Supply 5 V/3.3 V Operation
48-Lead LQFP Package
Low Power Dissipation (30 mW Min @ 3 V)
Low Power Standby Mode (6 mW Typ @ 3 V)
Industrial Temperature Range (–40°C to +85°C)

APPLICATIONS
Digital Video Systems
High Resolution Color Graphics
Digital Radio Modulation
Image Processing
Instrumentation
Video Signal Reconstruction

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADV®7125 is a triple high speed, digital-to-analog converter on a single monolithic chip. It consists of three high speed, 8-bit video DACs with complementary outputs, a standard TTL input interface, and a high impedance, analog output current source.

The ADV7125 has three separate 8-bit-wide input ports. A single 5 V/3.3 V power supply and clock are all that are required to make the part functional. The ADV7125 has additional video control signals, composite $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$, as well as a power-save mode.

The ADV7125 is fabricated in a 5 V CMOS process. Its monolithic CMOS construction ensures greater functionality with lower power dissipation. The ADV7125 is available in a 48-lead LQFP package.

PRODUCT HIGHLIGHTS

1. 330 MSPS (3.3 V only) throughput
2. Guaranteed monotonic to eight bits
3. Compatible with a wide variety of high resolution color graphics systems, including RS-343A and RS-170

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 **www.analog.com**
Fax: 781/326-8703

ADV7125–SPECIFICATIONS

5 V ELECTRICAL CHARACTERISTICS

(V_{AA} = 5 V ± 5%, V_{REF} = 1.235 V, R_{SET} = 560 Ω, C_L = 10 pF. All specifications T_{MIN} to T_{MAX}[1], unless otherwise noted, $T_{J\,MAX}$ = 110°C.)

Parameter	Min	Typ	Max	Unit	Test Conditions[1]
STATIC PERFORMANCE					
Resolution (Each DAC)	8			Bits	
Integral Nonlinearity (BSL)	–1	±0.4	+1	LSB	
Differential Nonlinearity	–1	±0.25	+1	LSB	Guaranteed Monotonic
DIGITAL AND CONTROL INPUTS					
Input High Voltage, V_{IH}	2			V	
Input Low Voltage, V_{IL}			0.8	V	
Input Current, I_{IN}	–1		+1	μA	V_{IN} = 0.0 V or V_{DD}
PSAVE Pull-Up Current		20		μA	
Input Capacitance, C_{IN}		10		pF	
ANALOG OUTPUTS					
Output Current	2.0		26.5	mA	Green DAC, Sync = High
Output Current	2.0		18.5	mA	R/G/B DAC, Sync = Low
DAC-to-DAC Matching		1.0	5	%	
Output Compliance Range, V_{OC}	0		1.4	V	
Output Impedance, R_{OUT}		100		kΩ	
Output Capacitance, C_{OUT}		10		pF	I_{OUT} = 0 mA
Offset Error	–0.025		+0.025	% FSR	Tested with DAC Output = 0 V
Gain Error[2]	–5.0		+5.0	% FSR	FSR = 18.62 mA
VOLTAGE REFERENCE (Ext. and Int.)					
Reference Range, V_{REF}	1.12	1.235	1.35	V	
POWER DISSIPATION					
Digital Supply Current[3]		3.4	9	mA	f_{CLK} = 50 MHz
Digital Supply Current[3]		10.5	15	mA	f_{CLK} = 140 MHz
Digital Supply Current[3]		18	25	mA	f_{CLK} = 240 MHz
Analog Supply Current		67	72	mA	R_{SET} = 530 Ω
Analog Supply Current		8		mA	R_{SET} = 4933 Ω
Standby Supply Current[4]		2.1	5.0	mA	PSAVE = Low, Digital, and Control Inputs at V_{DD}
Power Supply Rejection Ratio		0.1	0.5	%/%	

NOTES

[1]Temperature range T_{MIN} to T_{MAX}: –40°C to +85°C at 50 MHz and 140 MHz, 0°C to +70°C at 240 MHz and 330 MHz.

[2]Gain error = (Measured (FSC)/Ideal (FSC) –1) × 100), where Ideal = $V_{REF}/R_{SET} \times K \times (FFH) \times 4$ and K = 7.9896.

[3]Digital supply is measured with continuous clock with data input corresponding to a ramp pattern and with an input level at 0 V and V_{DD}.

[4]These max/min specifications are guaranteed by characterization in the 4.75 V to 5.25 V range.

Specifications subject to change without notice.

3.3 V ELECTRICAL CHARACTERISTICS[1]

(V_{AA} = 3.0 V to 3.6 V, V_{REF} = 1.235 V, R_{SET} = 560 Ω, C_L = 10 pF. All specifications T_{MIN} to T_{MAX}[2], unless otherwise noted, $T_{J\,MAX}$ = 110°C.)

Parameter	Min	Typ	Max	Unit	Test Conditions[2]
STATIC PERFORMANCE					
Resolution (Each DAC)			8	Bits	R_{SET} = 680 Ω
Integral Nonlinearity (BSL)	–1	±0.5	+1	LSB	R_{SET} = 680 Ω
Differential Nonlinearity	–1	±0.25	+1	LSB	R_{SET} = 680 Ω
DIGITAL AND CONTROL INPUTS					
Input High Voltage, V_{IH}	2.0			V	
Input Low Voltage, V_{IL}		0.8		V	
Input Current, I_{IN}	–1		+1	μA	V_{IN} = 0.0 V or V_{DD}
PSAVE Pull-Up Current		20		μA	
Input Capacitance, C_{IN}		10		pF	
ANALOG OUTPUTS					
Output Current	2.0		26.5	mA	Green DAC, Sync = High
Output Current	2.0		18.5	mA	R/G/B DAC, Sync = Low
DAC-to-DAC Matching		1.0		%	
Output Compliance Range, V_{OC}	0		1.4	V	
Output Impedance, R_{OUT}		70		kΩ	
Output Capacitance, C_{OUT}		10		pF	
Offset Error		0	0	% FSR	Tested with DAC Output = 0 V
Gain Error[3]		0		% FSR	FSR = 18.62 mA
VOLTAGE REFERENCE (Ext.)					
Reference Range, V_{REF}	1.12	1.235	1.35	V	
VOLTAGE REFERENCE (Int.)					
Reference Range, V_{REF}		1.235		V	
POWER DISSIPATION					
Digital Supply Current[4]		2.2	5.0	mA	f_{CLK} = 50 MHz
Digital Supply Current[4]		6.5	12.0	mA	f_{CLK} = 140 MHz
Digital Supply Current[4]		11	15	mA	f_{CLK} = 240 MHz
Digital Supply Current[4]		16		mA	f_{CLK} = 330 MHz
Analog Supply Current		67	72	mA	R_{SET} = 560 Ω
Analog Supply Current		8		mA	R_{SET} = 4933 Ω
Standby Supply Current		2.1	5.0	mA	PSAVE = Low, Digital, and Control Inputs at V_{DD}
Power Supply Rejection Ratio		0.1	0.5	%/%	

NOTES

[1]These max/min specifications are guaranteed by characterization in the 3.0 V to 3.6 V range.

[2]Temperature range T_{MIN} to T_{MAX}: –40°C to +85°C at 50 MHz and 140 MHz, 0°C to +70°C at 240 MHz and 330 MHz.

[3]Gain error = (Measured (FSC)/Ideal (FSC) –1) × 100), where Ideal = $V_{REF}/R_{SET} \times K \times (FFH) \times 4$ and K = 7.9896.

[4]Digital supply is measured with continuous clock with data input corresponding to a ramp pattern and with an input level at 0 V and V_{DD}.

Specifications subject to change without notice.

5 V TIMING SPECIFICATIONS[1] (V_{AA} = 5 V ± 5%[2], V_{REF} = 1.235 V, R_{SET} = 560 Ω, C_L = 10 pF. All specifications T_{MIN} to T_{MAX}[3], unless otherwise noted, $T_{J\ MAX}$ = 110°C.)

Parameter	Min	Typ	Max	Unit	Condition
ANALOG OUTPUTS					
Analog Output Delay, t_6		5.5		ns	
Analog Output Rise/Fall Time, t_7[4]		1.0		ns	
Analog Output Transition Time, t_8[5]		15		ns	
Analog Output Skew, t_9[6]		1	2	ns	
CLOCK CONTROL					
f_{CLK}[7]	0.5		50	MHz	50 MHz Grade
f_{CLK}[7]	0.5		140	MHz	140 MHz Grade
f_{CLK}[7]	0.5		240	MHz	240 MHz Grade
Data and Control Setup, t_1[6]	0.5			ns	
Data and Control Hold, t_2[6]	1.5			ns	
Clock Period, t_3	4.17			ns	
Clock Pulsewidth High, t_4[6]	1.875			ns	f_{CLK_MAX} = 240 MHz
Clock Pulsewidth Low, t_5[6]	1.875			ns	f_{CLK_MAX} = 240 MHz
Clock Pulsewidth High, t_4[6]	2.85			ns	f_{CLK_MAX} = 140 MHz
Clock Pulsewidth Low, t_5[6]	2.85			ns	f_{CLK_MAX} = 140 MHz
Clock Pulsewidth High, t_4	8.0			ns	f_{CLK_MAX} = 50 MHz
Clock Pulsewidth Low, t_5	8.0			ns	f_{CLK_MAX} = 50 MHz
Pipeline Delay, t_{PD}[6]	1.0	1.0	1.0	Clock Cycles	
PSAVE Up Time, t_{10}[6]		2	10	ns	

NOTES
[1]Timing specifications are measured with input levels of 3.0 V (V_{IH}) and 0 V (V_{IL}) for both 5 V and 3.3 V supplies.
[2]These maximum and minimum specifications are guaranteed over this range.
[3]Temperature range T_{MIN} to T_{MAX}: –40°C to +85°C at 50 MHz and 140 MHz, 0°C to +70°C at 240 MHz.
[4]Rise time was measured from the 10% to 90% point of zero to full-scale transition, fall time from the 90% to 10% point of a full-scale transition.
[5]Measured from 50% point of full-scale transition to 2% of final value.
[6]Guaranteed by characterization.
[7]f_{CLK} max specification production tested at 125 MHz and 5 V. Limits specified here are guaranteed by characterization.

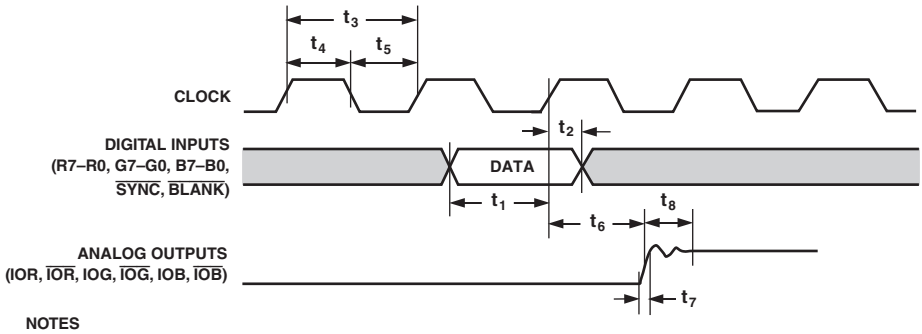
Specifications subject to change without notice.

3.3 V TIMING SPECIFICATIONS[1] (V_{AA} = 3.0 V to 3.6 V[2], V_{REF} = 1.235 V, R_{SET} = 560 Ω, C_L = 10 pF. All specifications T_{MIN} to T_{MAX}[3], unless otherwise noted, $T_{J\ MAX}$ = 110°C.)

Parameter	Min	Typ	Max	Unit	Condition
ANALOG OUTPUTS					
Analog Output Delay, t_6		7.5		ns	
Analog Output Rise/Fall Time, t_7[4]		1.0		ns	
Analog Output Transition Time, t_8[5]		15		ns	
Analog Output Skew, t_9[6]		1	2	ns	
CLOCK CONTROL					
f_{CLK}[7]			50	MHz	50 MHz Grade
f_{CLK}[7]			140	MHz	140 MHz Grade
f_{CLK}[7]			240	MHz	240 MHz Grade
f_{CLK}[7]			330	MHz	330 MHz Grade
Data and Control Setup, t_1[6]	0.2			ns	
Data and Control Hold, t_2[6]	1.5			ns	
Clock Period, t_3	3			ns	
Clock Pulsewidth High, t_4[6]	1.4			ns	f_{CLK_MAX} = 330 MHz
Clock Pulsewidth Low, t_5[6]	1.4			ns	f_{CLK_MAX} = 330 MHz
Clock Pulsewidth High, t_4[6]	1.875			ns	f_{CLK_MAX} = 240 MHz
Clock Pulsewidth Low, t_5[6]	1.875			ns	f_{CLK_MAX} = 240 MHz
Clock Pulsewidth High, t_4[6]	2.85			ns	f_{CLK_MAX} = 140 MHz
Clock Pulsewidth Low, t_5[6]	2.85			ns	f_{CLK_MAX} = 140 MHz
Clock Pulsewidth High, t_4	8.0			ns	f_{CLK_MAX} = 50 MHz
Clock Pulsewidth Low, t_5	8.0			ns	f_{CLK_MAX} = 50 MHz
Pipeline Delay, t_{PD}[6]	1.0	1.0	1.0	Clock Cycles	
PSAVE Up Time, t_{10}[6]		4	10	ns	

NOTES
[1]Timing specifications are measured with input levels of 3.0 V (V_{IH}) and 0 V (V_{IL}) for 3.3 V supplies.
[2]These maximum and minimum specifications are guaranteed over this range.
[3]Temperature range: T_{MIN} to T_{MAX}: –40°C to +85°C at 50 MHz and 140 MHz, 0°C to +70°C at 240 MHz and 330 MHz.
[4]Rise time was measured from the 10% to 90% point of zero to full-scale transition, fall time from the 90% to 10% point of a full-scale transition.
[5]Measured from 50% point of full-scale transition to 2% of final value.
[6]Guaranteed by characterization.
[7]f_{CLK} max specification production tested at 125 MHz and 5 V. Limits specified here are guaranteed by characterization.

Specifications subject to change without notice.



NOTES
1. OUTPUT DELAY (t_6) MEASURED FROM THE 50% POINT OF THE RISING EDGE OF CLOCK TO THE 50% POINT OF FULL-SCALE TRANSITION.
2. OUTPUT RISE/FALL TIME (t_7) MEASURED BETWEEN THE 10% AND 90% POINTS OF FULL-SCALE TRANSITION.
3. TRANSITION TIME (t_8) MEASURED FROM THE 50% POINT OF FULL-SCALE TRANSITION TO WITHIN 2% OF THE FINAL OUTPUT VALUE.

Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

V_{AA} to GND ..... 7 V
Voltage on any Digital Pin ..... GND – 0.5 V to V_{AA} + 0.5 V
Ambient Operating Temperature (T_A) ..... –40°C to +85°C
Storage Temperature (T_S) ..... –65°C to +150°C
Junction Temperature (T_J) ..... 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C
Vapor Phase Soldering (1 Minute) ..... 220°C
I_{OUT} to GND[2] ..... 0 V to V_{AA}

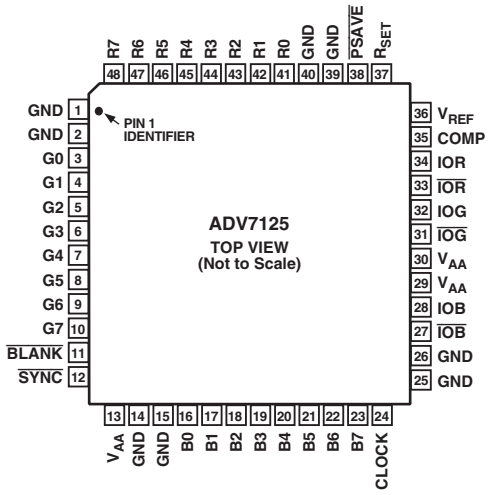
NOTES
[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2] Analog output short circuit to any power supply or common can be of an indefinite duration.

ORDERING GUIDE

	Speed Options			
Package	**50 MHz**[1]	**140 MHz**[1]	**240 MHz**[2]	**330 MHz**[2, 3]
Plastic LQFP (ST-48)	ADV7125KST50	ADV7125KST140	ADV7125JST240	ADV7125JST330

NOTES
[1]Specified for –40°C to +85°C operation.
[2]Specified for 0°C to +70°C operation.
[3]Available in 3.3 V version only.

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV7125 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin Number	Mnemonic	Function
1, 2, 14, 15, 25, 26, 39, 40	GND	Ground. All GND pins must be connected.
3–10, 16–23, 41–48	G0–G7, B0–B7, R0–R7	Red, Green, and Blue Pixel Data Inputs (TTL Compatible). Pixel data is latched on the rising edge of CLOCK. R0, G0, and B0 are the least significant data bits. Unused pixel data inputs should be connected to either the regular PCB power or ground plane.
11	$\overline{\text{BLANK}}$	Composite Blank Control Input (TTL Compatible). A logic zero on this control input drives the analog outputs, IOR, IOB, and IOG, to the blanking level. The $\overline{\text{BLANK}}$ signal is latched on the rising edge of CLOCK. While $\overline{\text{BLANK}}$ is a logical zero, the R0–R7, G0–G7, and B0–B7 pixel inputs are ignored.
12	$\overline{\text{SYNC}}$	Composite Sync Control Input (TTL Compatible). A logical zero on the $\overline{\text{SYNC}}$ input switches off a 40 IRE current source. This is internally connected to the IOG analog output. $\overline{\text{SYNC}}$ does not override any other control or data input; therefore, it should only be asserted during the blanking interval. $\overline{\text{SYNC}}$ is latched on the rising edge of CLOCK. If sync information is not required on the green channel, the $\overline{\text{SYNC}}$ input should be tied to logical zero.
13, 29, 30	V_{AA}	Analog Power Supply (5 V ± 5%). All V_{AA} pins on the ADV7125 must be connected.
24	CLOCK	Clock Input (TTL Compatible). The rising edge of CLOCK latches the R0–R7, G0–G7, B0–B7, $\overline{\text{SYNC}}$, and $\overline{\text{BLANK}}$ pixel and control inputs. It is typically the pixel clock rate of the video system. CLOCK should be driven by a dedicated TTL buffer.
27, 31, 33	$\overline{\text{IOR}}$, $\overline{\text{IOG}}$, $\overline{\text{IOB}}$	Differential Red, Green, and Blue Current Outputs (High Impedance Current Sources). These RGB video outputs are specified to directly drive RS-343A and RS-170 video levels into a doubly terminated 75 Ω load. If the complementary outputs are not required, these outputs should be tied to ground.
28, 32, 34	IOR, IOG, IOB	Red, Green, and Blue Current Outputs. These high impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable. All three current outputs should have similar output loads whether or not they are all being used.
35	COMP	Compensation Pin. This is a compensation pin for the internal reference amplifier. A 0.1 μF ceramic capacitor must be connected between COMP and V_{AA}.
36	V_{REF}	Voltage Reference Input for DACs or Voltage Reference Output (1.235 V)
37	R_{SET}	A resistor (R_{SET}) connected between this pin and GND controls the magnitude of the full-scale video signal. Note that the IRE relationships are maintained, regardless of the full-scale output current. The relationship between R_{SET} and the full-scale output current on IOG (assuming I_{SYNC} is connected to IOG) is given by: $$R_{SET}\ (\Omega) = 11,445 \times V_{REF}\ (V) / IOG\ (mA)$$ The relationship between R_{SET} and the full-scale output current on IOR, IOG, and IOB is given by: $$IOG\ (mA) = 11,444.8 \times V_{REF}\ (V) / R_{SET}\ (\Omega)\ (SYNC\ being\ asserted)$$ $$IOR, IOB\ (mA) = 7,989.6 \times V_{REF}\ (V) / R_{SET}\ (\Omega)$$ The equation for IOG will be the same as that for IOR and IOB when $\overline{\text{SYNC}}$ is not being used, i.e., $\overline{\text{SYNC}}$ tied permanently low.
38	$\overline{\text{PSAVE}}$	Power Save Control Pin. Reduced power consumption is available on the ADV7125 when this pin is active.

TERMINOLOGY

Blanking Level
The level separating the $\overline{\text{SYNC}}$ portion from the video portion of the waveform. Usually referred to as the front porch or back porch. At 0 IRE units, it is the level that will shut off the picture tube, resulting in the blackest possible picture.

Color Video (RGB)
This usually refers to the technique of combining the three primary colors of red, green, and blue to produce color pictures within the usual spectrum. In RGB monitors, three DACs are required, one for each color.

Sync Signal ($\overline{\text{SYNC}}$)
The position of the composite video signal that synchronizes the scanning process.

Grayscale
The discrete levels of video signal between reference black and reference white levels. An 8-bit DAC contains 256 different levels.

Raster Scan
The most basic method of sweeping a CRT one line at a time to generate and display images.

Reference Black Level
The maximum negative polarity amplitude of the video signal.

Reference White Level
The maximum positive polarity amplitude of the video signal.

Sync Level
The peak level of the $\overline{\text{SYNC}}$ signal.

Video Signal
The portion of the composite video signal that varies in grayscale levels between reference white and reference black. Also referred to as the picture signal, this is the portion that may be visually observed.

CIRCUIT DESCRIPTION AND OPERATION

The ADV7125 contains three 8-bit DACs, with three input channels, each containing an 8-bit register. Also integrated on board the part is a reference amplifier. CRT control functions $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$ are integrated on board the ADV7125.

Digital Inputs

Twenty-four bits of pixel data (color information) R0–R7, G0–G7, and B0–B7 are latched into the device on the rising edge of each clock cycle. This data is presented to the three 8-bit DACs and then converted to three analog (RGB) output waveforms (See Figure 2).

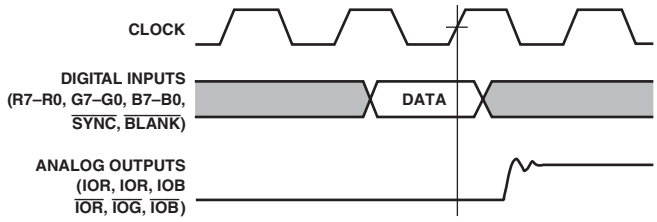


Figure 2. Video Data Input/Output

The ADV7125 has two additional control signals that are latched to the analog video outputs in a similar fashion. $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$ are each latched on the rising edge of CLOCK to maintain synchronization with the pixel data stream.

The $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$ functions allow for the encoding of these video synchronization signals onto the RGB video output. This is done by adding appropriately weighted current sources to the analog outputs, as determined by the logic levels on the $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$ digital inputs. Figure 3 shows the analog output, RGB video waveform of the ADV7125. The influence of $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ on the analog video waveform is illustrated.

Table I details the resultant effect on the analog outputs of $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$.

All these digital inputs are specified to accept TTL logic levels.

Clock Input

The CLOCK input of the ADV7125 is typically the pixel clock rate of the system. It is also known as the dot rate. The dot rate, and thus the required CLOCK frequency, will be determined by the on-screen resolution, according to the following equation:

Dot Rate = (*Horiz Res*) × (*Vert Res*) × (*Refresh Rate*)/(*Retrace Factor*)

Horiz Res = Number of Pixels/Line

Vert Res = Number of Lines/Frame

Refresh Rate = Horizontal Scan Rate. This is the rate at which the screen must be refreshed, typically 60 Hz for a noninterlaced system or 30 Hz for an interlaced system.

Retrace Factor = Total Blank Time Factor. This takes into account that the display is blanked for a certain fraction of the total duration of each frame (e.g., 0.8).

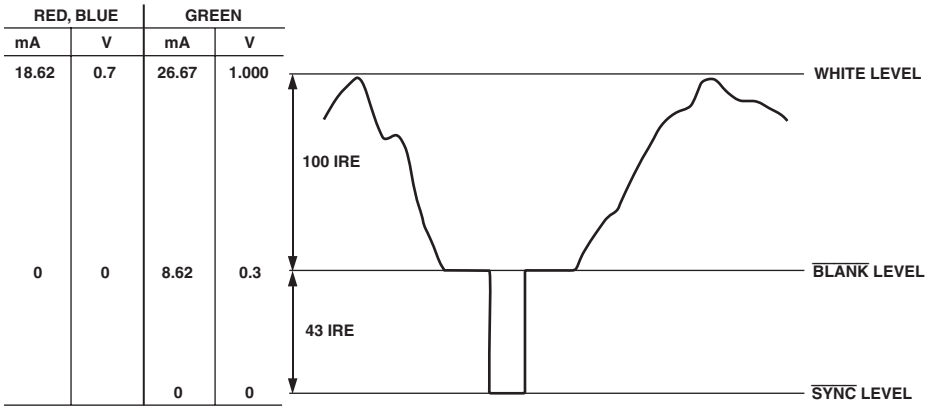


Figure 3. RGB Video Output Waveform

Table I. Video Output Truth Table (R_{SET} = 530 Ω, R_{LOAD} = 37.5 Ω)

Description	IOG (mA)	$\overline{\text{IOG}}$ (mA)	IOR/IOB	$\overline{\text{IOR}}$/$\overline{\text{IOB}}$	$\overline{\text{SYNC}}$	$\overline{\text{BLANK}}$	DAC Input Data
WHITE LEVEL	26.67	0	18.62	0	1	1	FFH
VIDEO	Video + 8.05	18.62 – Video	Video	18.62 – Video	1	1	Data
VIDEO to $\overline{\text{BLANK}}$	Video	18.62 – Video	Video	18.62 – Video	0	1	Data
BLACK LEVEL	8.05	18.62	0	18.62	1	1	00H
BLACK to $\overline{\text{BLANK}}$	0	18.62	0	18.62	0	1	00H
$\overline{\text{BLANK}}$ LEVEL	8.05	18.62	0	18.62	1	0	xxH
$\overline{\text{SYNC}}$ LEVEL	0	18.62	0	18.62	0	0	xxH

Therefore, if we have a graphics system with a 1024 × 1024 resolution, a noninterlaced 60 Hz refresh rate, and a retrace factor of 0.8, then:

$$Dot\ Rate = 1024 \times 1024 \times 60 / 0.8$$
$$= 78.6\ MHz$$

The required CLOCK frequency is thus 78.6 MHz.

All video data and control inputs are latched into the ADV7125 on the rising edge of CLOCK, as previously described in the Digital Inputs section. It is recommended that the CLOCK input to the ADV7125 be driven by a TTL buffer (e.g., 74F244).

Video Synchronization and Control

The ADV7125 has a single composite sync ($\overline{SYNC}$) input control. Many graphics processors and CRT controllers have the ability to generate horizontal sync (HSYNC), vertical sync (VSYNC), and composite $\overline{SYNC}$.

In a graphics system that does not automatically generate a composite $\overline{SYNC}$ signal, the inclusion of some additional logic circuitry enables the generation of a composite $\overline{SYNC}$ signal.

The sync current is internally connected directly to the IOG output, thus encoding video synchronization information onto the green video channel. If it is not required to encode sync information onto the ADV7125, the $\overline{SYNC}$ input should be tied to logic low.

Reference Input

The ADV7125 contains an on-board voltage reference. The V_{REF} pin is normally terminated to V_{AA} through a 0.1 μF capacitor. Alternatively, the part could, if required, be overdriven by an external 1.23 V reference (AD1580).

A resistance, R_{SET}, connected between the R_{SET} pin and GND determines the amplitude of the output video level according to Equations 1 and 2 for the ADV7125:

$$IOG * (mA) = 11,444.8 \times V_{REF}\ (V) / R_{SET}\ (\Omega) \quad (1)$$

$$IOR, IOB\ (mA) = 7,989.6 \times V_{REF}\ (V) / R_{SET}\ (\Omega) \quad (2)$$

*Applies to the ADV7125 only when SYNC is being used. If SYNC is not being encoded onto the green channel, Equation 1 will be similar to Equation 2.

Using a variable value of R_{SET} allows for accurate adjustment of the analog output video levels. Use of a fixed 560 Ω R_{SET} resistor yields the analog output levels quoted in the specification page. These values typically correspond to the RS-343A video waveform values as shown in Figure 3.

DACs

The ADV7125 contains three matched 8-bit DACs. The DACs are designed using an advanced, high speed, segmented architecture. The bit currents corresponding to each digital input are routed to either the analog output (bit = "1") or GND (bit = "0") by a sophisticated decoding scheme. As all this circuitry is on one monolithic device, matching between the three DACs is optimized. As well as matching, the use of identical current sources in a monolithic design guarantees monotonicity and low glitch. The on-board operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

Analog Outputs

The ADV7125 has three analog outputs, corresponding to the red, green, and blue video signals.

The red, green, and blue analog outputs of the ADV7125 are high impedance current sources. Each one of these three RGB current outputs is capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable. Figure 4a shows the required configuration for each of the three RGB outputs connected into a doubly terminated 75 Ω load. This arrangement develops RS-343A video output voltage levels across a 75 Ω monitor.

A suggested method of driving RS-170 video levels into a 75 Ω monitor is shown in Figure 4b. The output current levels of the DACs remain unchanged, but the source termination resistance, Z_S, on each of the three DACs is increased from 75 Ω to 150 Ω.

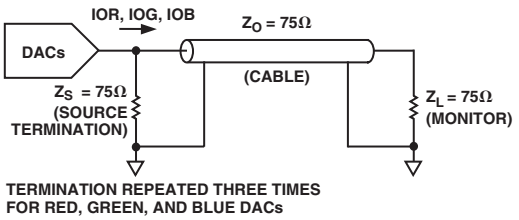


Figure 4a. Analog Output Termination for RS-343A

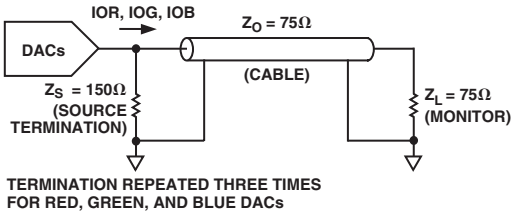


Figure 4b. Analog Output Termination for RS-170

More detailed information regarding load terminations for various output configurations, including RS-343A and RS-170, is available in an application note entitled, *Video Formats and Required Load Terminations* available from Analog Devices, (www.analog.com/library/applicationNotes/video/AN205.pdf).

Figure 3 shows the video waveforms associated with the three RGB outputs driving the doubly terminated 75 Ω load of Figure 4a. As well as the gray scale levels (black level to white level), the diagram also shows the contributions of $\overline{SYNC}$ and $\overline{BLANK}$ for the ADV7125. These control inputs add appropriately weighted currents to the analog outputs, producing the specific output level requirements for video applications. Table I details how the $\overline{SYNC}$ and $\overline{BLANK}$ inputs modify the output levels.

Grayscale Operation

The ADV7125 can be used for standalone, grayscale (monochrome) or composite video applications (i.e., only one channel used for video information). Any one of the three channels, red, green, or blue, can be used to input the digital video data. The two unused video data channels should be tied to logical zero. The unused analog outputs should be terminated with the same load as that for the used channel. In other words, if the red

channel is used and IOR is terminated with a doubly terminated 75 Ω load (37.5 Ω), IOB and IOG should be terminated with 37.5 Ω resistors (See Figure 5).

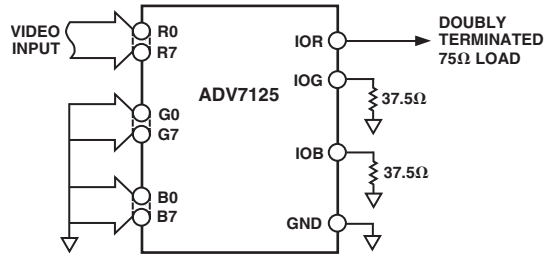


Figure 5. Input and Output Connections for Standalone Grayscale or Composite Video

Video Output Buffers

The ADV7125 is specified to drive transmission line loads, as are most monitors rated. The analog output configurations to drive such loads are described in the Analog Outputs section and are illustrated in Figure 6. However, in some applications, it may be required to drive long transmission line cable lengths. Cable lengths greater than 10 meters can attenuate and distort high frequency analog output pulses. The inclusion of output buffers will compensate for some cable distortion. Buffers with large full power bandwidths and gains between two and four will be required. These buffers will also need to be able to supply sufficient current over the complete output voltage swing. Analog Devices produces a range of suitable op amps for such applications. These include the AD84x series of monolithic op amps. In very high frequency applications (80 MHz), the AD8061 is recommended. More information on line driver buffering circuits is given in the relevant op amp data sheets.

Use of buffer amplifiers also allows implementation of other video standards besides RS-343A and RS-170. Altering the gain components of the buffer circuit will result in any desired video level.

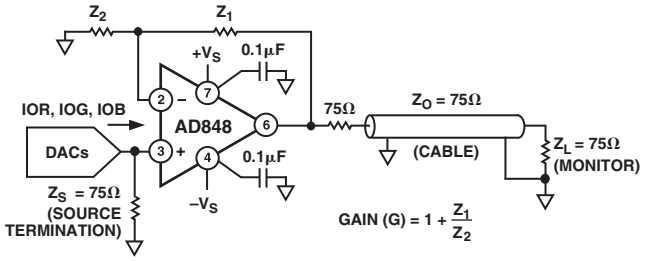


Figure 6. AD848 As an Output Buffer

PC Board Layout Considerations

The ADV7125 is optimally designed for lowest noise performance, both radiated and conducted noise. To complement the excellent noise performance of the ADV7125, it is imperative that great care be given to the PC board layout. Figure 7 shows a recommended connection diagram for the ADV7125.

The layout should be optimized for lowest noise on the ADV7125 power and ground lines. This can be achieved by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins should by minimized to minimize inductive ringing.

Ground Planes

The ADV7125 and associated analog circuitry should have a separate ground plane referred to as the analog ground plane. This ground plane should connect to the regular PCB ground plane at a single point through a ferrite bead, as illustrated in Figure 7. This bead should be located as close as possible (within three inches) to the ADV7125.

The analog ground plane should encompass all ADV7125 ground pins, voltage reference circuitry, power supply bypass circuitry, the analog output traces, and any output amplifiers.

The regular PCB ground plane area should encompass all the digital signal traces, excluding the ground pins, leading up to the ADV7125.

Power Planes

The PC board layout should have two distinct power planes, one for analog circuitry and one for digital circuitry. The analog power plane should encompass the ADV7125 (V_{AA}) and all associated analog circuitry. This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead, as illustrated in Figure 6. This bead should be located within three inches of the ADV7125.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV7125 power pins, voltage reference circuitry, and any output amplifiers.

The PCB power and ground planes should not overlay portions of the analog power plane. Keeping the PCB power and ground planes from overlaying the analog power plane will contribute to a reduction in plane-to-plane noise coupling.

Supply Decoupling

Noise on the analog power plane can be further reduced by the use of multiple decoupling capacitors (see Figure 7).

Optimum performance is achieved by the use of 0.1 µF ceramic capacitors. Each of the two groups of V_{AA} should be individually decoupled to ground. This should be done by placing the capacitors as close as possible to the device with the capacitor leads as short as possible, thus minimizing lead inductance.

It is important to note that while the ADV7125 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise. A dc power supply filter (Murata BNX002) will provide EMI suppression between the switching power supply and the main PCB. Alternatively, consideration could be given to using a three-terminal voltage regulator.

Digital Signal Interconnect

The digital signal lines to the ADV7125 should be isolated as much as possible from the analog outputs and other analog circuitry. Digital signal lines should not overlay the analog power plane.

Due to the high clock rates used, long clock lines to the ADV7125 should be avoided to minimize noise pickup.

Any active pull-up termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}) and not the analog power plane.

Analog Signal Interconnect

The ADV7125 should be located as close as possible to the output connectors, thus minimizing noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane and not the analog power plane, thereby maximizing the high frequency power supply rejection.

For optimum performance, the analog outputs should each have a source termination resistance to ground of 75 Ω (doubly terminated 75 Ω configuration). This termination resistance should be as close as possible to the ADV7125 to minimize reflections.

Additional information on PCB design is available in an application note entitled *Design and Layout of a Video Graphics System for Reduced EMI*. This application note is available from Analog Devices, publication no. E1309–15–10/89 (www.analog.com/library/applicationNotes/designTech/AN333.pdf).

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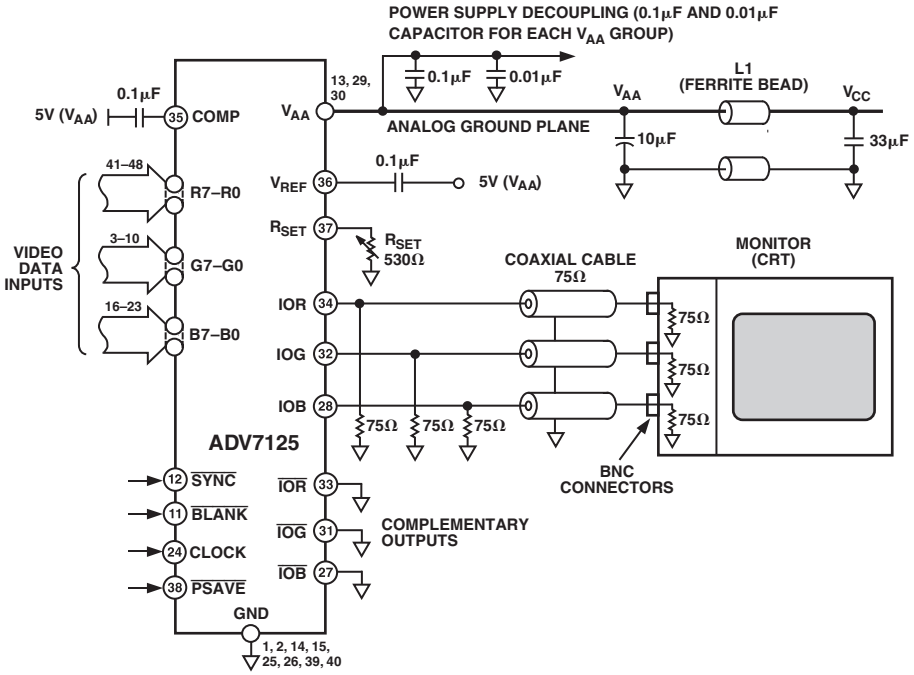
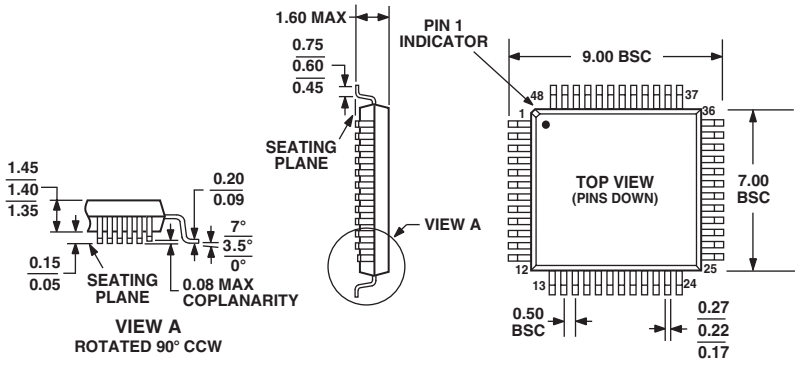


Figure 7. Typical Connection Diagram

OUTLINE DIMENSIONS

48-Lead Plastic Quad Flatpack [LQFP]
1.4 mm Thick
(ST-48)

Dimensions shown in millimeters



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