Enhanced Memory Systems Inc.

DM2242/2252 EDRAM Multibank EDO 1Mb x 4 Enhanced Dynamic RAM

Product Specification

Features

- 8Kbit SRAM Cache Memory for 12ns Random Reads Within Four Active Pages (Multibank Cache)
- Fast 4Mbit DRAM Array for 30ns Access to Any New Page
- Write Posting Register for 12ns Random Writes and Burst Writes Within a Page (Hit or Miss)
- 256-byte Wide DRAM to SRAM Bus for 14.2 Gigabytes/Sec Cache Fill
- On-chip Cache Hit/Miss Comparators Maintain Cache Coherency on Writes
- Hidden Precharge and Refresh Cycles
- Write-per-bit Option (DM2252) for Parity and Video Applications
- Extended 64ms Refresh Period for Low Standby Power
- 300 Mil Plastic SOJ and TSOP-II Package Options
- +5 and +3.3 Volt Power Supply Voltage Options
- Multibank Extended Data Output (EDO) for Faster System Operation
- Low Power, Self Refresh Mode Option
- Industrial Temperature Range Option

Description

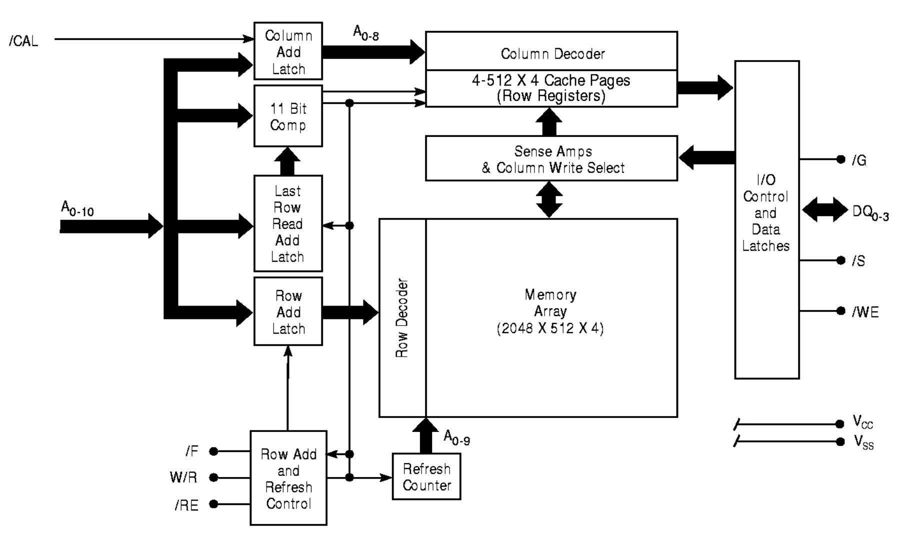
The 4Mb Multibank EDO Enhanced DRAM (EDRAM) combines raw speed with innovative architecture to offer the optimum cost-performance solution for high performance local or system main memory. In most high speed applications, no-wait-state performance can be achieved without secondary SRAM cache and without interleaving main memory banks at system clock speeds through 83MHz. Two-way interleave will allow no-wait-state operation at clock speeds greater than 132MHz without the need of secondary SRAM cache. The EDRAM outperforms conventional SRAM cache plus DRAM memory systems by minimizing processor wait states for all possible bus events, not just cache hits. The combination of data and address latching, 8K of fast on-chip SRAM cache, and simplified on-chip cache control allows system level flexibility, performance, and overall memory cost reduction not available with any other high density memory component. The 8Kbit cache is now arranged as four 512 x 4 direct mapped row registers. This improves the hit rate over a smaller size cache or a single bank, 8Kbit cache. The EDO feature allows the column addresses and data to be pipelined to allow for shorter memory cycle times and higher bandwidth. Architectural similarity with JEDEC DRAMs allows a single memory controller design to support either slow JEDEC DRAMs or high speed EDRAMs. A system designed in this manner can provide a simple upgrade path to higher system performance.

Architecture

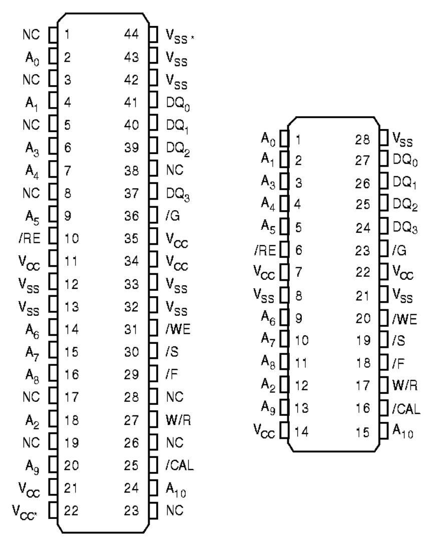
The EDRAM architecture has a simple integrated SRAM cache which allows it to operate much like an EDO DRAM.

The EDRAM's SRAM cache is integrated into the DRAM array as tightly coupled row registers. The 1Mx4 EDRAM has a total of four independent DRAM memory banks each with its own 512 x 4 SRAM row register. Memory reads always occur from the cache row register of one of these banks as specified by row address bits A_2 and

Functional Diagram



TSOP-II Pin Configuration *SOJ Pin Configuration*



* Reserved for future use

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A_9 (bank select). When the internal comparator detects that the row address matches the last row read from any of the four DRAM banks (page hit), the SRAM is accessed and data is available on the output pins in 12ns from column address input. Subsequent reads within the page (burst reads or random reads) can continue at 12ns cycle time. When the row address does not match the last row read from any of the four DRAM banks (page miss), the new DRAM row is accessed and loaded into the appropriate SRAM row register and data is available on the output pins all within 30ns from row enable. Subsequent reads within the page (burst reads or random reads) can continue at 12ns cycle time.

Since reads occur from the SRAM cache, the DRAM precharge can occur during burst reads. This eliminates the precharge time delay suffered by other DRAMs and SDRAMs when accessing a new page. The EDRAM has an independent on-chip refresh counter and dedicated refresh control pin to allow the DRAM array to be refreshed concurrently with cache read operations (hidden refresh).

During EDO EDRAM read accesses, the first column address is latched on the falling edge of /CAL. Then the next column address is placed on the bus while the data from the previous column address is output from the data latch after time t_{CLV}. On the next rising edge of /CAL, the data can be latched by the system. On the next falling edge of /CAL, the second column address is latched while the data for the previous column address is removed from the data bus. After time t_{CLV} the data for the second column address will be output on the data bus. This pipelining feature of EDO EDRAM allows for data transfers up to 83MHz without the need to interleave memory or add secondary cache.

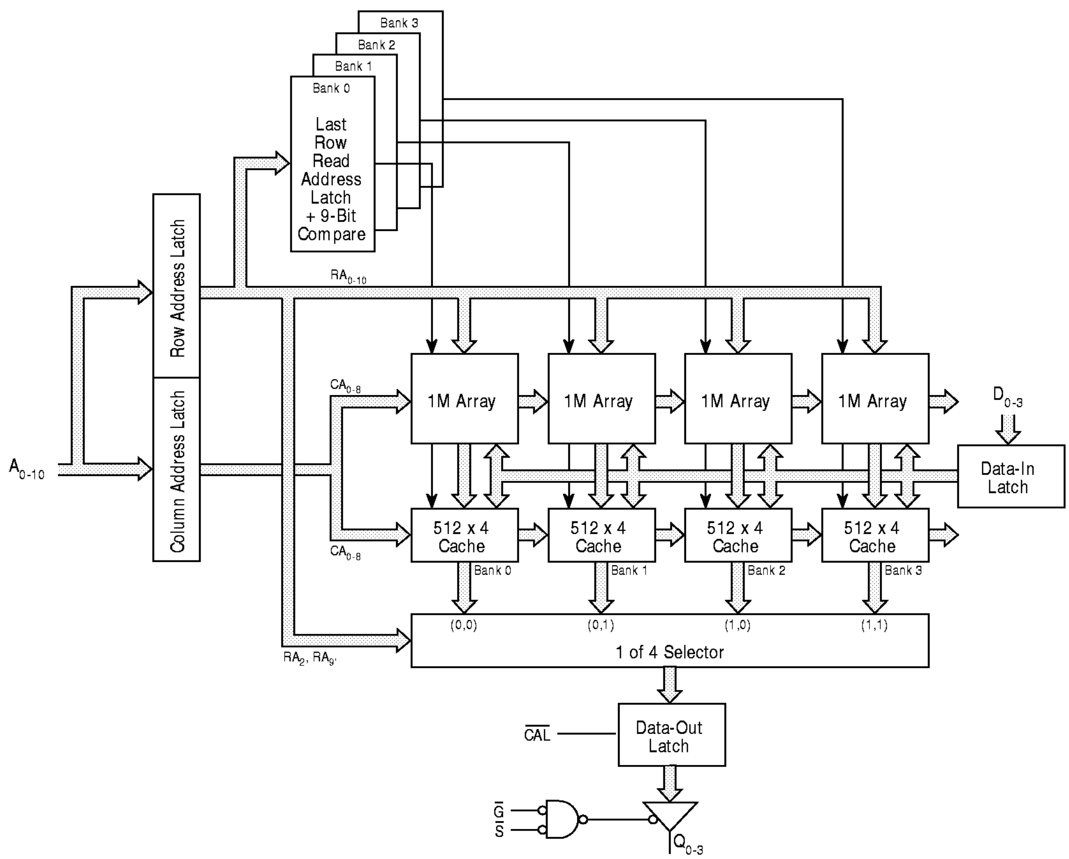
Memory writes are posted to the input data latch and directed to the DRAM array. During a write hit, the on-chip address comparator activates a parallel write path to the SRAM cache to maintain coherency. Random or page mode writes can be posted 5ns after column address and data area available. The EDRAM allows 12ns page mode cycle time for both write hits and write misses. Memory writes do not affect the contents of the cache row register except during a cache hit. Since the DRAM array can be written to at SRAM speeds, there is no need for complex writeback schemes.

By integrating the SRAM cache as row registers in the DRAM array and keeping the on-chip control simple, the EDRAM is able to provide superior performance over standard slow 4Mb DRAMs. By eliminating the need for SRAMs and cache controllers, system cost, board space, and power can all be reduced.

Functional Description

The EDRAM is designed to provide optimum memory performance with high speed microprocessors. As a result, it is possible to perform simultaneous operations to the DRAM and SRAM cache sections of the EDRAM. This feature allows the EDRAM

Four Bank Cache Architecture



to hide precharge and refresh operation during SRAM cache reads and maximize SRAM cache hit rate by maintaining valid cache contents during write operations even if data is written to another memory page. These new functions, in conjunction with the faster basic DRAM and cache speeds of the EDRAM, minimize processor wait states.

EDRAM Basic Operating Modes

The EDRAM operating modes are specified in the table below.

Hit and Miss Terminology

In this datasheet, "hit" and "miss" always refer to a hit or miss to any of the four pages of data contained in the SRAM cache row registers. There are four cache row registers, one for each of the four banks of DRAM. These registers are specified by the bank select row address bits A_2 and A_9. The contents of these cache row registers is always equal to the last row that was read from each of the four internal DRAM banks (as modified by any write hit data).

DRAM Read Hit

A DRAM read request is initiated by clocking /RE with W/R low and /F high. The EDRAM compares the new row address to the last row read address latch for the bank specified by row address bits $A_{2,9}$ (LRR: a 9-bit row address latch for each internal DRAM bank which is reloaded on each /RE active read miss cycle). If the row address matches the LRR, the requested data is already in the SRAM cache and no DRAM memory reference is initiated. The data specified by the column address is available at the output pins at the greater of times t_{RAC1}, t_{AC}, t_{GQV}, and $t_{ASC}+ t_{CLV}$. Since no DRAM activity is initiated, /RE can be brought high after time t_{RE1}, and a shorter precharge time, t_{RP1}, is allowed. It is possible to access additional SRAM cache locations by providing new column addresses to the multiplex address inputs. New data is available at the output at time $t_{ASC}+ t_{CLV}$ after each column address change.

DRAM Read Miss

A DRAM read request is initiated by clocking /RE with W/R low and /F high. The EDRAM compares the new row address to the LRR address latch for bank specified by row address bits $A_{2,9}$ (LRR: a 9-bit row address latch for each internal DRAM bank which is reloaded on each /RE active read miss cycle). If the row address does not match the LRR, the requested data is not in SRAM cache and a new row must be fetched from the DRAM. The EDRAM will load the new row data into the SRAM cache and update the LRR latch. The data at the specified column address is available at the output pins at the greater of times t_{RAC1}, t_{AC}, t_{GQV}, and $t_{ASC}+ t_{CLV}$. It is possible to bring /RE high after time t_{RE} since the new row data is safely latched into SRAM cache. This allows the EDRAM to precharge the DRAM array while data is accessed from SRAM cache. It is possible to access additional SRAM cache locations by providing new column addresses to the multiplex address inputs. New data is available at the output at time $t_{ASC}+ t_{CLV}$ after each column address change.

DRAM Write Hit

A DRAM write request is initiated by clocking /RE while W/R, /WE, and /F are high. The EDRAM will compare the new row address to the LRR address latch for the bank specified by row address bits $A_{2,9}$ (LRR: a 9-bit row address latch for each internal DRAM bank which is reloaded on each /RE active read miss cycle). If the row address matches the LRR, the EDRAM will write data to both the DRAM page in the appropriate bank and its corresponding SRAM cache simultaneously to maintain coherency. The write address and data are posted to the DRAM as soon as the column address is latched by bringing /CAL low and the write data is latched by bringing /WE low. The write address and data can be latched very quickly after the fall of /RE (t_{RAH} + t_{ASC} for the column address and t_{DS} for the data). During a write burst sequence, the second write data can be posted at time t_{RSW} after /RE. Subsequent writes within a page can occur with write cycle time t_{PC}. With /G enabled and /WE disabled, it is possible to perform cache read operations while the /RE is activated in write hit mode. This allows read-modify-write, write-verify, or random read-write sequences within the page with 12ns cycle times (the first read cannot complete until after time t_{RAC2}). At the end of a write sequence (after /CAL and /WE are brought high and t_{RE} is satisfied), /RE can be brought high to precharge the memory. It is possible to perform cache reads concurrently with precharge. During write sequences, a write operation is not performed unless both /CAL and /WE are low. As a result, the /CAL input can be used as a byte write select in multi-chip systems.

DRAM Write Miss

A DRAM write request is initiated by clocking /RE while W/R, /WE, and /F are high. The EDRAM will compare the new row address to the LRR address latch for the bank specified for row address bits $A_{2,9}$ (LRR: a 9-bit row address latch for each internal

EDRAM Basic Operating Modes

Function	/S	/RE	W/R	/F	/CAL	/WE	A_{0-10}	Comment
Read Hit	L	↓	L	H	H	X	Row = LRR	No DRAM Reference, Data in Cache
Read Miss	L	↓	L	H	H	X	Row ≠ LRR	DRAM Row to Cache
Write Hit	L	↓	H	H	H	H	Row = LRR	Write to DRAM and Cache, Reads Enabled
Write Miss	L	↓	H	H	H	H	Row ≠ LRR	Write to DRAM, Cache Not Updated, Reads Disabled
Internal Refresh	X	↓	X	L	X	X	X	Cache Reads Enabled
Low Power Standby	H	H	X	X	H	H	X	1mA Standby Current
Unallowed Mode	H	L	X	H	X	X	X	Unallowed Mode (Except -L Option)
Low Power Self-Refresh Option	H	↓	H	H	L	H	X	Standby Current, Internal Refresh Clock (-L Option)

H = High; L = Low; X = Don't Care; ↓ = High-to-Low Transition; LRR = Last Row Read

DRAM bank which is reloaded on each /RE active read miss cycle). If the row address does not match any of the LRRs, the EDRAM will write data to the DRAM page in the appropriate banks and the contents of the current cache is not modified. The write address and data are posted to the DRAM as soon as the column address is latched by bringing /CAL low and the write data is latched by bringing /WE low. The write address and data can be latched very quickly after the fall of /RE (t_{RAH} + t_{ASC} for the column address and t_{DS} for the data). During a write burst sequence, the second write data can be posted at time t_{RSW} after /RE. Subsequent writes within a page can occur with write cycle time t_{PC}. During a write miss sequence, cache reads are inhibited and the output buffers are disabled (independently of /G) until time t_{WRR} after /RE goes high. At the end of a write sequence (after /CAL and /WE are brought high and t_{RE} is satisfied), /RE can be brought high to precharge the memory. It is possible to perform cache reads concurrently with the precharge. During write sequences, a write operation is not performed unless both /CAL and /WE are low. As a result, /CAL can be used as a byte write select in multi-chip systems.

/RE Inactive Operation

It is possible to read data from the SRAM cache without clocking /RE. This option is desirable when the external control logic is capable of fast hit/miss comparison. In this case, the controller can avoid the time required to perform row/column multiplexing on hit cycles. This capability also allows the EDRAM to perform cache read operations during precharge and refresh cycles to minimize wait states and reduce power. It is only necessary to select /S and /G and provide the appropriate column address to read data. The row address of the SRAM cache accessed without clocking /RE will be specified by the LRR address latch loaded during the last /RE active read cycle. To perform a cache read, /CAL is clocked to latch the column address. The cache data is valid at time t_{CLV} after the column address is setup to /CAL.

Internal Refresh

If /F is active (low) on the assertion of /RE, an internal refresh cycle is executed. This cycle refreshes the row address supplied by an internal refresh counter. This counter is incremented at the end of the cycle in preparation for the next /F refresh cycle. At least 1,024 /F cycles must be executed every 64ms. /F refresh cycles can be hidden because cache memory can be read under column address control throughout the entire /F cycle.

Low Power Mode

The EDRAM enters its low power mode when /S is high. In this mode, the internal DRAM circuitry is powered down to reduce standby current to 1mA.

Low Power, Self-Refresh Mode Option

When the low power, self refresh mode option is specified when ordering the EDRAM, the EDRAM enters this mode when /RE is clocked while /S, W/R, /F, and /WE are high; and /CAL is low. In this mode, the power is turned off to all I/O pins except /RE to minimize chip power, and an on-board refresh clock is enabled to perform self-refresh cycles using the on-board refresh counter. The EDRAM remains in this low power mode until /RE is brought high again to terminate the mode. The EDRAM /RE input must remain high for t_{RP2} following exit from self-refresh mode to allow any on-going internal refresh to terminate prior to the next memory operation.

Write-Per-Bit Operation

The DM2252 version of the 1Mb x 4 EDRAM offers a write-per-bit capability which allows single bits of the memory to be selectively written without altering other bits in the same word. This capability may be useful for implementing parity or masking data in video graphics applications. The bits to be written are determined by a bit mask data word which is placed on the I/O data pins DQ_{0-3} prior to clocking /RE. The logic one bits in the mask data select the bits to be written. As soon as the mask is latched by /RE, the mask data is removed and write data can be placed on the databus. The mask is only specified on the /RE transition. During page mode burst write operations, the same mask is used for all write operations.

+3.3 Volt Power Supply Operation

If the +3.3 volt power supply option is specified, the EDRAM will operate from a +3.3 volt ±0.3 volt power supply and all inputs and outputs will have LVTTL/LVCMOS compatible signal levels. The +3.3 volt EDRAM will not accept input levels which exceed the power supply voltage. If mixed I/O levels are expected in your system, please specify the +5 volt version of the EDRAM.

/CAL Before /RE Refresh ("/CAS Before /RAS")

/CAL before /RE refresh, a special case of internal refresh, is discussed in the "Reduced Pin Count Operation" section.

/RE Only Refresh Operation

Although /F refresh using the internal refresh counter is the recommended method of EDRAM refresh, it is possible to perform

Pin Names

Pin Names	Function
A_{0-10}	Address Inputs
/RE	Row Enable
DQ_{0-3}	Data In/Data Out
/CAL	Column Address Latch
W/R	Write/Read Control
V_{CC}	Power (+5V or +3.3V)

Pin Names	Function
V_{SS}	Ground
/WE	Write Enable
/G	Output Enable
/F	Refresh Control
/S	Chip Select - Active/Standby Control
NC	Not Connected

an /RE only refresh using an externally supplied row address. /RE refresh is performed by executing a *write cycle* (W/R and /F are high) where /CAL is not clocked. This is necessary so that the current cache contents and LRR are not modified by the refresh operation. All combinations of addresses A_{0-9} must be sequenced every 64ms refresh period. A_{10} does not need to be cycled. Read refresh cycles are not allowed because a DRAM refresh cycle does not occur when a read refresh address matches the LRR address latch.

Initialization Cycles

A minimum of eight /RE active initialization cycles (read, write or refresh) are required before normal operation is guaranteed. Following these start-up cycles, two read cycles to different row addresses must be performed for each of the four internal banks of DRAM to initialize the internal cache logic. Row address bits A_2 and A_9 define the four internal DRAM banks. /RE must be high for at least 300ns prior to initialization.

Unallowed Mode

Read, write, or /RE only refresh operations must not be initiated to unselected memory banks by clocking /RE when /S is high.

Reduced Pin Count Operation

Although it is desirable to use all EDRAM control pins to optimize system performance, it is possible to simplify the interface to the EDRAM by either tying pins to ground or by tying one or more control inputs together. The /S input can be tied to ground if the low power standby modes are not required. The /CAL and /F pins can be tied together if hidden refresh operation is not required. In this case, a CBR refresh (/CAL before /RE) can be performed by holding the combined input low prior to /RE. A CBR refresh does not require that a row address be supplied when /RE is asserted. The timing is identical to /F refresh cycle timing. The /WE input can be tied to /CAL if independent posting of column addresses and data are not required during write operations. In this case, both column address and write data will be latched by the combined input during writes. W/R and /G can be tied together if reads are not performed during write hit cycles. If these techniques are used, the EDRAM will require only three control lines for operation (/RE, /CAS [combined /CAL, /F, and /WE], and W/R [combined W/R and /G]). The simplified control interface still allows the fast page read/write cycle times, fast random read/write times, and hidden precharge functions available with the EDRAM.

Pin Descriptions

/RE — Row Enable

This input is used to initiate DRAM read and write operations and latch a row address. It is not necessary to clock /RE to read data from the EDRAM SRAM row registers. On read operations, /RE can be brought high as soon as data is loaded into cache to allow early precharge.

/CAL — Column Address Latch

This input is used to latch the column address and in combination with /WE to trigger write operations. When /CAL is high, the column address latch is transparent. When /CAL is low, the column address latch is closed and the output of the latch contains the address present while /CAL was high. It also controls the operation of the output data latch. Data is latched while /CAL is high, and the latch is transparent when /CAL is low.

W/R — Write/Read

This input along with /F specifies the type of DRAM operation initiated on the low going edge of /RE. When /F is high, W/R specifies either a write (logic high) or read operation (logic low).

/F — Refresh

This input will initiate a DRAM refresh operation using the internal refresh counter as an address source when it is low on the low going edge of /RE.

/WE — Write Enable

This input controls the latching of write data on the input data pins. A write operation is initiated when both /CAL and /WE are low.

/G — Output Enable

This input controls the gating of read data to the output data pins during read operations.

/S — Chip Select

This input is used to power up the I/O and clock circuitry. When /S is high, the EDRAM remains in its low power mode. /S must remain active throughout any read or write operation. With the exception of /F refresh cycles, /RE should never be clocked when /S is inactive.

DQ_{0-3} — Data Input/Output

These bidirectional data pins are used to read and write data to the EDRAM. On the DM2252 write-per-bit memory, these pins are also used to specify the bit mask used during write operations.

A_{0-10} — Multiplex Address

These inputs are used to specify the row and column addresses of the EDRAM data. The 11-bit row address is latched on the falling edge of /RE. The 9-bit column address can be specified at any other time to select read data from the SRAM cache or to specify the write column address during write cycles.

V_{CC} Power Supply

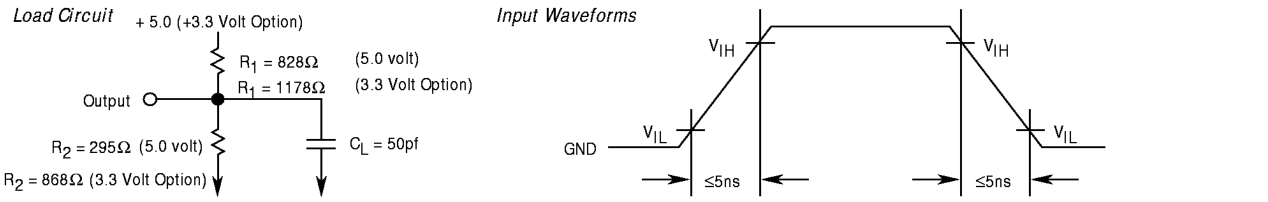
These inputs are connected to the +5 or +3.3 volt power supply.

V_{SS} Ground

These inputs are connected to the power supply ground connection.

AC Test Load and Waveforms

V_{IN} Timing Reference Point at V_{IL} and V_{IH}



Absolute Maximum Ratings

(Beyond Which Permanent Damage Could Result)

Description	3.3V Option Rating	Ratings
Input Voltage (V_{IN})	- .5 ~ 4.6v	- 1 ~ 7v
Output Voltage (V_{OUT})	- .5 ~ 4.6v	- 1 ~ 7v
Power Supply Voltage (V_{CC})	- .5 ~ 4.6v	- 1 ~ 7v
Ambient Operating Temperature (T_A)	-40 ~ +85°C	-40 ~ +85°C
Storage Temperature (T_S)	-55 ~ 150°C	-55 ~ 150°C
Static Discharge Voltage (Per MIL-STD-883 Method 3015)	Class 1	Class 1
Short Circuit O/P Current (I_{OUT})	20mA*	50mA*

*One output at a time; short duration.

Capacitance

Description	Max	Pins
Input Capacitance	6pf	A_{0-10}
Input Capacitance	7pf	/CAL, /RE, W/R, /WE, /F, /S
Input Capacitance	2pf	/G
I/O Capacitance	6pf	DQ_{0-3}

Electrical Characteristics

T_A = 0 to 70°C (Commercial), -40 to 85°C (Industrial)

Symbol	Parameters	+3.3V Option Min	+3.3V Option Max	Min	Max	Test Conditions
V_{CC}	Supply Voltage	3.0V	3.6V	4.75V	5.25V	All Voltages Referenced to V_{SS}
V_{IH}	Input High Voltage	2.0V	V_{CC}+0.3V	2.4V	Vcc+0.5V	
V_{IL}	Input Low Voltage	Vss-0.3V	0.8V	Vss-0.5V	0.8V	
V_{OH}	Output High Level	2.4V	—	2.4V	—	I_{OUT} = - 5mA (-2ma For 3.3 Volt Option)
V_{OL}	Output Low Level	—	0.4V	—	0.4V	I_{OUT} = 4.2mA (2ma For 3.3 Volt Option)
$I_{i(L)}$	Input Leakage Current	-5µA	5µA	-10µA	10µA	OV ≤ V_{IN} ≤ Vcc to 0.5 Volt
$I_{O(L)}$	Output Leakage Current	-5µA	5µA	-10µA	10µA	O ≤ $V_{I/O}$ ≤ Vcc

Symbol	Operating Current	33MHz Typ (1)	-12 Max	-15 Max	Test Condition	Notes
I_{CC1}	Random Read	110mA	225mA	180mA	/RE, /CAL, and Addresses Cycling: $t_C = t_C$ Minimum	2, 3, 5
I_{CC2}	Fast Page Mode Read	65mA	145mA	115mA	/CAL and Addresses Cycling: $t_{PC} = t_{PC}$ Minimum	2, 4, 5
I_{CC3}	Static Column Read	55mA	110mA	90mA	Addresses Cycling: $t_{SC} = t_{SC}$ Minimum	2, 4, 5
I_{CC4}	Random Write	135mA	190mA	150mA	/RE, /CAL, /WE, and Addresses Cycling: $t_C = t_C$ Minimum	2, 3
I_{CC5}	Fast Page Mode Write	50mA	135mA	105mA	/CAL, /WE, and Addresses Cycling: $t_{PC} = t_{PC}$ Minimum	2, 4
I_{CC6}	Standby	1mA	1mA	1mA	All Control Inputs Stable ≥ V_{CC} - 0.2V, Output Driven	
I_{CC7}	Self-Refresh (-L Option)	200 µA	200 µA	200 µA	/S, /F, W/R, /WE, and A_{0-10} at ≥ V_{CC} - 0.2V /RE and /CAL at ≤ V_{SS} + 0.2V, I/O Open	
I_{CCT}	Average Typical Operating Current	30mA	—	—	See "Estimating EDRAM Operating Power" Application Note	1

(1) "33MHz Typ" refers to worst case I_{CC} expected in a system operating with a 33MHz memory bus. See power applications note for further details. This parameter is not 100% tested or guaranteed. (2) I_{CC} is dependent on cycle rates and is measured with CMOS levels and the outputs open. (3) I_{CC} is measured with a maximum of one address change while /RE = V_{IL}. (4) I_{CC} is measured with a maximum of one address change while /CAL = V_{IH}. (5) /G is high.

Switching Characteristics

V_{CC} = 5V ± 5% (+5 Volt Option), V_{CC} = 3.3V ± 0.3V (+3.3 Volt Option), C_L = 50pf, T_A = 0 to 70°C (Commercial), -40 to 85°C (Industrial)

Symbol	*Description*	*-12*		*-15*		*Units*
		Min	*Max*	*Min*	*Max*	
t_{AC}[1]	Column Address Access Time		12		15	ns
t_{ACH}	Column Address Valid to /CAL Inactive (Write Cycle)	12		15		ns
t_{ACI}	Column Address Valid to /CAL Inactive	12		15		ns
t_{AQX}	Column Address Change to Output Data Invalid	5		5		ns
t_{ASC}	Column Address Setup Time	5		5		ns
t_{ASR}	Row Address Setup Time	5		5		ns
t_{C}	Row Enable Cycle Time	55		65		ns
t_{C1}	Row Enable Cycle Time, Cache Hit (Row=LRR), Read Cycle Only	20		25		ns
t_{CAE}	Column Address Latch Active Time	5		6		ns
t_{CAH}	Column Address Hold Time	0		0		ns
t_{CH}	Column Address Latch High Time (Latch Transparent)	5		5		ns
t_{CHR}	/CAL Inactive Lead Time to /RE Inactive (Write Cycles Only)	-2		-2		ns
t_{CHW}	Column Address Latch High to Write Enable Low (Multiple Writes)	0		0		ns
t_{CLV}	Column Address Latch High to Data Valid		7		7	ns
t_{CQH}	Column Address Latch Low to Data Invalid	3		3		ns
t_{CQV}	Column Address Latch Low to Data Valid		7		7	ns
t_{CRP}	Column Address Latch Setup Time to Row Enable	5		5		ns
t_{CWL}	/WE Low to /CAL Inactive	5		5		ns
t_{DH}	Data Input Hold Time	0		0		ns
t_{DMH}	Mask Hold Time From Row Enable (Write-Per-Bit)	1		1.5		ns
t_{DMS}	Mask Setup Time to Row Enable (Write-Per-Bit)	5		5		ns
t_{DS}	Data Input Setup Time	5		5		ns
t_{GQV}[1]	Output Enable Access Time		5		5	ns
t_{GQX}[2,3]	Output Enable to Output Drive Time	0	5	0	5	ns
t_{GQZ}[4,5]	Output Turn-Off Delay From Output Disabled (/G↑)	0	5	0	5	ns
t_{MH}	/F and W/R Mode Select Hold Time	0		0		ns
t_{MSU}	/F and W/R Mode Select Setup Time	5		5		ns
t_{NRH}	/CAL, /G, W/R, and /WE Hold Time For /RE-Only Refresh	0		0		ns
t_{NRS}	/CAL, /G, W/R, and /WE Setup Time For /RE-Only Refresh	5		5		ns
t_{PC}	Column Address Latch Cycle Time	12		15		ns
t_{RAC}[1]	Row Enable Access Time, On a Cache Miss		30		35	ns
t_{RAC1}[1]	Row Enable Access Time, On a Cache Hit (Limit Becomes t_{AC})		15		17	ns
t_{RAC2}[1,6]	Row Enable Access Time for a Cache Write Hit		30		35	ns
t_{RAH}	Row Address Hold Time	1		1.5		ns
t_{RE}	Row Enable Active Time	30	100000	35	100000	ns

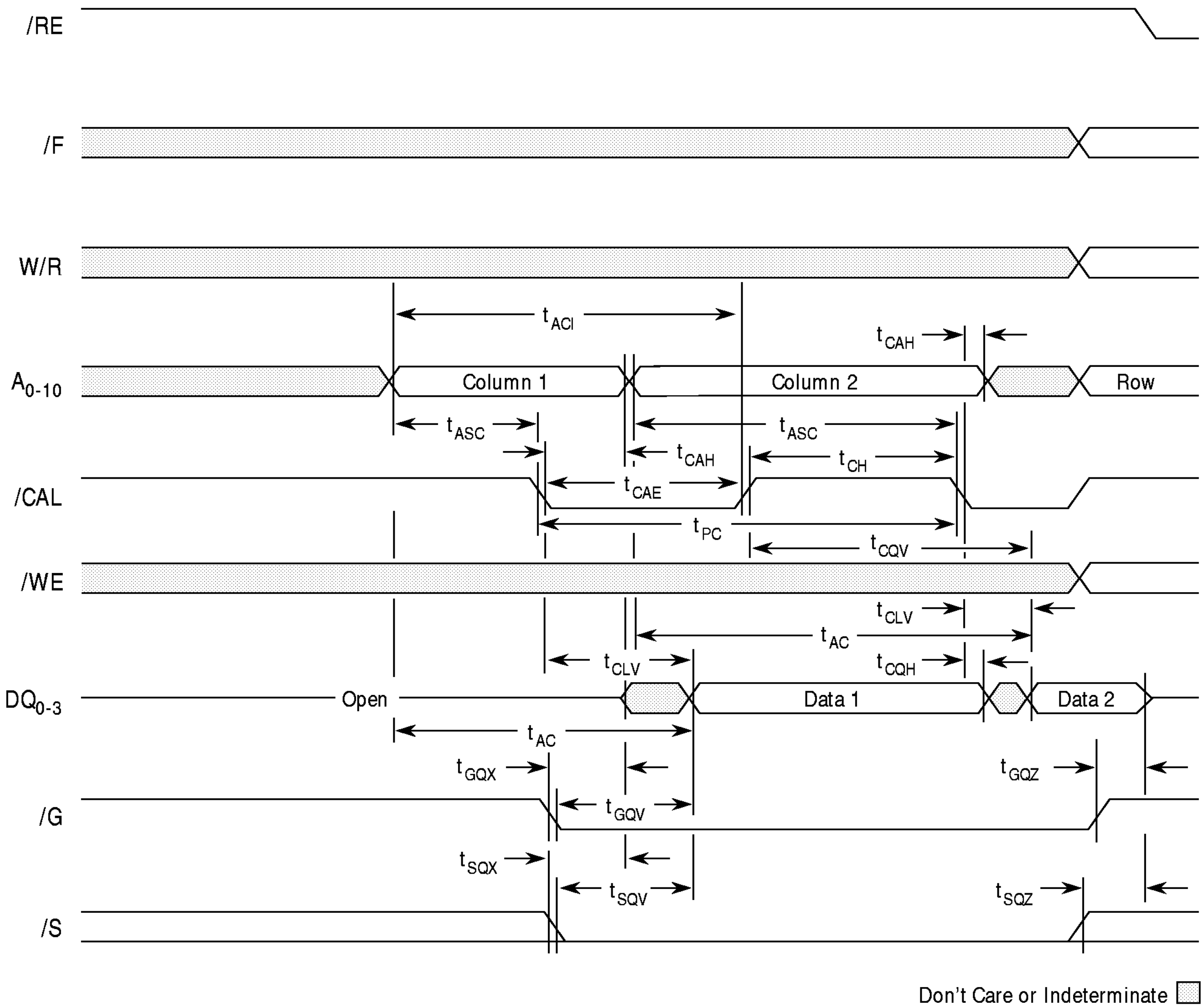
Switching Characteristics (continued)

V_{CC} = 5V ± 5% (+5 Volt Option), V_{CC} = 3.3V ± 0.3V (+3.3 Volt Option), C_L = 50pf, T_A = 0 to 70°C (Commercial), -40 to 85°C (Industrial)

Symbol	Description	-12 Min	-12 Max	-15 Min	-15 Max	Units
t_{RE1}	Row Enable Active Time, Cache Hit (Row=LRR) Read Cycle	8		10		ns
t_{REF}	Refresh Period		64		64	ms
t_{RGX}	Output Enable Don't Care From Row Enable (Write, Cache Miss), O/P Hi Z	9		10		ns
t_{RQX1} (2,6)	Row Enable High to Output Turn-On After Write Miss	0	12	0	15	ns
t_{RP} (7)	Row Precharge Time	20		25		ns
t_{RP1}	Row Precharge Time, Cache Hit (Row=LRR) Read Cycle	8		10		ns
t_{RP2}	Row Precharge Time, Self-Refresh Mode	100		100		ns
t_{RRH}	Read Hold Time From Row Enable (Write Only)	0		0		ns
t_{RSH}	Last Write Address Latch to End of Write	12		15		ns
t_{RSW}	Row Enable to Column Address Latch Low For Second Write	35		40		ns
t_{RWL}	Last Write Enable to End of Write	12		15		ns
t_{SC}	Column Address Cycle Time	12		15		ns
t_{SHR}	Select Hold From Row Enable	0		0		ns
t_{SQV} (1)	Chip Select Access Time		12		15	ns
t_{SQX} (2,3)	Output Turn-On From Select Low	0	12	0	15	ns
t_{SQZ} (4,5)	Output Turn-Off From Chip Select	0	8	0	10	ns
t_{SSR}	Select Setup Time to Row Enable	5		5		ns
t_T	Transition Time (Rise and Fall)	1	10	1	10	ns
t_{WC}	Write Enable Cycle Time	12		15		ns
t_{WCH}	Column Address Latch Low to Write Enable Inactive Time	5		5		ns
t_{WHR} (7)	Write Enable Hold After /RE	0		0		ns
t_{WI}	Write Enable Inactive Time	5		5		ns
t_{WP}	Write Enable Active Time	5		5		ns
t_{WQV} (1)	Data Valid From Write Enable High		12		15	ns
t_{WQX} (2,5)	Data Output Turn-On From Write Enable High	0	12	0	15	ns
t_{WQZ} (3,4)	Data Turn-Off From Write Enable Low	0	12	0	15	ns
t_{WRP}	Write Enable Setup Time to Row Enable	5		5		ns
t_{WRR}	Write to Read Recovery (Following Write Miss)		16		18	ns

(1) V_{OUT} Timing Reference Point at 1.5V
(2) Parameter Defines Time When Output is Enabled (Sourcing or Sinking Current) and is Not Referenced to V_{OH} or V_{OL}
(3) Minimum Specification is Referenced from V_{IH} and Maximum Specification is Referenced from V_{IL} on Input Control Signal
(4) Parameter Defines Time When Output Achieves Open-Circuit Condition and is Not Referenced to V_{OH} or V_{OL}
(5) Minimum Specification is Referenced from V_{IL} and Maximum Specification is Referenced from V_{IH} on Input Control Signal
(6) Access Parameter Applies When /CAL Has Not Been Asserted Prior to t_{RAC2}
(7) For Write-Per-Bit Devices, t_{WHR} is Limited By Data Input Setup Time, t_{DS}

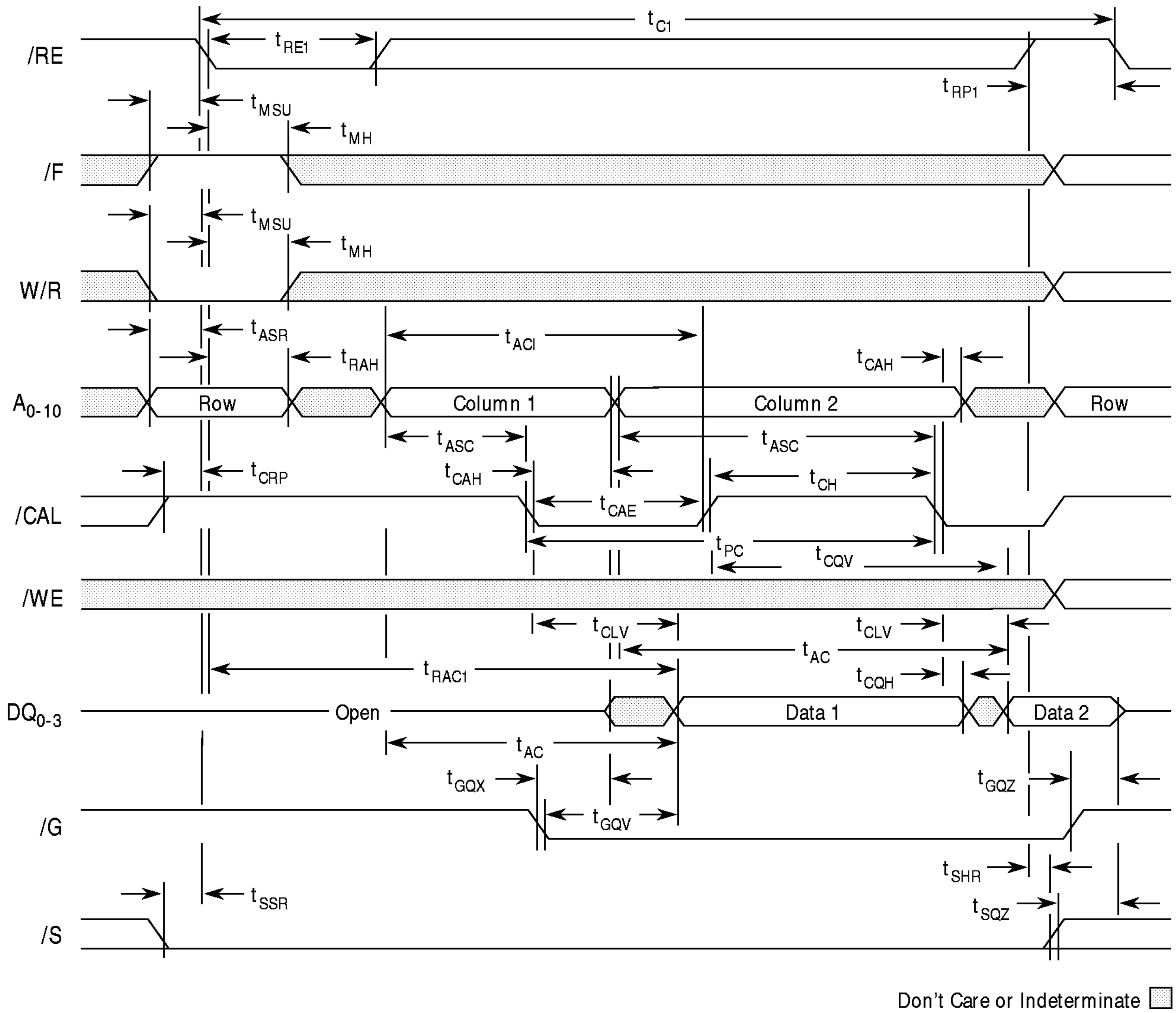
/RE Inactive Cache Read Hit (EDO Mode)



Notes: 1. Data accessed during /RE inactive read is from the row address specified during the last /RE active read cycle.

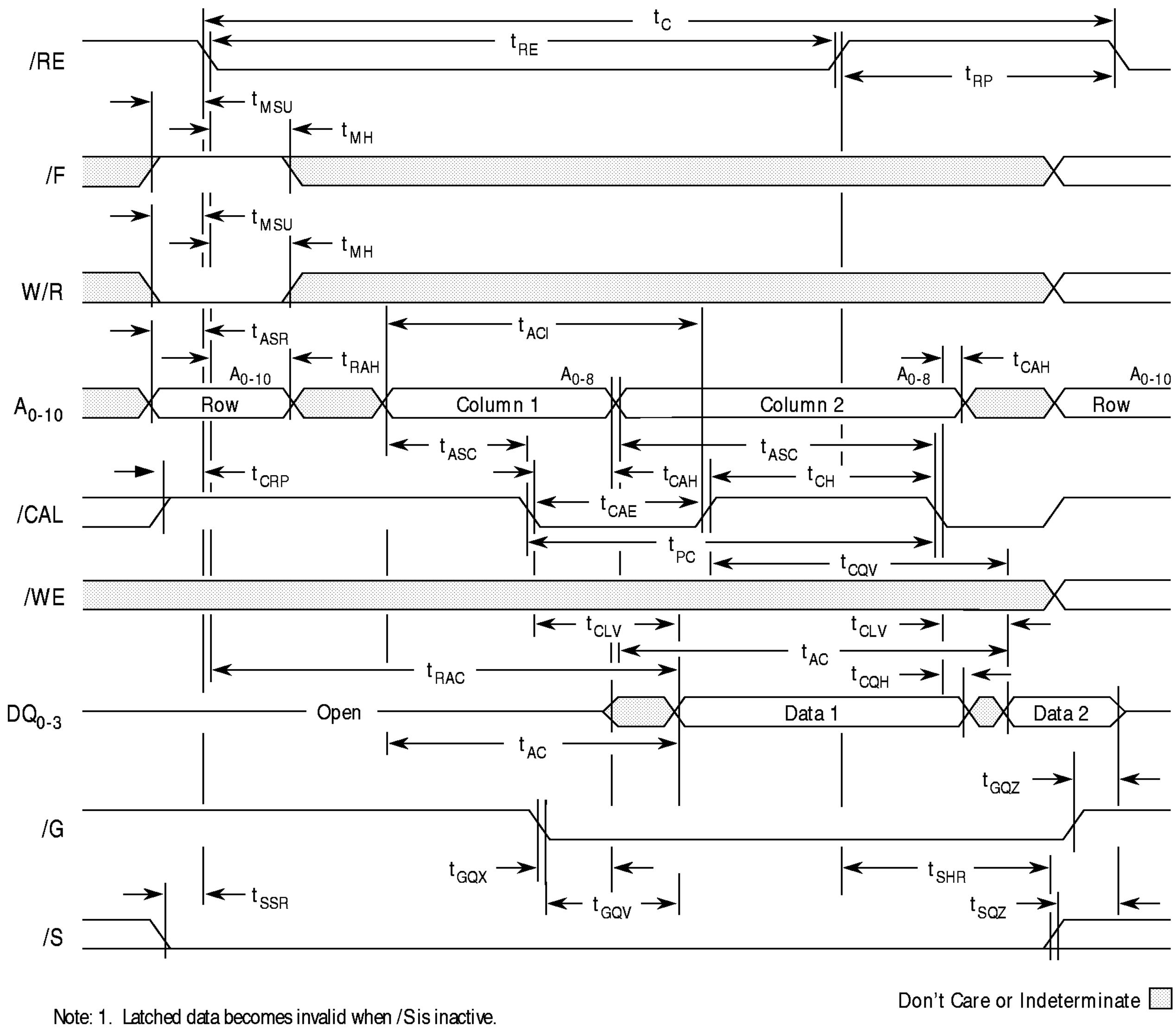
2. Latched data becomes invalid when /S is inactive.

/RE Active Cache Read Hit



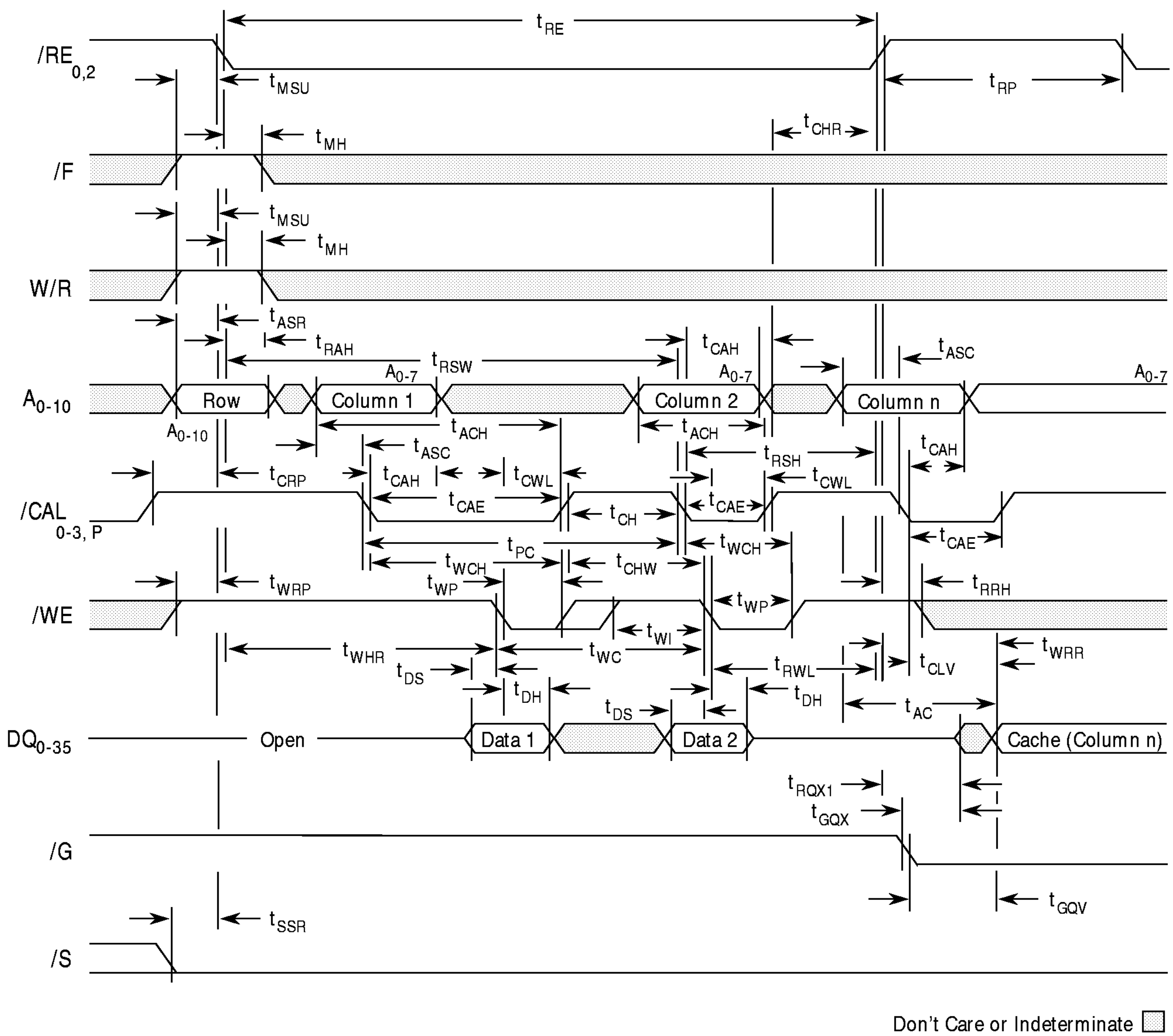
Note: 1. Latched data becomes invalid when /S is inactive.

/RE Active Cache Read Miss



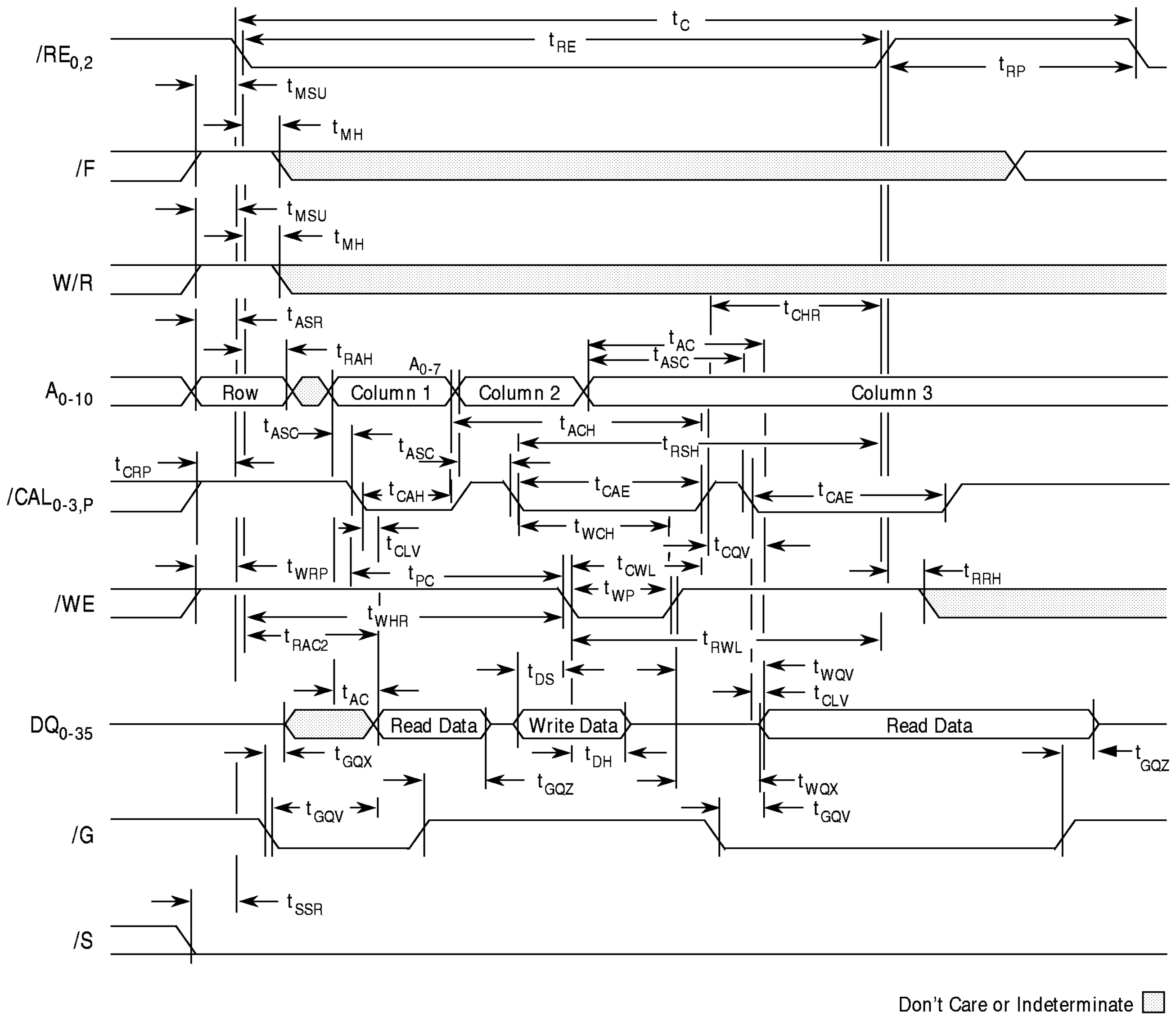
Note: 1. Latched data becomes invalid when /S is inactive.

Burst Write (Hit or Miss) Followed By /RE Inactive Cache Reads



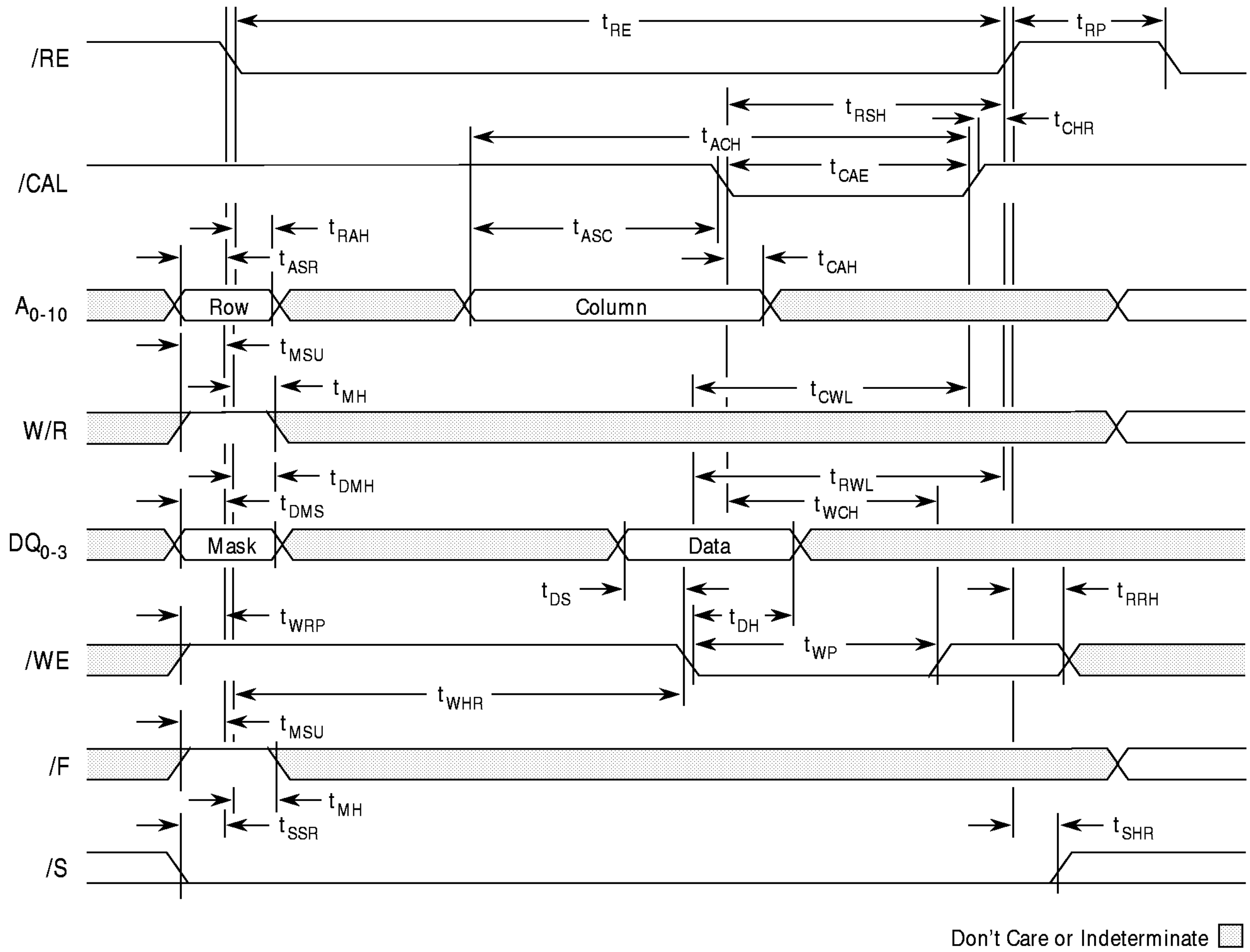
NOTES: 1. /G becomes a don't care after t_{RGX} during a write miss.

Read/Write During Write Hit Cycle (Can Include Read-Modify-Write)



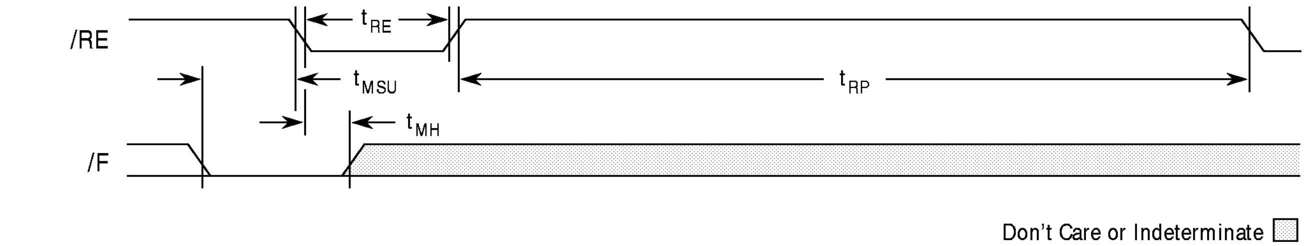
NOTES: 1. If column address one equals column address two, then a read-modify-write cycle is performed.

Write-Per-Bit Cycle (/G=High)



NOTES: 1. Data mask bit high (1) enables bit write; data mask bit low (0) inhibits bit write.
2. Write-per-bit cycle valid only for DM2252.

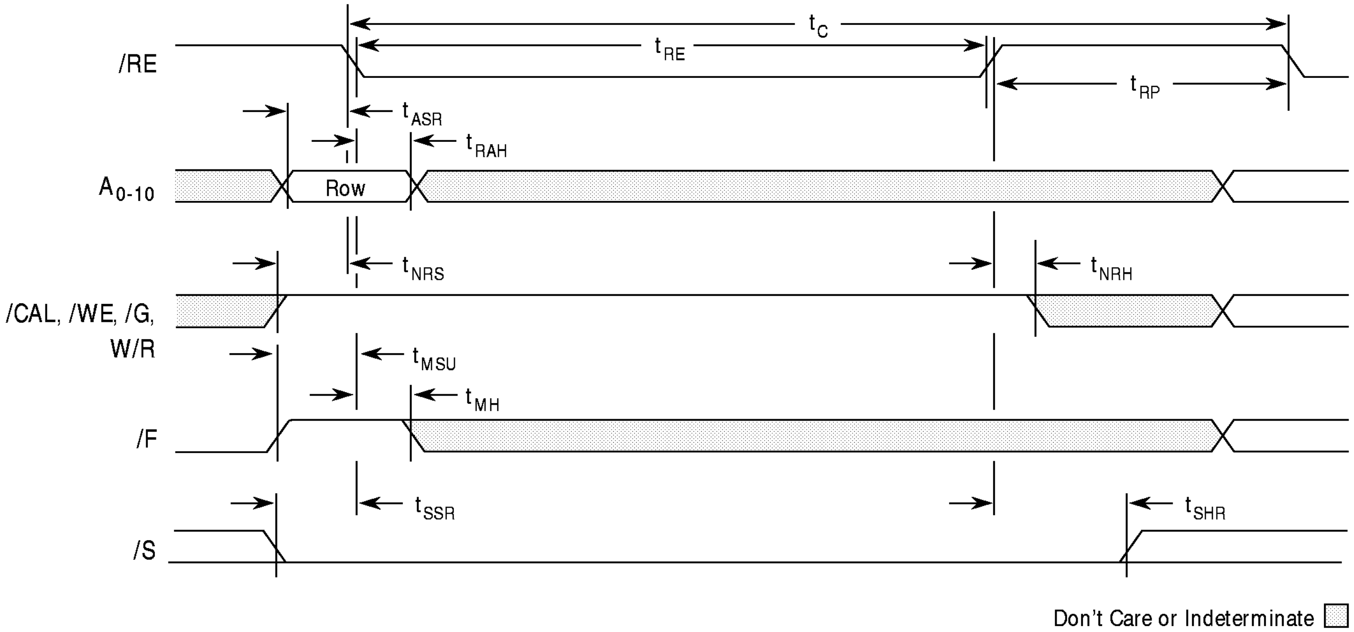
/F Refresh Cycle



NOTES: 1. During /F refresh cycles, the status of W/R, /WE, $A_{0\text{-}10}$, /CAL, /S, and /G is a don't care.

2. /RE inactive cache reads may be performed in parallel with /F refresh cycles.

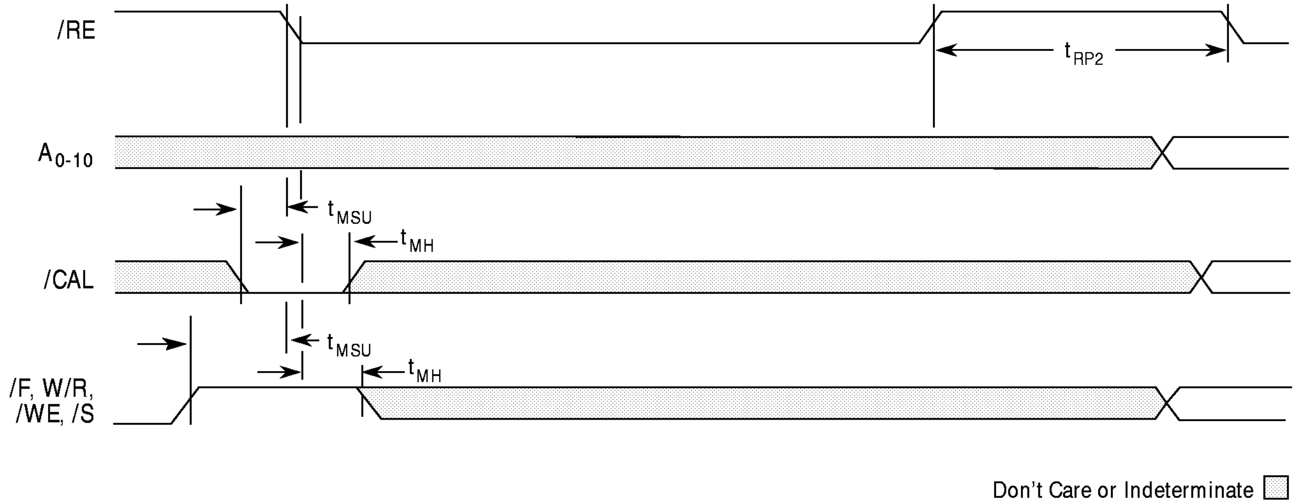
/RE-Only Refresh



NOTES: 1. All binary combinations of $A_{0\text{-}9}$ must be refreshed every 64ms interval. A_{10} does not have to be cycled, but must remain valid during row address setup and hold times.

2. /RE refresh is write cycle with no /CAL active cycle.

Low Power Self-Refresh Mode Option



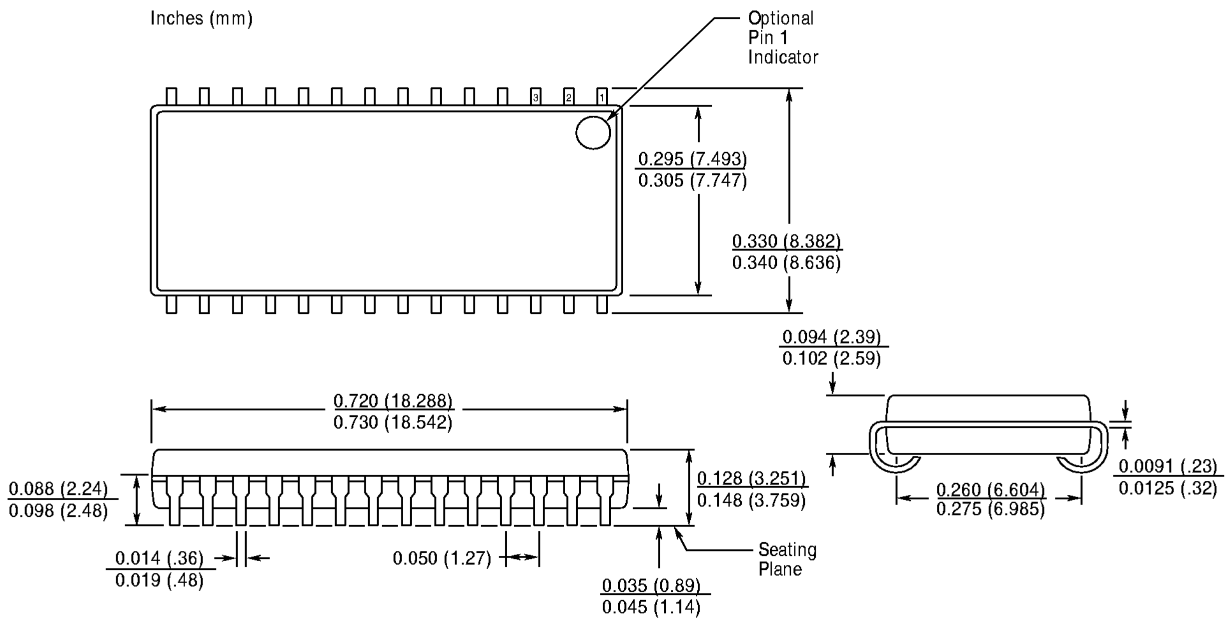
NOTES: 1. EDRAM self refreshes as long as /RE remains low. (Low Power Self Refresh part only).
2. When using the Low Power Self Refresh mode the following operations must be performed:
If row addresses are being refreshed in an *evenly distributed* manner over the refresh interval using /F refresh cycles, then at least one /F refresh cycle must be performed immediately after exit from the Low Power Self Refesh Mode. If row addresses are being refreshed in any other manner (/F burst or /RE distributed or burst), then all rows must be refreshed immediately befor entry to and immediately after exit from the Low Power Self Refresh.

Part Numbering System

DM2242J 2 - 12I

- Temperature Range
  - No Designator = 0 to 70°C (Commercial)
  - I = -40 to +85°C (Industrial)
  - L = 0 to 70°C, Low Power Self-Refresh
- Access Time from Cache in Nanoseconds
  - 12ns
  - 15ns
- Configuration
  - 2 = +5 Volts, EDO
  - 3 = +3.3 Volts, EDO
- Packaging System
  - J = 300 Mil, Plastic SOJ
  - T = 300 Mil, Plastic TSOP-II
- I/O Width
  - i.e., Power to Which 2 is Raised for I/O Width (x4)
- Special Feature Field
  - 4= No Write-Per-Bit
  - 5= Write-Per-Bit
- Capacity in Bits
  - i.e., Power to Which 2 is Raised for Total Capacity (4Mbit)
- Dynamic Memory

Mechanical Data
28 Pin 300 Mil Plastic SOJ Package



Mechanical Data
44 Pin 300 Mil Plastic TSOP-II Package