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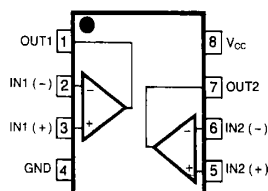
DUAL OPERATIONAL AMPLIFIERS

The NE5532 is an internally compensated dual low noise op AMP. The high small signal and power bandwidths provides superior performance in high quality AMP, all control circuits, and telephone applications.

FEATURE

- Internal frequency compensation
- Slew Rate: 8V/ μ s
- Input noise voltage: 8nV/ $\sqrt{\text{Hz}}$ ($f_o = 30\text{Hz}$)
- Full power bandwidth: 140KHz

BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operating Temperature
NE5532	8 DIP	0 ~ + 70 °C

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Characteristics	Symbol	NE5532	Unit
Power Supply Voltage	V_{CC}	± 22	V
Differential Input Voltage	V_{IO}	13	V
Input Voltage	V_I	Supply Voltage	V
Power Dissipation	P_D	1000	mW
Operating Temperature Range	T_{OPR}	0 ~ + 70	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = -5\text{V}$, $V_{EE} = -15\text{V}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}			0.5	4.0	mV
Input Offset Current	I_{IO}			10	150	nA
Input Bias Current	I_{BIAS}			200	800	nA
Supply Current	I_{CC}			6.0	16	mA
Input Voltage Range	$V_{I(R)}$		± 12	± 13		V
Common Mode Rejection Range	CMRR	$T_A = 25^\circ\text{C}$	70	100		dB
Power Supply Rejection Ratio	PSRR	$T_A = 25^\circ\text{C}$	80	100		dB
Output Voltage Swing	$V_{O(P,P)}$	$R_L \geq 600\Omega$	± 12	± 13		V
Input Resistance	R_I	$T_A = 25^\circ\text{C}$	30	300		K Ω
Short Circuit Current	I_{SC}			38		mA
Overshoot	O_S	$R_L = 600\Omega$, $C_L = 100\text{pF}$		10	20	%
Gain	G_V	$f = 10\text{KHz}$	2	2.2		V/mV
Gain Bandwidth Product	GBW	$C_L = 100\text{pF}$, $R_L = 600\Omega$	8	10		MHz
Slew Rate	SR	$R_L = 1\text{K}$, $C_L = 100\text{pF}$, $R_L = 600\Omega$	6	8.0		V/ μ s
Input Noise Voltage	V_{NI}	$f_o = 30\text{Hz}$ $f_o = 1\text{KHz}$		8.0 5.0		nV/ $\sqrt{\text{Hz}}$

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 Open Loop Frequency Response

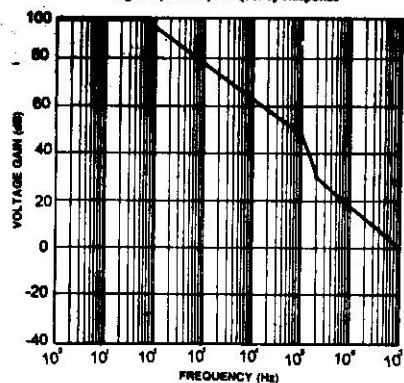


Fig. 2 Large Signal Frequency Response

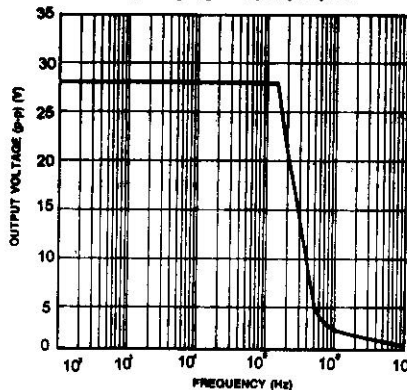


Fig. 3 Supply Current

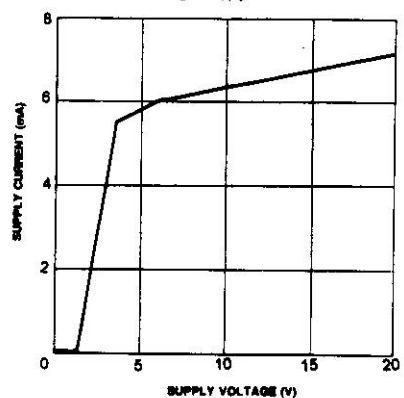


Fig. 4 Input Bias Current

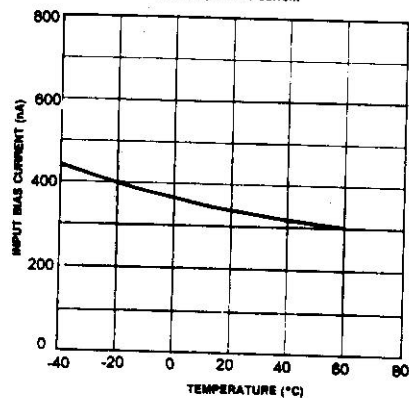


Fig. 5 Output Circuit Current

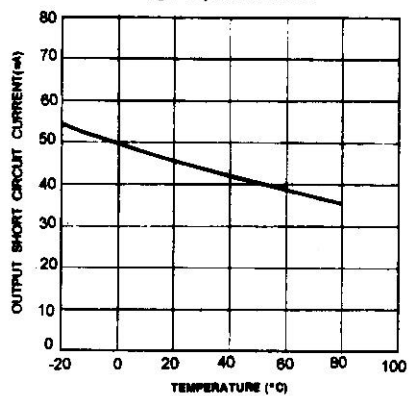
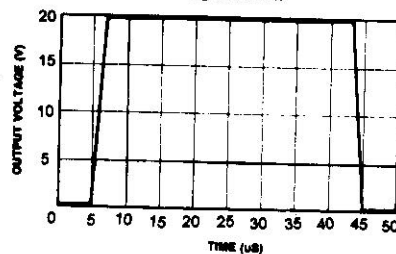


Fig. 6 Slew Rate



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FACT™	QS™
FACT Quiet Series™	Quiet Series™
FAST®	SuperSOT™-3
FASTr™	SuperSOT™-6
GTO™	SuperSOT™-8
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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

SINGLE TIMER

The NE555/1 is a highly stable controller capable of producing accurate timing pulses. With monostable operation, the time delay is controlled by one external resistor and one capacitor. With astable operation, the frequency and duty cycle are accurately controlled with two external resistors and one capacitor.

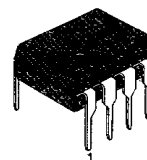
FEATURES

- High Current Drive Capability (= 200mA)
- Adjustable Duty Cycle
- Temperature Stability of 0.005%/°C
- Timing From μSec To Hours
- Turn Off Time Less Than 2 μSec

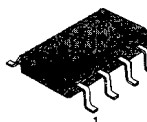
APPLICATIONS

- Precision Timing
- Pulse Generation
- Time Delay Generation
- Sequential Timing

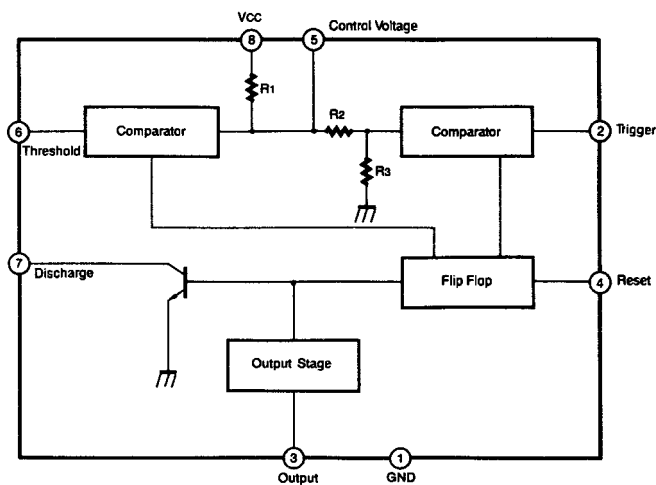
8 DIP



8 SOP

**ORDERING INFORMATION**

Device	Package	Operating Temperature
NE555N	8 DIP	0 ~ +70°C
NE555M	8 SOP	
NE555IN	8 DIP	-40 ~ +85°C
NE555IM	8 SOP	

BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Lead Temperature (soldering 10sec)	T_{LEAD}	300	$^\circ\text{C}$
Power Dissipation	P_D	600	mW
Operating Temperature Range NE555C NE555CI	T_{OPR}	0 ~ + 70 - 40 ~ + 85	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	- 65 ~ + 150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS($T_A = 25^\circ\text{C}$, $V_{CC} = 5 \sim 15\text{V}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		4.5		16	V
Supply Current	I_{CC}	$V_{CC} = 5\text{V}$, $R_L = \infty$		3	6	mA
* ¹ (low stable)		$V_{CC} = 15\text{V}$, $R_L = \infty$		7.5	15	mA
*Timing Error (Monostable)	ACCUR	$R_A = 1\text{K}\Omega$ to 100K Ω $C = 0.1\mu\text{F}$				% ppm/ $^\circ\text{C}$ %/V
² Initial Accuracy				1.0	3.0	
Drift with Temperature				50		
Drift with Supply Voltage				0.1	0.5	
*Timing Error (astable)	ACCUR	$R_A = 1\text{K}\Omega$ to 100K Ω $C = 0.1\mu\text{F}$				% ppm/ $^\circ\text{C}$ %/V
² Initial Accuracy				2.25		
Drift with Temperature				150		
Drift with Supply Voltage				0.3		
Control Voltage	V_C	$V_{CC} = 15\text{V}$	9.0	10.0	11.0	V
		$V_{CC} = 5\text{V}$	2.6	3.33	4.0	V
Threshold Voltage	V_{TH}	$V_{CC} = 15\text{V}$		10.0		V
		$V_{CC} = 5\text{V}$		3.33		V
* ³ Threshold Current	I_{TH}			0.1	0.25	μA
Trigger Voltage	V_{TR}	$V_{CC} = 5\text{V}$	1.1	1.67	2.2	V
Trigger Voltage	V_{TR}	$V_{CC} = 15\text{V}$	4.5	5	5.6	V
Trigger Current	I_{TR}	$V_{TR} = 0\text{V}$		0.01	2.0	μA
Reset Voltage	V_{RST}		0.4	0.7	1.0	V
Reset Current	I_{RST}			0.1	0.4	mA

SINGLE TIMER

(T_A = 25°C, V_{CC} = 5 ~ 15V, unless otherwise specified)

Notes:

1. Supply current when output is high is typically 1mA less at $V_{CC} = 5V$
2. Tested at $V_{CC} = 5.0V$ and $V_{CC} = 15V$
3. This will determine maximum value of $R_A + R_B$ for 15V operation, the max. total $R = 20M\Omega$, and for 5V operation the max. total $R = 6.7M\Omega$

The circuit diagram shows a 555 timer configured as a monostable multivibrator. The pins are connected as follows:

- Pin 1 (GND):** Connected to ground.
- Pin 2 (TRIGGER):** Connected to pin 6 (THRESHOLD) through capacitor C₁.
- Pin 3 (Output):** Labeled "Output".
- Pin 4 (Reset):** Connected to VCC through resistor R_A.
- Pin 5 (THRESHOLD):** Connected to VCC through resistor R_B. It also has a network consisting of a series combination of resistors R₁, R₂, and R₃ connected to GND. A junction between R₁ and R₂ is connected to the non-inverting input of the upper comparator.
- Pin 6 (THRESHOLD):** Connected to pin 2 through capacitor C₁.
- Pin 7 (DISCHARGE):** Connected to VCC through resistor R_A. It also has a network consisting of a series combination of resistors R₁, R₂, and R₃ connected to GND. A junction between R₁ and R₂ is connected to the inverting input of the lower comparator. Additionally, there is a branch from pin 7 through a switch Q₁ to GND.
- Pin 8 (VCC):** Connected to VCC.

The internal components include two comparators (labeled "Low comparator" and "Upper comparator"), a flip-flop (labeled "Flip-Flop"), and several resistors (R₁, R₂, R₃, R_A, R_B) and a capacitor (C₁). The output of the flip-flop is connected to pin 3.

APPLICATION NOTE

The application circuit shows astable mode.

Pin 6 (threshold) is tied to Pin 2 (trigger) and Pin 4 (reset) is tied to V_{CC} (Pin 8).

The external capacitor C_1 of Pin 6 and Pin 2 charges through R_A , R_B and discharges through R_B only.

In the internal circuit of the NE555 one input of the upper comparator is the $2/3 V_{CC}$ ($R_1 = R_2 = R_3$, another input if it is connected Pin 6).

As soon as charging C_1 is higher than $2/3 V_{CC}$, discharge transistor Q_1 turns on and C_1 discharges to collector of transistor Q_1 .

Therefore, the flip-flop circuit is reset and output is low.

One input of lower comparator is the $1/3 V_{CC}$, discharge transistor Q_1 turn off and C_1 charges through R_A and R_B .

Therefore, the flip-flop circuit is set and output is high.

So to say, when C_1 charges through R_A and R_1 output is high and when C_1 discharges through R_B output is low.

The charge time (output is high) T_1 is $0.693 (R_A + R_B) C_1$ and the discharge time (output is low) T_2 is $0.693 (R_B C_1)$.

$$(I_n \frac{V_{CC}-1/3V_{CC}}{V_{CC}-2/3V_{CC}}) (0.693)$$

Thus the total period time T is given by

$$T = T_1 + T_2 = 0.693 (R_A + 2R_B) C_1.$$

Then the frequency of astable mode is given by

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C_1}$$

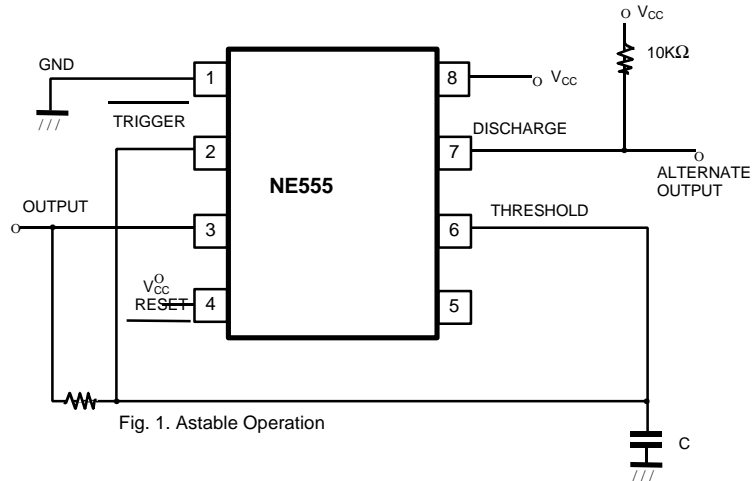
The duty cycle is given by

$$D.C = \frac{T_H}{T} = \frac{R_B}{R_A + 2R_B}$$

If you make use of the NE555 you can make two astable modes.

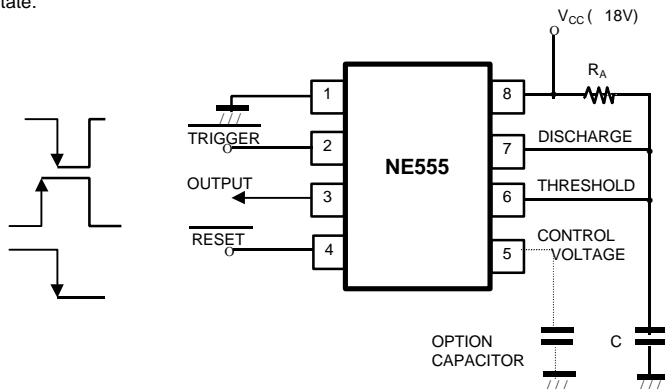
Astable Operation

The NE555 can free run as a multivibrator by triggering itself; refer to Fig.2. The output can swing from V_{DD} to GND and have 50% duty cycle square wave. Less than 1% frequency deviation can be observed, over a voltage range of 2 to 5V. $f = 1/1.4RC$



Monostable Operation

The NE555 can be used as a one-shot, i.e. monostable multivibrator. Initially, because the inside discharge transistor is on state, external timing capacitor is held to GND potential. Upon application of a negative TRIGGER pulse pin 2, the internal discharge transistor is off state and the voltage across the capacitor increases with time constant $T = R_A C$ and OUTPUT goes to high state. When the voltage across the capacitor equals $2/3 V_{CC}$ the inner comparator is reset by THRESHOLD input and the discharge transistor goes to on state, which in turn discharges the capacitor rapidly and drives the OUTPUT to its low state.



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