mosaic

Mosaic Semiconductor Inc.

32K x 32 SRAM

PUMA 2S1010-030/35/45/55/70

Issue 2.0 : May 1992

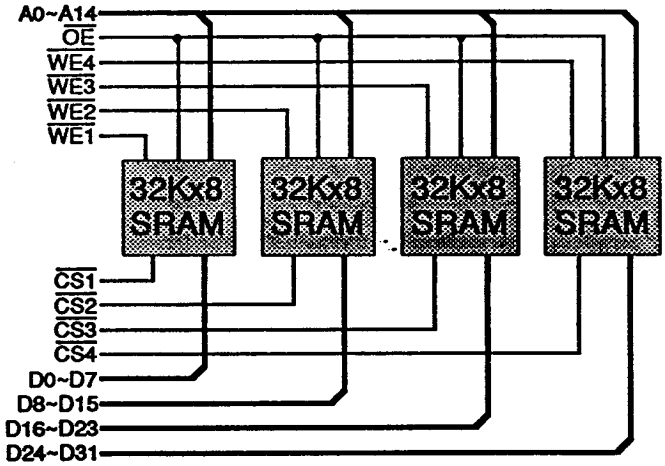
PRELIMINARY

1,048,576 bit CMOS High Speed Static RAM

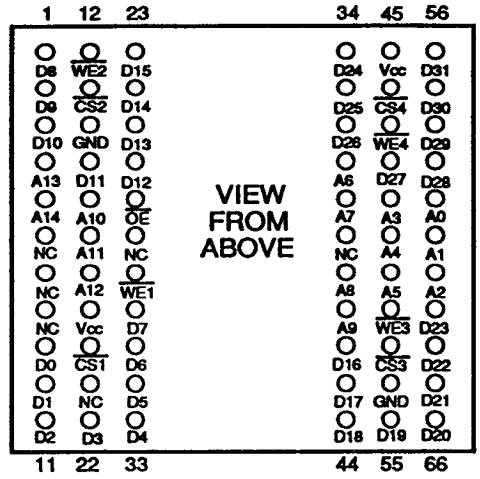
Features

Ultra Fast access times of 30/35/45/55/70 ns.
Configurable as 32 / 16 / 8 bit wide output.
Operating Power 2640 / 1375 / 770 mW (maximum)
Standby Power 11 mW (maximum)
Pin grid array gives 2:1 improvement over DIL.
Package Suitable for Thermal Ladder Applications.
On board decoupling capacitors.
Battery back-up capability.
May be processed to MIL-STD-883, method 5004 non-compliant.

Block Diagram



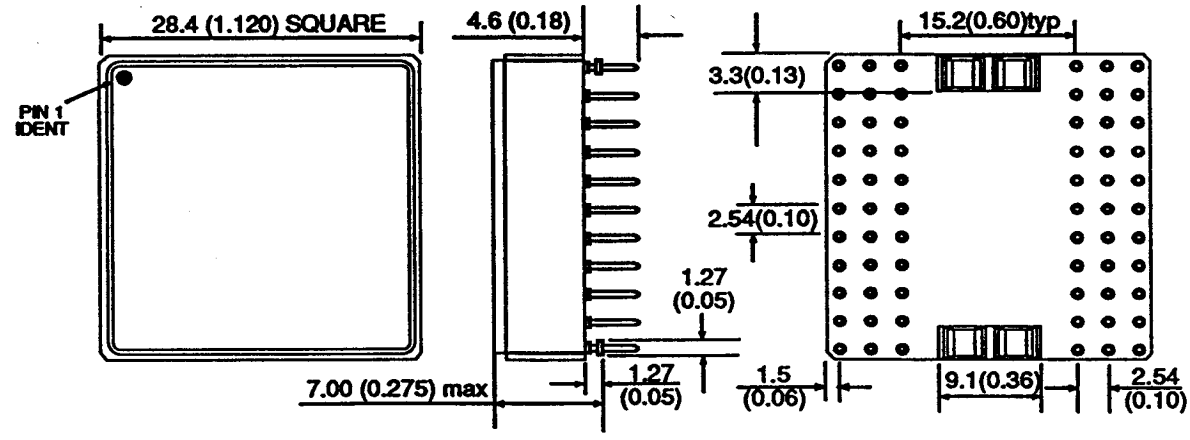
Pin Definition



Pin Functions

A0 -A14	Address Inputs
D0-D31	Data Inputs/Outputs
$\overline{CS1\text{-}4}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE1\text{-}4}$	Write Enable
NC	No Connect
V_{cc}	Power (+5V)
GND	Ground

Package Details Dimensions in mm (inches).



Absolute Maximum Ratings (1)

Voltage on any pin relative to V_{SS} (2)	V_T	-0.5V to +7	V
Power Dissipation	P_T	1	W
Storage Temperature	T_{STG}	-55 to +150	°C

Notes (1) Stresses above those listed may cause permanent damage to the module. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Pulse width:- 2.5V for less than 10ns.

Recommended Operating Conditions

		min	*typ*	*max*	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	-0.5	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AL}	-40	-	85	°C (suffix I)
	T_{AM}	-55	-	125	°C (suffix M, MB)

DC Electrical Characteristics (V_{CC} = 5V±10%, T_A = -55°C to +125°C)

Parameter		*Symbol*	*Test Condition*	*030/35 min*	*030/35 max*	*45/55/70 min*	*45/55/70 max*	*Unit*
I/P Leakage Current	A0~14, $\overline{OE}$	I_{LI1}	V_{IN}=0V to V_{CC}	-	8	-	8	µA
	$\overline{WE}$(2), $\overline{CS}$(2)	I_{LI2}	V_{IN} = 0V to V_{CC}	-	2	-	2	µA
Output Leakage Current	32 bit	I_{LO}	$\overline{CS}$(2) = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0V to V_{CC}	-	2	-	2	µA
Operating Supply Current	32 bit	I	$\overline{CS}$(2)=V_{IL}, inputs static	-	250	-	250	mA
Average Supply Current	32 bit	I_{CC32}	$\overline{CS}$(2) = V_{IL}, Min. cycle, $I_{I/O}$ = 0mA	-	480	-	380	mA
	16 bit	I_{CC16}	As above	-	250	-	200	mA
	8 bit	I_{CC8}	As above	-	140	-	115	mA
Standby Supply Current	TTL	I_{SB}	$\overline{CS}$(2)=V_{IH}, minimum cycle.	-	30	-	30	mA
	CMOS	I_{SB1}	$\overline{CS}$(2) ≥ V_{CC}-0.2V, 0.2V ≥ V_{IN} ≥ V_{CC}-0.2V	-	2	-	2	mA
Output Voltage Low		V_{OL}	I_{OL} = 8.0mA	-	0.4	-	0.4	V
Output Voltage High		V_{OH}	I_{OH} = -4.0mA	2.4	-	2.4	-	V

Notes (1) Typical values are at V_{CC} = 5.0V, T_A = 25°C and specified loading.

(2) $\overline{CS}$ and $\overline{WE}$ above are accessed through $\overline{CS1\text{-}4}$ and $\overline{WE1\text{-}4}$ respectively. These inputs must be operated simultaneously for 32 bit mode, in pairs for 16 bit mode and singly for 8 bit mode.

Capacitance (V_{CC}=5V±10%, T_A=25°C)

Parameter		*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance	Address, $\overline{OE}$	C_{IN1}	V_{IN}=0V	-	34	pF
	$\overline{WE1\text{-}4}$, $\overline{CS1\text{-}4}$	C_{IN2}	V_{IN}=0V	-	22	pF
I/O Capacitance:	32 bit mode	$C_{I/O32}$	$V_{I/O}$=0V	-	17	pF
	16 bit mode	$C_{I/O16}$	$V_{I/O}$=0V	-	24	pF
	8 bit mode	$C_{I/O8}$	$V_{I/O}$=0V	-	38	pF

Note: This parameter is calculated and not measured.

Operating Modes

The Table below shows the logic inputs required to control the operating modes of each of the SRAMs on the PUMA 2S1010.

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	*V_{CC} Current*	*I/O Pin*	*Reference Cycle*
Not Selected	1	X	X	I_{SB},I_{SB1}	High Z	-
Read	0	0	1	I_{CC}	D_{OUT}	Read Cycle 1,2,3
Write	0	1	0	I_{CC}	D_{IN}	Write Cycle 1
Write	0	0	0	I_{CC}	D_{IN}	Write Cycle 2

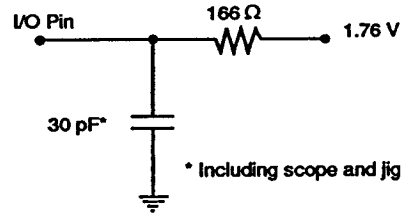
$1 = V_{IH}$, $0 = V_{IL}$, X = Don't Care

Note: $\overline{CS}$ is accessed through $\overline{CS1\text{-}4}$, and $\overline{WE}$ is accessed through $\overline{WE1\text{-}4}$. For correct operation, $\overline{CS1\text{-}4}$ must operate simultaneously for 32 bit operation, in pairs for 16 bit operation, or singly for 8 bit operation. $\overline{WE1\text{-}4}$ must also be operated in the same manner.

AC Test Conditions

* Input pulse levels: 0V to 3.0V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: see diagram
* V_{CC}=5V±10%
* Module is tested in 32 bit mode.

Output Load



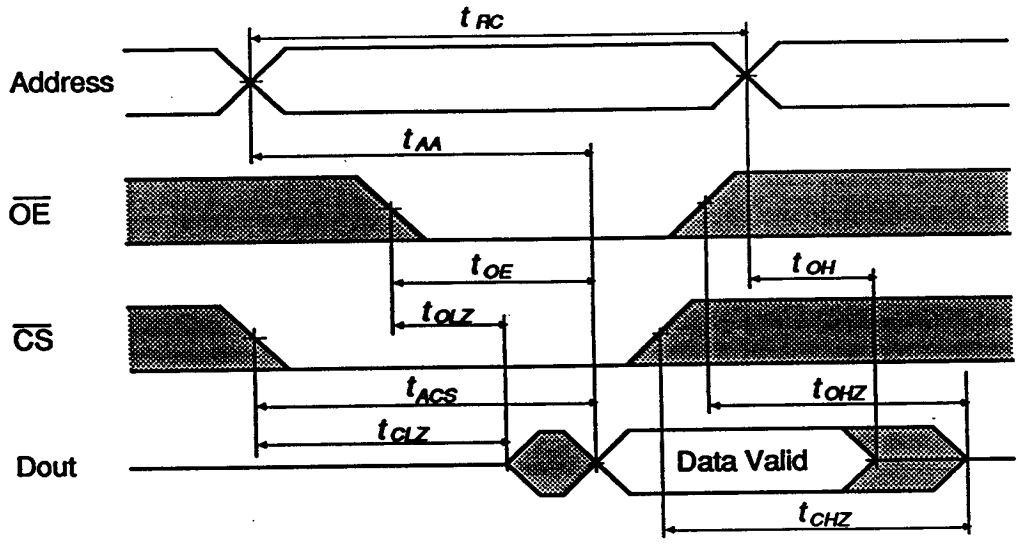
Electrical Characteristics & Recommended AC Operating Conditions

Read Cycle

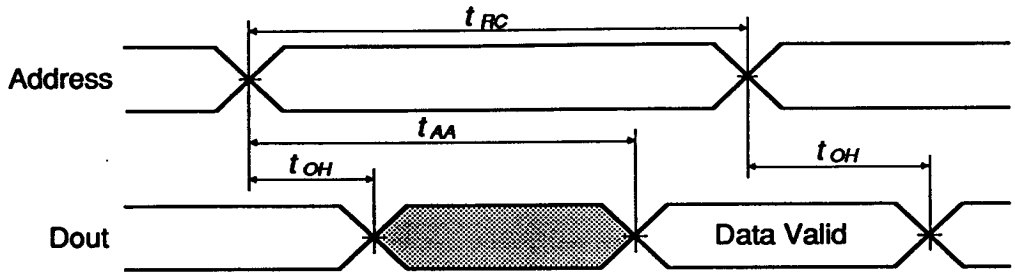
Parameter	Symbol	-30 min	-30 max	-35 min	-35 max	Unit
Read Cycle Time	t_{RC}	30	-	35	-	ns
Address Access Time	t_{AA}	-	30	-	35	ns
Chip Select Access Time	t_{ACS}	-	30	-	35	ns
Output Enable to Output Valid	t_{OE}	-	12	-	15	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	ns
Chip Selection to Output in Low Z[5]	t_{CLZ}	3	-	3	-	ns
Output Enable to Output in Low Z[5]	t_{OLZ}	0	-	0	-	ns
Chip Deselection to Output in High Z[5]	t_{CHZ}	0	12	0	15	ns
Output Disable to Output in High Z[5]	t_{OHZ}	0	12	0	15	ns

Parameter	Symbol	-45 min	-45 max	-55 min	-55 max	-70 min	-70 max	Unit
Read Cycle Time	t_{RC}	45	-	55	-	70	-	ns
Address Access Time	t_{AA}	-	45	-	55	-	70	ns
Chip Select Access Time	t_{ACS}	-	45	-	55	-	60	ns
Output Enable to Output Valid	t_{OE}	-	20	-	25	-	30	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns
Chip Selection to Output in Low Z[5]	t_{CLZ}	3	-	3	-	3	-	ns
Output Enable to Output in Low Z[5]	t_{OLZ}	0	-	0	-	0	-	ns
Chip Deselection to Output in High Z[5]	t_{CHZ}	0	20	0	25	0	30	ns
Output Disable to Output in High Z[5]	t_{OHZ}	0	20	0	25	0	30	ns

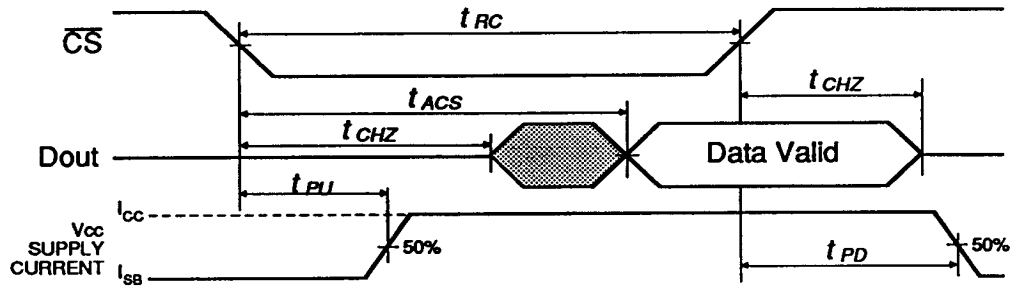
Read Cycle 1 Timing Waveform[1]



Read Cycle 2 Timing Waveform (1) (2) (4)

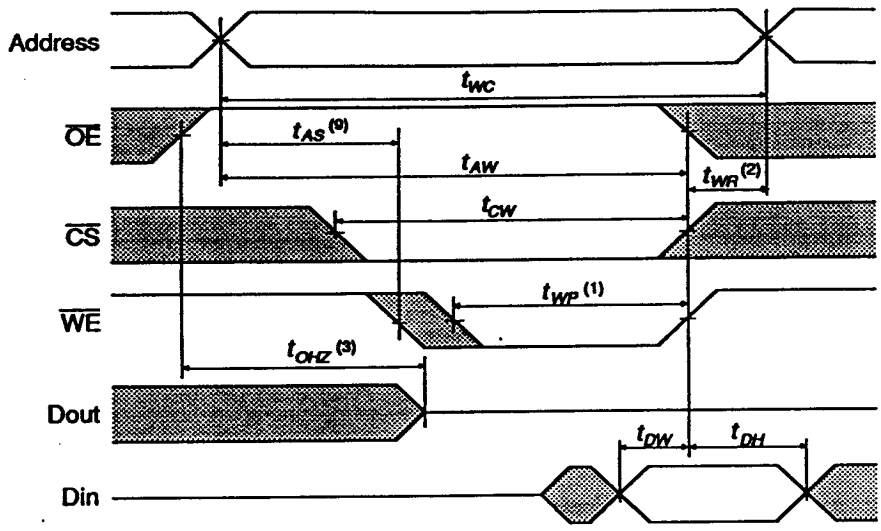


Read Cycle 3 Timing Waveform (1) (3) (4)

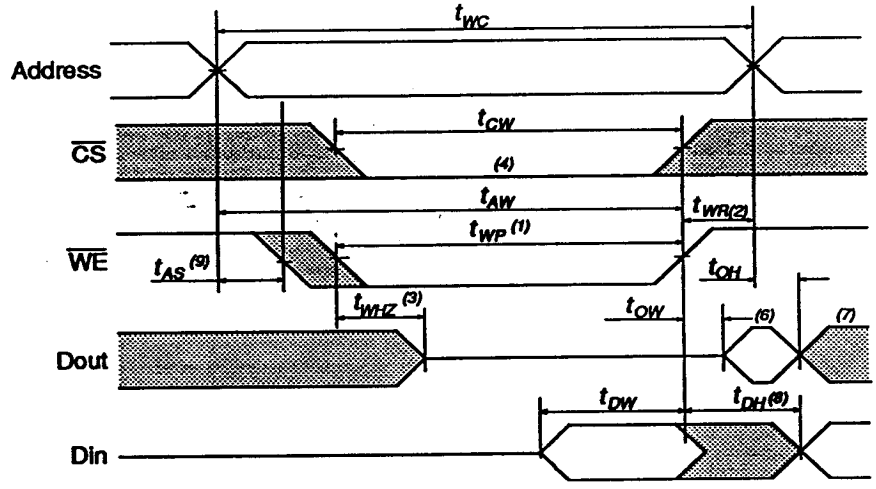


Notes: (1) $\overline{WE}$ is High for Read Cycle.
(2) Device is continuously selected, $\overline{CS}$=V_{IL}.
(3) Address valid prior to or coincident with $\overline{CS}$ transition Low.
(4) $\overline{OE}$=V_{IL}.
(5) t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

Write Cycle 1 Timing Waveform ($\overline{OE}$ Clock)



Write Cycle 2 Timing Waveform ($\overline{OE}$ Low Fixed)



AC Write Characteristics Notes

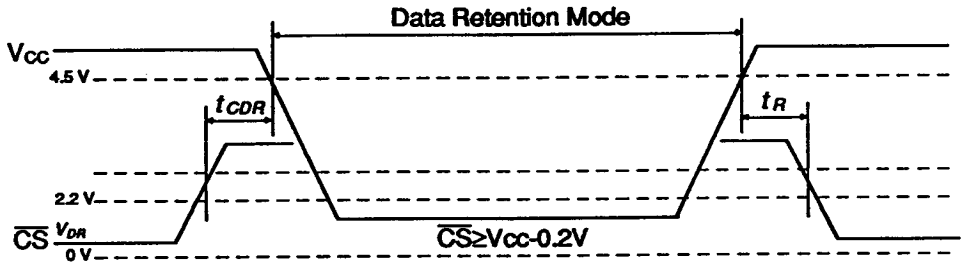
(1) A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
(2) t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
(3) During this period, I/O pins are in the output state. Input signals out of phase must not be applied.
(4) If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
(5) $\overline{OE}$ is continuously low. ($\overline{OE}$=V_{IL})
(6) Dout is in the same phase as written data of this write cycle.
(7) Dout is the read data of next address.
(8) If $\overline{CS}$ is low during this period, I/O pins are in the output state. Input signals out of phase must not be applied to I/O pins.
(9) $\overline{WE}$ must be high during all address transitions except when the device is deselected with $\overline{CS}$.
(10) t_{WHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

Low V_{cc} Data Retention Characteristics -L version only

Parameter	*Symbol*	*Test Condition*	*min*	*max*		*Unit*
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$-0.2V	2.0	-	-	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3.0V, $\overline{CS} \geq V_{CC}$-0.2V, $T_{OP} = T_A$	-	8	200	µA
	I_{CCDR2}	V_{CC} = 3.0V, $\overline{CS} \geq V_{CC}$-0.2V, $T_{OP} = T_{AI}$		TBA		µA
	I_{CCDR3}	V_{CC} = 3.0V, $\overline{CS} \geq V_{CC}$-0.2V, $T_{OP} = T_{AM}$	-	-	450	µA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	t_{RC}	-	-	ns

Notes (1) Typical figures measured at 25°C

Data Retention Waveform



Military Screening Procedure

MultiChip Screening Flow for high reliability non-compliant product pocessed to Mil-Std-883 Method 5004 shown below.

MB MULTICHIP MODULE SCREENING FLOW		
SCREEN	**TEST METHOD**	**LEVEL**
Visual and Mechanical		
Internal visual	2010 Condition B or manufacturers equivalent	100%
Temperature cycle	1010 Condition C (10 Cycles,-65°C to +150°C)	100%
Constant acceleration	2001 Condition B (Y_1 only) (10,000g)	100%
Burn-In		
Pre-Burn-in electrical	Per applicable device specifications at T_A=+25°C	100%
Burn-in	Method 1015,Condition D,T_A=+125°C,160hrs min	100%
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective allowable (PDA)	Calculated at post burn-in at T_A=+25°C	10%
Hermeticity	1014	
Fine	Condition A	100%
Gross	Condition C	100%
Quality Conformance	Per applicable Device Specification	Sample
External Visual	2009 Per vendor or customer specification	100%

Ordering Information

PUMA 2S1010LMB-030

- Speed
  - 030 = 30 ns
  - 35 = 35 ns
  - 45 = 45 ns
  - 55 = 55 ns
  - 70 = 70 ns
- Temp. range/screening
  - Blank = Commercial Temperature
  - I = Industrial Temperature
  - M = Military Temperature
  - MB = Processed to MIL-STD-883 non-compliant
- Power Consumption
  - Blank = Standard Power Part
  - L = Low Power Part
- Memory Organization
  - S1010 = 32K x 32 SRAM (Configurable as 64K x 16 and 128K x 8)

The policy of the company is one of continuous development and while the information presented in this data sheet is believed to be accurate, no liability is assumed for any data contained within. The company reserves the right to make changes without notice at any time.

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