SRM21256$_{45/55}$

CMOS 256K-BIT STATIC RAM

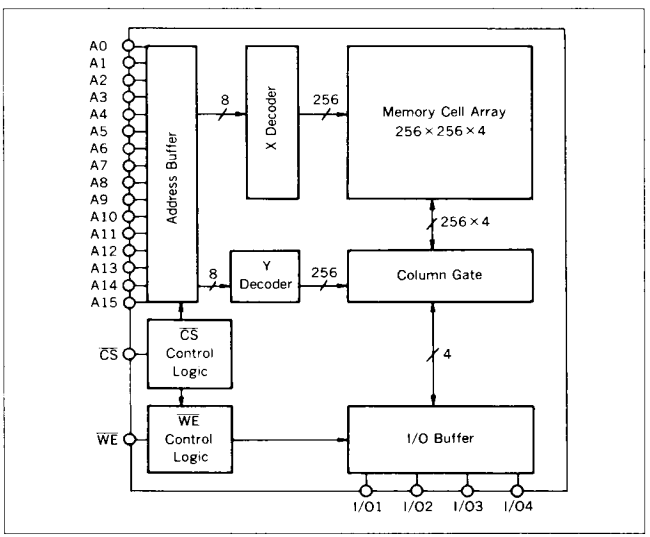
■ DESCRIPTION

The SRM21256$_{45/55}$ is a 65,536 word x 4 bits asynchronous, static, random access memory fabricated using an advanced CMOS technology. The asynchronous and static nature of the memory requires no external clock or refresh circuit. Input and output ports are TTL compatible and the three-state output allows easy expansion of memory capacity.

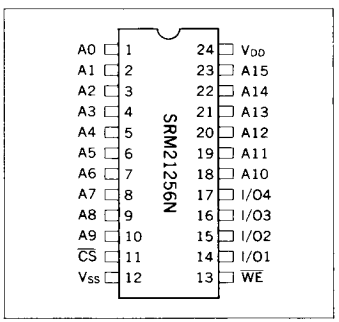
■ FEATURES

- Fast access time ..... SRM21256$_{45}$ 45ns (Max)
  SRM21256$_{55}$ 55ns (Max)
- Low supply current ..... Standby : 3mA (Typ)
  Operation: 120mA (Max)
- Completely static ..... No clock required
- Single power supply ..... 5V ± 10%
- TTL compatible inputs and outputs
- 3-state output
- Package ..... SRM20256N$_{45/55}$ 24-pin Skinny DIP
  (300 mil plastic package)

■BLOCK DIAGRAM



■PIN CONFIGURATION



■PIN DESCRIPTION

A0 to A15	Address Input
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O1 to 4	Data Input/Output
V_{DD}	Power Supply (+5V)
V_{SS}	Power Supply (0V)

■ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to 7.0	V
Input voltage	V_I	−0.5* to 7.0	V
Input/Output voltage	$V_{I/O}$	−0.5* to V_{DD}+0.3	V
Power dissipation	P_D	1.0	W
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (Lead only)	—

*V_I, $V_{I/O}$(Min)= −3.0V when pulse width is ≦20ns

■DC RECOMMENDED OPERATING CONDITIONS

(V_{SS}=0V, Ta=0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
	V_{SS}		0	0	0	V
Input voltage	V_{IH}		2.2	—	V_{DD}+0.3	V
	V_{IL}		−0.3*	—	0.8	V

*V_{IL}(Min)= −3.0V when pulse width is ≦20ns

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input leakage	I_{LI}	V_I=0 to V_{DD}	−1	—	1	μA
Standby supply current	I_{DDS}	$\overline{CS}$=V_{IH}	—	—	10	mA
	I_{DDS1}	$\overline{CS}$≧V_{DD}−0.2V	—	—	2	mA
Average operating current	I_{DDA}	V_I=V_{IL}, V_{IH} $I_{I/O}$=0mA t_{cyc}=Min	—	—	120	mA
Output leakage	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL} $V_{I/O}$=0 to V_{DD}	−1	—	1	μA
High level output voltage	V_{OH}	I_{OH}=−4.0mA	2.4	—	—	V
Low level output voltage	V_{OL}	I_{OL}=8.0mA	—	—	0.4	V

●Terminal Capacitance

(f=1MHz, Ta=25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address Capacitance	C_{ADD}		—	—	10	pF
Input Capacitance	C_I		—	—	10	pF
I/O Capacitance	$C_{I/O}$		—	—	10	pF

■ AC ELECTRICAL CHARACTERISTICS

O Read Cycle

(V_{DD} = 5V ± 10%, V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Conditions	SRM2125645		SRM2125655		Unit
			Min	Max	Min	Max	
Read cycle time	t_{RC}	*1	45	—	55	—	ns
Address access time	t_{ACC}		—	45	—	55	ns
$\overline{CS}$ access time	t_{ACS}		—	45	—	55	ns
$\overline{CS}$ output set time	t_{CLZ}	*2	5	—	5	—	ns
$\overline{CS}$ output floating time	t_{CHZ}		0	20	0	25	ns
Output hold time	t_{OH}	*1	5	—	5	—	ns

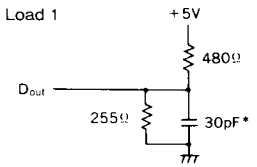
O Write Cycle

(V_{DD} = 5V ± 10%, V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Conditions	SRM2125645		SRM2125655		Unit
			Min	Max	Min	Max	
Write cycle time	t_{WC}	*1	45	—	55	—	ns
Chip select time	t_{CW}		40	—	50	—	ns
Address valid to end of write	t_{AW}		40	—	50	—	ns
Address setup time	t_{AS}		0	—	0	—	ns
Write pulse width	t_{WP}		35	—	45	—	ns
Address hold time	t_{WR}		0	—	0	—	ns
Input data set time	t_{DW}		20	—	25	—	ns
Input data hold time	t_{DH}		0	—	0	—	ns
Write to output floating	t_{WHZ}	*2	0	20	0	25	ns
Output active from end of write	t_{OW}		0	—	10	—	ns

*1 Test Conditions

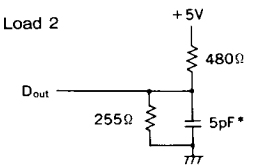
1. Input pulse level: V_{SS} to 3.0V
2. $t_r = t_f = 5$ns
3. Input and output timing reference levels: 1.5V
4. Output load $C_L = 30$pF



*Including scope and jig.

*2 Test Conditions

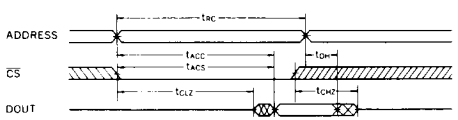
1. Input pulse level: V_{SS} to 3.0V
2. $t_r = t_f = 5$ns
3. Input timing reference levels: 1.5V
4. Output timing reference levels: ±200mV (the level displaced from stable output voltage level)
5. Output load $C_L = 5$pF



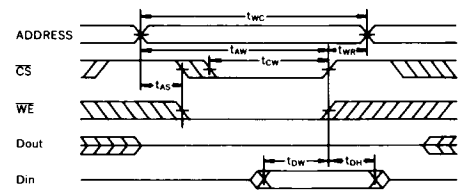
*Including scope and jig.

●Timing Chart

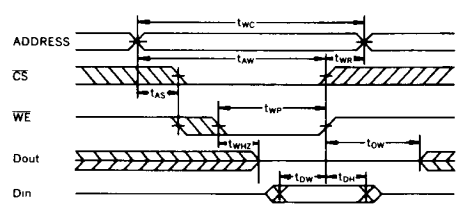
○Read Cycle



○Write Cycle (1) ($\overline{CS}$ Control)



○Write Cycle (2) ($\overline{WE}$ Control)



Note : During read cycle time, $\overline{WE}$ should be "H" level.

■FUNCTIONS

●Truth Table

$\overline{CS}$	$\overline{WE}$	A0 to A15	DATA I/O	Mode	I_{DD}
H	*	*	Hi-Z	Standby	I_{DDS}, I_{DDSI}
L	L	Stable	D_{IN}	Write	I_{DDA}
L	H	Stable	D_{OUT}	Read	I_{DDA}

* : "H" or "L"

●Read Mode

The Data appear when the address is setted while holding $\overline{CS}$="L", and $\overline{WE}$="H".

●Write Mode

There are following 3 ways of writing data into memory.

(1) Hold $\overline{WE}$="L", set sddress and give "L" pulse to $\overline{CS}$.

(2) Hold $\overline{CS}$="L", set address and give "L" pulse to $\overline{WE}$.

(3) After setting addresses, give "L" pulse to both $\overline{CS}$ and $\overline{WE}$.

In above any case, data on the DATA I/O terminals are latched up into the SRM21256 when $\overline{CS}$ or $\overline{WE}$ is in positive-going. Since DATA I/O terminals are high impedance when $\overline{CS}$="H", the contention on the data bus can be avoided.

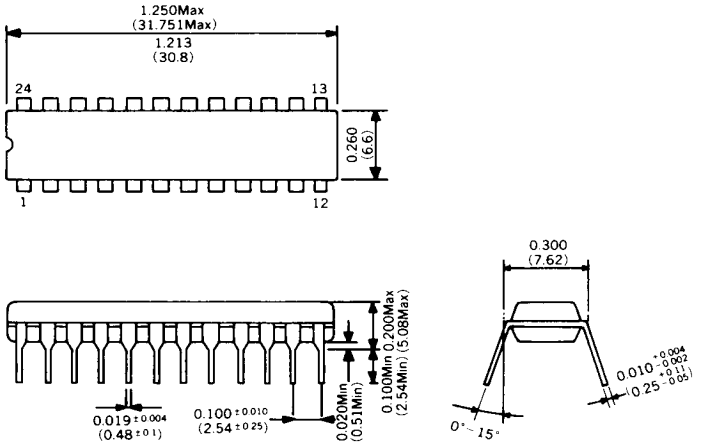
●Standby Mode

When $\overline{CS}$ is "H" the SRM21256 is in the stand-by mode. In this case, Data I/O terminals are in Hi-Z, so that all inputs of addresses, $\overline{WE}$ and data can be any "H" or "L".

■PACKAGE DIMENSIONS

N24

24-pin DIP



unit : inch
(mm)

■CHARACTERISTICS CURVES

Under measurment