Radiation-Hardened Semicustom Products

UTE-R Array Family

Data Sheet

T-42-11-09

UNITED TECHNOLOGIES MICROELECTRONICS CENTER

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FEATURES

- ☐ Total dose 1E6 rads(Si) to this data sheet specification according to MIL-STD-883, Method 1019
- ☐ Total dose 1E7 rads(Si) functional
- ☐ Dose-rate upset > 5E9 rads(Si)/sec UT20ER*
  Dose-rate upset > 5E8 rads(Si)/sec UT50ER*
- ☐ Dose-rate survivability > 1E12 rads(Si)/sec
- ☐ Device will not latch up under specified use conditions.
- ☐ SEU < 6.25E-8 errors/cell-day (flip-flop)**
- ☐ LET threshold = 47 MeV cm^2/mg, flip-flop cross-section = 2E-6cm^2
- ☐ Projected neutron fluence 1E14 n/cm^2
- ☐ Designed for military/aerospace applications
  - Operating range: −55°C to +125°C
  - Supply voltage: 5V ±10%
  - Latchup immunity: ±150mA with a 500msec pulse
  - Screened to specific test methods of MIL-STD-883 Method 5004, Level B or Level S per UTMC's standard flows
- ☐ 1.2μ twin-well CMOS, epitaxial, double-level-metal technology
- ☐ Gate delay: 530 picoseconds typical (2-input NAND w/2 loads)
- ☐ Up to 50,000 usable gates
  Up to 256 signal I/O capability
- ☐ I/O TTL and CMOS compatible & programmable
- ☐ Clock circuit
- ☐ Boundary-scan registers built into I/O cell locations (IEEE 1149.1 Standard, "JTAG")
- ☐ Advanced package design with isolated quiet power and ground
- ☐ Design support through UTMC's Mentor Graphics® and Valid Workstation Toolkits on Apollo® and Sun® platforms and UTMC's in-house design system
- ☐ Embedded memory and megafunction capability

* Short pulse: 15ns FWHM (full width, half maximum)
** May be design dependent. SEU immunity of flip-flops can be improved through the use of special macrocell designs.

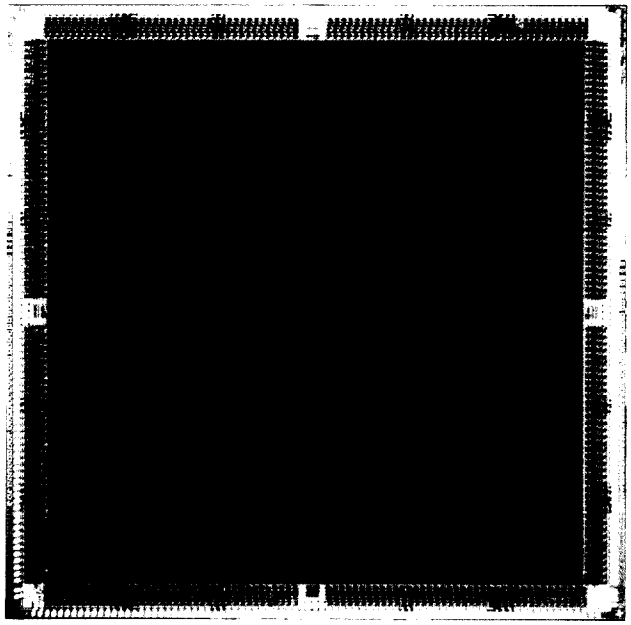


Figure 1. UT50ER

PRODUCT DESCRIPTION

UTMC designed the UTE-R array family to meet the needs of designers of high-reliability military and aerospace systems where high radiation tolerance is required. Without compromise, the family complies with the harsh and rugged environmental requirements of these systems. Built using UTMC's proprietary radiation-hardened process, these devices meet the needs of strategic and tactical radiation-hardened applications.

UTMC has developed special low-temperature processing techniques to enhance the total-dose radiation hardness of both the gate oxide and the field oxide while maintaining circuit density and reliability. For transient radiation hardness and latchup immunity, UTMC builds all its radiation-hardened products on epitaxial wafers using an advanced silicon gate CMOS process. In addition, UTMC has developed advanced power and ground distribution and packaging techniques ensuring greater transient-upset resistance.

ARRAY ARCHITECTURE

Developed from UTMC's patented continuous-column transistor architectures, the UTE-R array family uses a highly efficient continuous-transistor architecture for the internal cell constructions. The continuous-transistor architecture reduces the number of wasted transistors common in a conventional block-structured array. This architecture also provides additional flexibility during placement and routing, enabling the designer to achieve high functional density in the design.

CELL NAMING CONVENTIONS

The architecture for the UTE-R array family allows the user to program both the internal cells and the I/O cells. The basic internal cell set generally follows industry-standard nomenclature for the functions. Table 1 lists typical function names for the internal cell set. In addition to the core cell set, UTMC offers more extended functions and macros. Please contact UTMC for the current cell/macro listing.

Table 1. Basic UTE-R Internal Functions

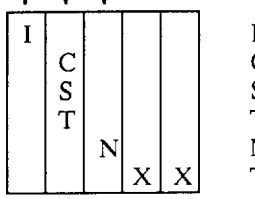
AND2	INV2	TS2
AND3	INV3	TSI1
AO21	INV4	XNOR2
AOI13	MUX2	XOR2
AOI21	MUX4	DFAPCB
AOI22	NAND2	DFFAC
AOI23	NAND3	DFFAP
AOI24	NAND4	DFFSC
BUF11	NAND6	DFF
BUF12	NAND8	DLC
BUF13	NOR2	DLP
BUF21	NOR4	DL
BUF22	OAI13	JKFFAC
BUF31	OAI21	JKFFAP
FADD	OAI22	QDFF
HADD	OR2	SR00
INV1	OR3	SR11
	QMUX21	TFAPCB

Most of the cells above have equivalents offering high output drive. Please refer to the UTE-R Cell Library for specific details.

In the I/O cell region, UTMC offers options that provide variable drive capability and other interface options. Table 2 illustrates the I/O cell-naming methodology used for the UTE-R technology.

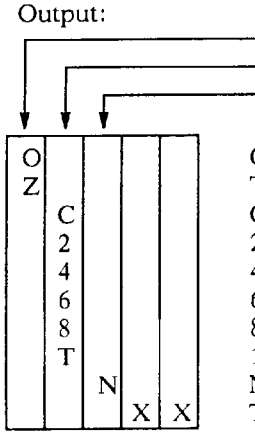
Table 2. UTE-R I/O Cell Naming

Input:



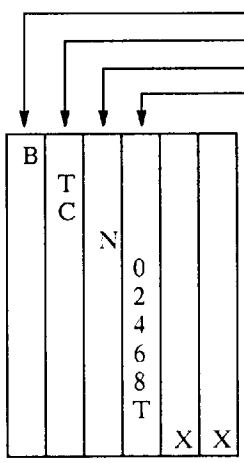
INPUT
CMOS
SCHMITT TRIGGER
TTL
NON-INVERTING
TWO-DIGIT NUMBER
represents type of configuration

Output:



OUTPUT
TRI-STATE
CMOS
2mA
4mA
6mA
8mA
12mA
NON-INVERTING
TWO-DIGIT NUMBER
represents type of configuration

Combination I/O:



BI-DIRECT
TTL (input level/output level)
CMOS (input level/output level)
NON-INVERTING
CMOS (4ma output drive)
2mA
4mA
6mA
8mA
12mA
TWO-DIGIT NUMBER
represents type of configuration

UTE-R GATE ARRAY FAMILY

PART NUMBERS	USABLE (1) TRANSISTOR PAIRS	EQUIVALENT (2) USABLE GATES	I/O CIRCUITS		TOTAL PADS
			(3)	(4)	
UT20ER	69,426	20,000	176	40	218
UT50ER	173,528	50,000	256	80	342

Notes:
1. This number will be larger for many applications and it does not apply for RAM applications.
2. Based on NAND2 equivalents, usable gate count will vary, depending on design.
3. I/O signals; these include 5 JTAG I/Os. Available I/O count is dependent upon package selected.
4. V_{DD}/V_{DDQ} -- V_{SS}/V_{SSQ} power pads reserved.

I/O BUFFERS

The UTMC UTE-R array library contains a wide selection of input, output, and bidirectional buffers. Each input buffer has the following features: input protection circuitry, non-inverting TTL or CMOS input levels, radiation-hardening design techniques, built-in boundary scan, and pull-up or pull-down resistors. Output buffers are available in 3-state, open drain, with and without voltage-rate control. The buffers also include built-in boundary scan and provide for output drive configurations ranging from 2 to 12 mA. The large output transistors used to drive off-chip loads are powered from their own set of power supply pins to help isolate noise and keep unwanted transients to a minimum. In addition, to assist users in minimizing undesirable transients on signal and power lines, the user can implement all output and bidirectional buffers with variable voltage ramp rates. The voltage ramp rate control is available to help control the rate of change of current switching (di/dt) during logic level transitions. The array family's pad count ranges up to 342 pad locations around the periphery with power and ground placements provided for power distribution.

I/O Built-In Scan

The UTMC UTE-R arrays include a test access port and boundary-scan architecture. The architecture conforms to the IEEE 1149.1 standard. The 1149.1 standard is a solution to the problem of testing assembled printed circuit boards and other products based on highly complex digital integrated circuits and high-density surface-mount assembly techniques. The boundary-scan architecture also provides a means of accessing and controlling design-for-test features built into the digital integrated circuits themselves. Such features might, for example, include internal scan paths and self-test functions as well as other features intended to support service applications in assembled product.

CAD TOOLS

UTMC's CAD tools support the UTE-R libraries. Extensive software toolkits on Mentor and Valid workstations support design in a familiar environment and, coupled with the vendor's CAE tools, offer an effective design environment. The toolkits include:

- Schematic capture support
- Design verification and checking
- Full simulation support featuring nominal, best-case, and worst-case delay. Simulation models incorporate actual circuit loading, and provide back-annotation of either pre- or post-layout delays.
- UTMC Simulation Input Language (SIL) support
- Test vector verification
- Design transfer

UTMC's in-house design system contains a comprehensive set of design tools including simulation, fault simulation, automatic layout, test vector conversion, physical design verification and PG tape generation. Design processing through UTMC's in-house design system is performed by UTMC personnel with feedback to the customer.

SPEED AND PERFORMANCE

The traditional propagation delay for a CMOS gate is a function of its fanout loading, interconnection loading, processing tolerance, supply voltage ranges, operating temperature, input transition times, and input signal polarity. In the radiation-hardened environment, additional performance variances must be considered in both the pre-rad and post-rad conditions.

In the UTE-R array family internal and I/O cell performance describes a nominal delay condition which estimates performance for nominal pre-rad process conditions, nominal power supplies, and room temperature operation. Each cell is then specified for a range of operation depending upon how its performance is affected by both the traditional factors and the factors encountered in a radiation environment.

Each cell in the UTE-R library may have a different maximum and minimum factor based upon its response to the performance variables listed above. For a rough estimate, designers may use a factor of 2.4X to .2X to estimate the maximum and minimum performance ranges as applied to the nominal delay equations. UTMC's in-house design system will provide an accurate delay estimate during the design implementation.

CLOCK CIRCUIT

UTMC has four optional clock drivers for the internal array. The clocking system has been designed to produce predictable, minimum skew timing control. Clock circuitry is located under center power and ground pins in the array's periphery. The circuit configuration allows designers to manipulate the clock signal prior to the drivers. Load connections are controlled throughout the clock network to reduce clock skew. Clock drivers can be combined to drive larger capacitive loads, within maximum and minimum load requirements for any clock driver combination.

POWER ESTIMATES

In CMOS technology, the power dissipated is a function of the loads being driven and the frequency at which the part is operated. To calculate a rough estimate of the expected power, designers should use a value of 8.25 uWatts/Gate MHz for internal gates with typical loading and 1.50 mWatts/I/O MHz for standard output buffers driving 50 pf. For a more accurate power estimate please consult with UTMC during the design implementation.

UTE-R ARRAY PERFORMANCE

Typical Transient Characteristics VDD=5V, TC=25°C (All values in nanoseconds, unless otherwise listed.)

CELL	OUTPUT TRANSITION	TRANSIENT DELAYS (ns)				INTERNAL GATE COUNT
		OUTPUT LOAD CAPACITANCE*				
OUTPUT BUFFERS		15PF		50PF		
OCN10, CMOS Scan	HL	3.80		6.00		N/A
	LH	3.85		6.10		
O4N10, TTL Scan, 4mA	HL	4.22		7.07		N/A
	LH	3.48		5.09		
OTN10, TTL Scan, 12mA	HL	3.90		5.07		N/A
	LH	3.64		4.46		
INPUT BUFFERS		FANOUT LOADS**				
		1	2	5	8	
ICN10, CMOS Scan	HL	1.70	1.74	1.87	2.00	N/A
	LH	1.42	1.47	1.65	1.82	
ITN10, TTL Scan	HL	2.40	2.45	2.60	2.74	N/A
	LH	1.33	1.40	1.57	1.75	
INTERNAL GATES		FANOUT LOADS				
		1	2	5	8	
INV, Inverter	HL	.32	.41	.69	.97	1/2
	LH	.41	.54	.90	1.28	
INV4, Inverter 4X	HL	.09	.15	.33	.52	2
	LH	.46	.51	.67	.82	
NAND2, 2-Input NAND	HL	.43	.55	.91	1.28	1
	LH	.45	.57	.95	1.32	
NOR2, 2-Input NOR	HL	.34	.44	.72	.99	1
	LH	.67	.92	1.66	2.39	

* Test is performed at 50pf load condition; other load conditions are for information only

** Fanout loads consist of 1 equivalent gate input load. In wiring, 400μ of Metal 1 or 700μ of Metal 2 is equivalent to 1 gate input load.

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ABSOLUTE MAXIMUM RATINGS*
(Referenced to VSS)

SYMBOL	PARAMETER	LIMITS	UNITS
VDD	DC supply voltage	-0.3 to +7.0	V
VI/O	Voltage on any pin	-0.3 to VDD +0.3	V
TSTG	Storage temperature	-65 to +150	°C
TJ	Maximum junction temperature	+175	°C
ILU	Latchup immunity	+/-150	mA
II	DC input current	+/-10	mA
TLS	Lead temperature (soldering, 5 sec)	+300	°C

Note:
* Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS	UNITS
VDD	DC supply voltage	4.5 to 5.5	V
TC	Temperature range	-55 to +125	°C
VIN	DC input voltage	0 to VDD	V

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5.0V ± 10%, V_{SS} = 0V (1); −55°C < T_A < +125°C)

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
V_{IL}	Low-level input voltage TTL inputs CMOS inputs			 0.8 .3 V_{DD}	 V V
V_{IH}	High-level input voltage TTL inputs CMOS inputs		 2.2 .7 V_{DD}		 V V
I_{IN}	Input leakage current TTL, CMOS input Inputs with pull-down resistors Inputs with pull-up resistors	 V_{IN} = V_{DD} or V_{SS} V_{IN} = V_{DD} V_{IN} = V_{SS}	 −10 +150 −900	 10 +900 −150	 µA µA µA
V_{OL}	Low-level output voltage TTL outputs Single-drive buffer Triple-drive buffer * CMOS outputs	 I_{OL} = 4.0mA I_{OL} = 12.0mA I_{OL} = 1µA		 0.4 0.4 0.05	 V V V
V_{OH}	High-level output voltage TTL outputs Single-drive buffer Triple-drive buffer * CMOS outputs	 I_{OH} = −4.0mA I_{OH} = −12.0mA I_{OH} = −1µA	 2.4 2.4 V_{DD} − 0.05		 V V V V
I_{OZ}	Three-state output leakage current TTL outputs Single-drive buffer Triple-drive buffer *	V_O = V_{DD} or V_{SS}	 −10 −30	 10 30	 µA µA
I_{OS}	Short-circuit output current (2, 3) Single-drive buffer (5) Triple-drive buffer * Single-drive buffer (5) Triple-drive buffer *	V_{DD} = 5.5V, V_O = V_{DD} V_{DD} = 5.5V, V_O = 0V	 −100 −300	 100 300 	 mA mA mA mA
C_{IN}	Input capacitance (4)	F = 1MHz @ 0V		10	pF
C_{OUT}	Output capacitance (4) Single-drive buffer Triple-drive buffer *	F = 1MHz @ 0V		 10 20	 pF pF
C_{IO}	Bidirect I/O capacitance (4) Single-drive buffer Triple-drive buffer *	F = 1MHz @ 0V		 15 25	 pF pF

Notes:
* Contact UTMC prior to usage.
1. Maximum allowable relative ground shift = 50mV.
2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for a maximum duration of one second.
4. Capacitance measured for initial qualification or design changes which may affect the value.
5. I_{OS} CMOS equals I_{OS} TTL single-drive buffer.

PACKAGING

UTMC's array packaging comes in two package types -- pingrid arrays and flatpacks. Both types are built using multilayer construction techniques. All packages have built-in power and ground planes, lowering the overall inductance and resistance for the part's power distribution. This improved package design ensures the part's proper performance during periods of heavy switching. Each design provides adequate power distribution for the VSS and VDD supplies. In general, the package types supported in UTMC's in-house design system reserve pins for power distribution depending upon the package type and package electrical characteristics.

RADIATION TESTING

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Total dose Co-60 testing is in accordance with MIL-STD-883, Method 1019.

SCREENING PROCEDURES

Contact UTMC for information on standard military screening flows.

PACKAGE DIE COMBINATIONS

PACKAGE / DIE	UT20ER	Θ_{JC} (2) (°C/watt)	UT50ER	Θ_{JC} (°C/watt)
Pingrid Arrays 84	X(1)	10		
120			X	6
144	X	8		
209	X	7	X(1)	6
281			X	6
Flatpacks 84	X(1)	12		
132	X	10		
144			X(1)	8
172	X	12		
196	X	12	X(1)	8
256			X	8
304			X(1)	8

Note:
1. Call for package availability.
2. Θ_{JC} is measured in still air.