MOSEL VITELIC

V53C511816502
1M x 16 EDO PAGE MODE
CMOS DYNAMIC RAM
OPTIONAL SELF REFRESH

HIGH PERFORMANCE	50	60
Max. $\overline{RAS}$ Access Time, (t_{RAC})	50 ns	60 ns
Max. Column Address Access Time, (t_{CAA})	25 ns	30 ns
Min. Extended Data Out Page Mode Cycle Time, (t_{PC})	20 ns	25 ns
Min. Read/Write Cycle Time, (t_{RC})	84 ns	104 ns

Features

- 1MB x 16-bit organization
- EDO Page Mode for a sustained data rate of 50 MHz
- $\overline{RAS}$ access time: 50, 60 ns
- Dual $\overline{CAS}$ Inputs
- Low power dissipation
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh
  - Refresh Interval: 1024 cycles/16 ms
- Available in 42-pin 400 mil SOJ and 44/50-pin 400 mil TSOP-II Packages
- Single 5V ±10% Power Supply
- TTL Interface
- Optional Self Refresh (V53C511816502S)
  - Refresh Interval: 1024 cycles/128 ms

Description

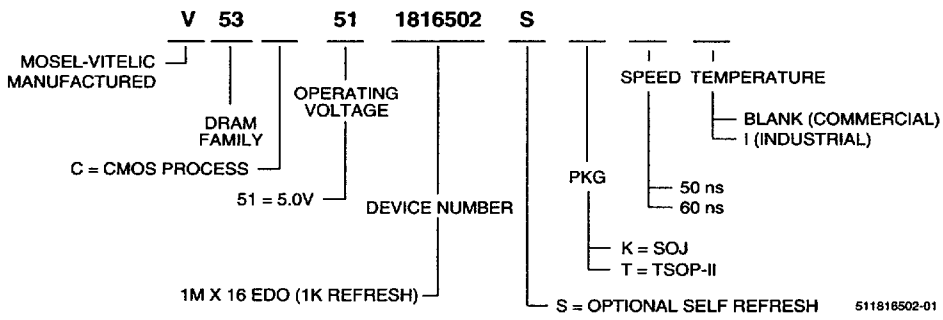
The V53C511816502 is a 1048576 x 16 bit high-performance CMOS dynamic random access memory. The V53C511816502 offers Page mode operation with Extended Data Output. The V53C511816502 has symmetric address, 10-bit row and 10-bit column.

All inputs are TTL compatible. EDO Page Mode operation allows random access up to 1024 x 16 bits, within a page, with cycle times as short as 20ns.

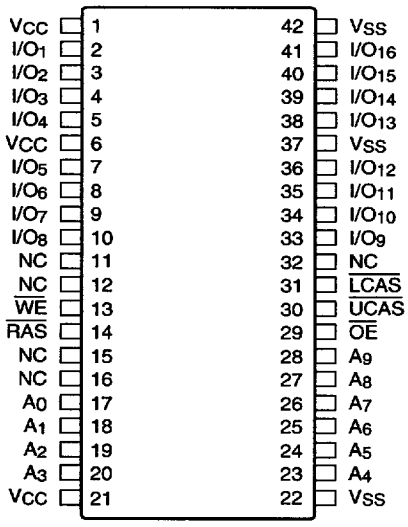
These features make the V53C511816502 ideally suited for a wide variety of high performance computer systems and peripheral applications.

Device Usage Chart

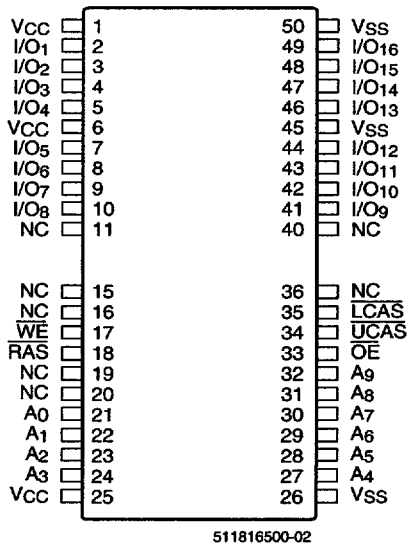
Operating Temperature Range	Package Outline		Access Time (ns)		Power	Temperature Mark
	K	T	50	60	Std.	
0°C to 70 °C	•	•	•	•	•	Blank
–40°C to +85°C	•	•	•	•	•	I



42-Pin Plastic SOJ PIN CONFIGURATION Top View



44/50-Pin Plastic TSOP-II PIN CONFIGURATION Top View



511816500-02

Description	Pkg.	Pin Count
TSOP-II	T	44/50
SOJ	K	42

Pin Names

A_0–A_9	Row, Column Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Column Address Strobe/Upper Byte Control
$\overline{LCAS}$	Column Address Strobe/Lower Byte Control
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O_1–I/O_{16}	Data Input, Output
V_{CC}	+5V Supply
V_{SS}	0V Supply
NC	No Connect

Absolute Maximum Ratings*

Symbol	Parameter	Commercial	Extended	Units
V_N	Power Supply Voltage	-1 to +7	-1 to +7	V
V_{DQ}	Input/Output Voltage	0.5 to min (V_{CC}+0.5, 7.0)	0.5 to min (V_{CC}+0.5, 7.0)	V
T_{BIAS}	Temperature Under Bias	-10 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C

*Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

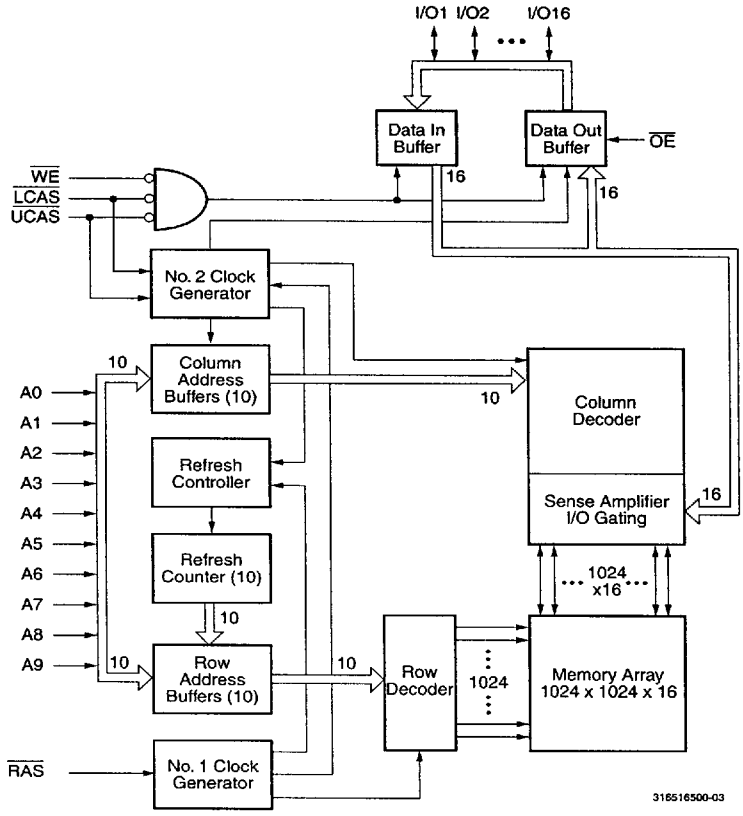
Capacitance*

T_A = 25°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V, f = 1 MHz

Symbol	Parameter	Min.	Max.	Unit
C_{IN1}	Address Input	—	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$	—	7	pF
C_{OUT}	Data Input/Output	—	7	pF

*Note: Capacitance is sampled and not 100% tested.

Block Diagram



DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V, t_T = 2ns unless otherwise specified.

Symbol	Parameter	Access Time	Commercial		Extended		Unit	Test Conditions	Notes
			Min.	Max.	Min.	Max.			
I_{LI}	Input Leakage Current (any input pin)		–10	10	–10	10	µA	$V_{SS} \le V_{IN} \le V_{CC}$ + 0.3V	1
I_{LO}	Output Leakage Current (for High-Z State)		–10	10	–10	10	µA	$V_{SS} \le V_{OUT} \le V_{CC}$+ 0.3V $\overline{RAS}$, $\overline{CAS}$ at V_{IH}	1
I_{CC1}	V_{CC} Supply Current, Operating	50		130		200	mA	$t_{RC} = t_{RC}$ (min.)	2, 3, 4
		60		115		180			
I_{CC2}	V_{CC} Supply Current, TTL Standby			2		2	mA	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{CC3}	V_{CC} Supply Current, $\overline{RAS}$-Only Refresh	50		130		200	mA	$t_{RC} = t_{RC}$ (min.)	2, 4
		60		115		180			
I_{CC4}	V_{CC} Supply Current, EDO Page Mode Operation	50		50		90	mA	Minimum Cycle	2, 4
		60		40		75			
I_{CC5}	V_{CC} Supply Current, during $\overline{CAS}$-before-$\overline{RAS}$ Refresh	50		130		200	mA	$t_{RC} = t_{RC}$ (min.)	2, 4
		60		115		180			
I_{CC6}	V_{CC} Supply Current, CMOS Standby			1.0		1.0	mA	$\overline{RAS} \ge V_{CC} - 0.2$ V, $\overline{CAS} \ge V_{CC} - 0.2$ V	1
I_{CC7}	Self Refresh (Optional)			250		250	µA	CBR cycle with $t_{RAS} \ge t_{RASS\ (min.)}$; $\overline{CAS}$ Held Low; $\overline{WE} = V_{CC}$-0.2V, Address and $D_{IN} = V_{CC}$-0.2V	
V_{CC}	Power Supply Voltage		4.5	5.5	4.5	5.5	V		
V_{IL}	Input Low Voltage		–0.5	0.8	–0.5	0.8	V		1
V_{IH}	Input High Voltage		2.4	V_{CC}+0.5	2.4	V_{CC}+0.5	V		1
V_{OL}	Output Low Voltage			0.4		0.4	V	I_{OL} = 4.2 mA	1
V_{OH}	Output High Voltage		2.4		2.4		V	I_{OH} = –5.0 mA	1

AC Characteristics[5,6]

T_A = 0°C to 70°C, V_{CC} = 5 V ± 10%, t_T = 2ns unless otherwise noted

#	Symbol	Parameter	Limit Values				Unit	Note
			-50		-60			
			Min.	Max.	Min.	Max.		
Common Parameters								
1	t_{RC}	Random read or write cycle time	84	—	104	—	ns	
2	t_{RP}	$\overline{RAS}$ precharge time	30	—	40	—	ns	
3	t_{RAS}	$\overline{RAS}$ pulse width	50	10k	60	10k	ns	
4	t_{CAS}	$\overline{CAS}$ pulse width	8	10k	10	10k	ns	
5	t_{ASR}	Row address setup time	0	—	0	—	ns	
6	t_{RAH}	Row address hold time	8	—	10	—	ns	
7	t_{ASC}	Column address setup time	0	—	0	—	ns	
8	t_{CAH}	Column address hold time	8	—	10	—	ns	
9	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	12	37	14	45	ns	
10	t_{RAD}	$\overline{RAS}$ to column address delay	10	25	12	30	ns	
11	t_{RSH}	$\overline{RAS}$ hold time	13	—	15	—	ns	
12	t_{CSH}	$\overline{CAS}$ hold time	40	—	50	—	ns	
13	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	5	—	5	—	ns	
14	t_T	Transition time (rise and fall)	1	50	1	50	ns	7
15	t_{REF}	Refresh period	—	16	—	16	ms	
Read Cycle								
16	t_{RAC}	Access time from $\overline{RAS}$	—	50	—	60	ns	8, 9
17	t_{CAC}	Access time from $\overline{CAS}$	—	13	—	15	ns	8, 9
18	t_{CAA}	Access time from column address	—	25	—	30	ns	8,10
19	t_{OAC}	$\overline{OE}$ access time	—	13	—	15	ns	
20	t_{CAR}	Column address to $\overline{RAS}$ lead time	25	—	30	—	ns	
21	t_{RCS}	Read command setup time	0	—	0	—	ns	
22	t_{RCH}	Read command hold time	0	—	0	—	ns	11
23	t_{RRH}	Read command hold time referenced to $\overline{RAS}$	0	—	0	—	ns	11
24	t_{CLZ}	$\overline{CAS}$ to output in low-Z	0	—	0	—	ns	8
25	t_{OFF}	Output buffer turn-off delay	0	13	0	15	ns	12
26	t_{OEZ}	Output turn-off delay from $\overline{OE}$	0	13	0	15	ns	12
27	t_{DZC}	Data to $\overline{CAS}$ low delay	0	—	0	—	ns	13
28	t_{DZO}	Data to $\overline{OE}$ low delay	0	—	0	—	ns	13
29	t_{CDD}	$\overline{CAS}$ high to data delay	10	—	13	—	ns	14
30	t_{ODD}	$\overline{OE}$ high to data delay	10	—	13	—	ns	14

AC Characteristics (Cont'd)

#	Symbol	Parameter	Limit Values				Unit	Note
			-50		-60			
			Min.	Max.	Min.	Max.		
Write Cycle								
31	t_{WCH}	Write command hold time	8	–	10	–	ns	
32	t_{WP}	Write command pulse width	8	–	10	–	ns	
33	t_{WCS}	Write command setup time	0	–	0	–	ns	15
34	t_{RWL}	Write command to $\overline{RAS}$ lead time	8	–	10	–	ns	
35	t_{CWL}	Write command to $\overline{CAS}$ lead time	8	–	10	–	ns	
36	t_{DS}	Data setup time	0	–	0	–	ns	16
37	t_{DH}	Data hold time	8	–	10	–	ns	16
Read-modify-Write Cycle								
38	t_{RWC}	Read-write cycle time	113	–	138	–	ns	
39	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ delay time	64	–	77	–	ns	15
40	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ delay time	27	–	32	–	ns	15
41	t_{AWD}	Column address to $\overline{WE}$ delay time	39	–	47	–	ns	15
42	t_{OEH}	$\overline{OE}$ command hold time	10	–	13	–	ns	
EDO Page Mode Cycle								
43	t_{HPC}	EDO page mode cycle time	20	–	25	–	ns	
44	t_{CP}	$\overline{CAS}$ precharge time	8	–	10	–	ns	
45	t_{CPA}	Access time from $\overline{CAS}$ precharge	–	27	–	32	ns	7
46	t_{COH}	Output data hold time	5	–	5	–	ns	
47	t_{RASP}	$\overline{RAS}$ pulse width in EDO page mode	50	200k	60	200k	ns	
48	t_{RHPC}	$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	27	–	32	–	ns	
49	t_{OES}	$\overline{OE}$ setup time prior to CAS	5	–	5	–	ns	
EDO Page Mode Read-Modify-Write Cycle								
50	t_{PRWC}	EDO page mode read-write cycle time	58	–	68	–	ns	
51	t_{CPWD}	$\overline{CAS}$ precharge to $\overline{WE}$	41	–	49	–	ns	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle								
52	t_{CSR}	$\overline{CAS}$ setup time	10	–	10	–	ns	
53	t_{CHR}	$\overline{CAS}$ hold time	10	–	10	–	ns	
54	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ precharge time	5	–	5	–	ns	
55	t_{WRP}	Write to $\overline{RAS}$ precharge time	10	–	10	–	ns	
56	t_{WRH}	Write hold time referenced to $\overline{RAS}$	10	–	10	–	ns	
$\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle								
57	t_{CPT}	$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test cycle)	35	–	40	–	ns	

#	Symbol	Parameter	Limit Values				Unit	Note
			-50		-60			
			Min.	Max.	Min.	Max.		
Optional Self Refresh								
58	t_{REF}	Self Refresh period	—	128	—	128	ms	
59	t_{RASS}	$\overline{RAS}$ pulse width	100K	—	100K	—	ns	17
60	t_{RPS}	$\overline{RAS}$ precharge time	95	—	110	—	ns	17
61	t_{CHS}	$\overline{CAS}$ hold time	-50	—	-50	—	ns	17

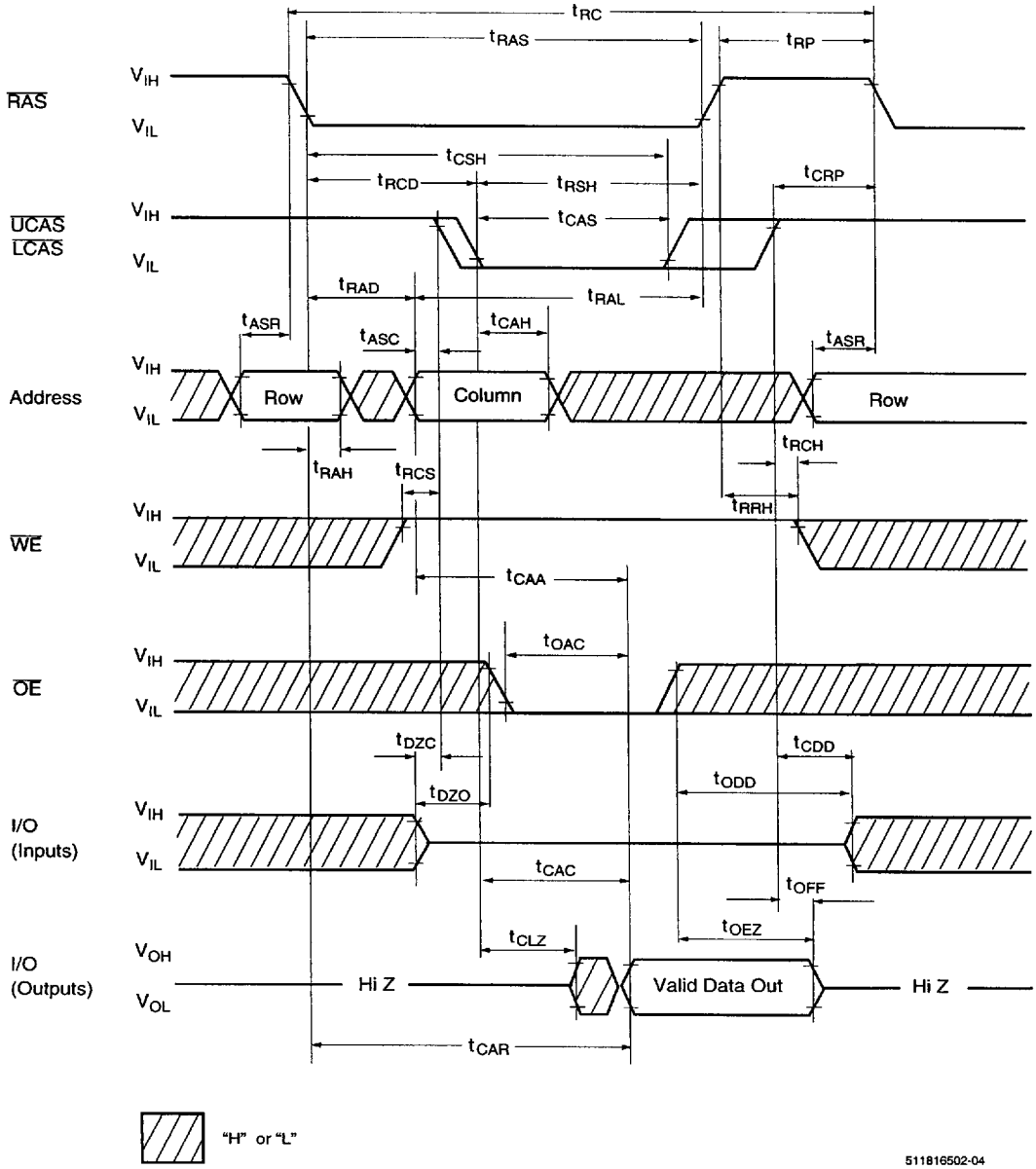
Notes:

1. All voltage are referenced to V_{SS}.
2. I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} depend on cycle rate.
3. I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.
4. Address can be changed once or less while RAS = V_{IL}. In the case of I_{CC4} it can be changed once or less during an EDO page mode cycle.
5. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T = 2ns.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.
8. Measured with the specified current load and 100pF at V_{OL} = 0.8 V and V_{OH} = 2.0 V. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{AA}, t_{CPA}, t_{OEA}, t_{CAC} is measured from tristate.
9. Operation within the $t_{RCD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RCD\ (max.)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.
10. Operation within the $t_{RAD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{AA}.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. $t_{OFF\ (max.)}$, $t_{OEZ\ (max.)}$ define the time at which the outputs acheive the open-circuit condition and are not referenced to output voltage levels. t_{OFF} is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.
13. Either t_{DZC} or t_{DZO} must be satisfied.
14. Either t_{CDD} or t_{ODD} must be satisfied.
15. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS\ (min.)}$, the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD\ (min.)}$, $t_{CWD} > t_{CWD\ (min.)}$, and $t_{AWD} > t_{AWD}$ (min.), the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.
16. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.
17. When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:

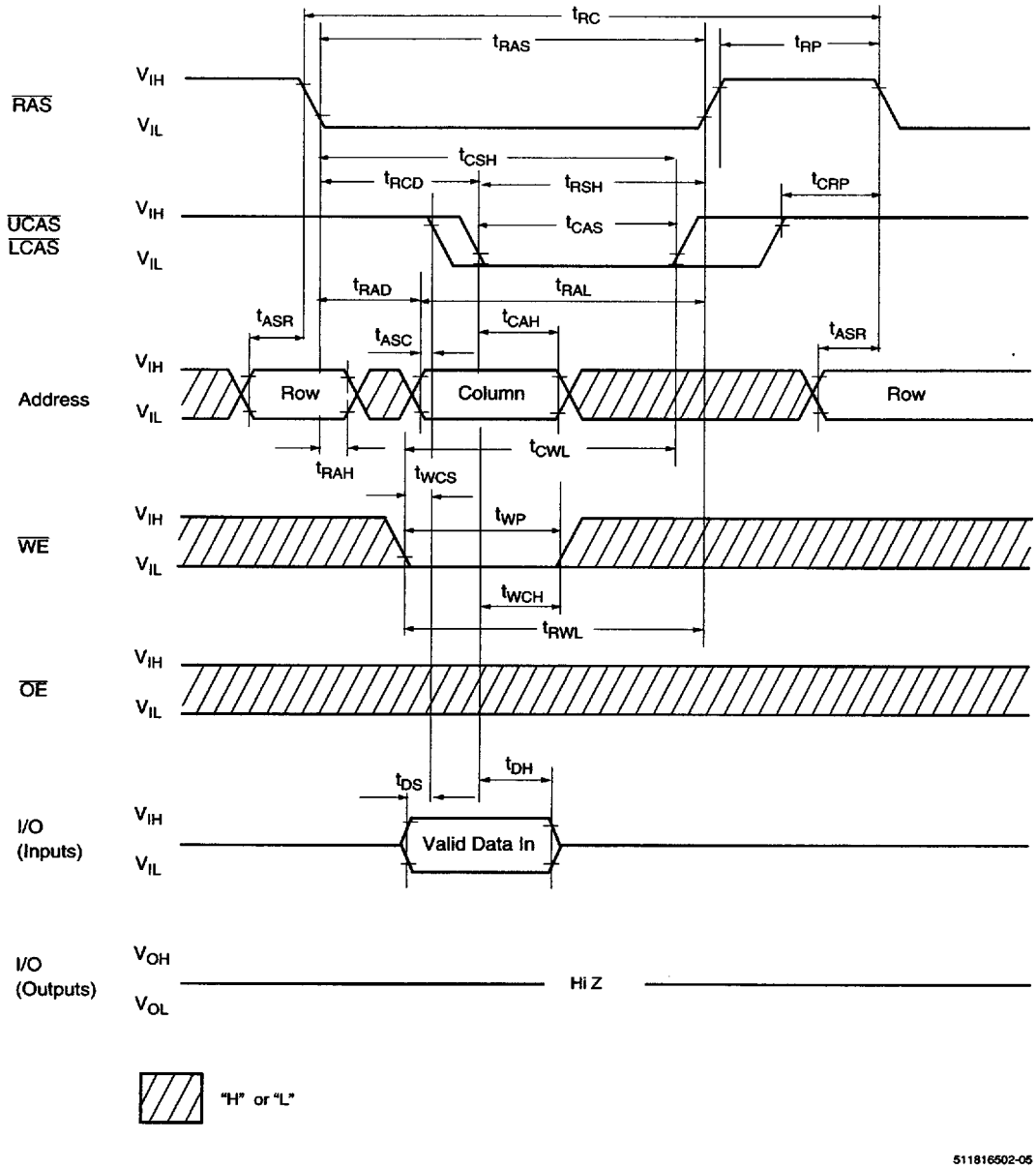
    If row addresses are being refreshed on an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.

    If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.

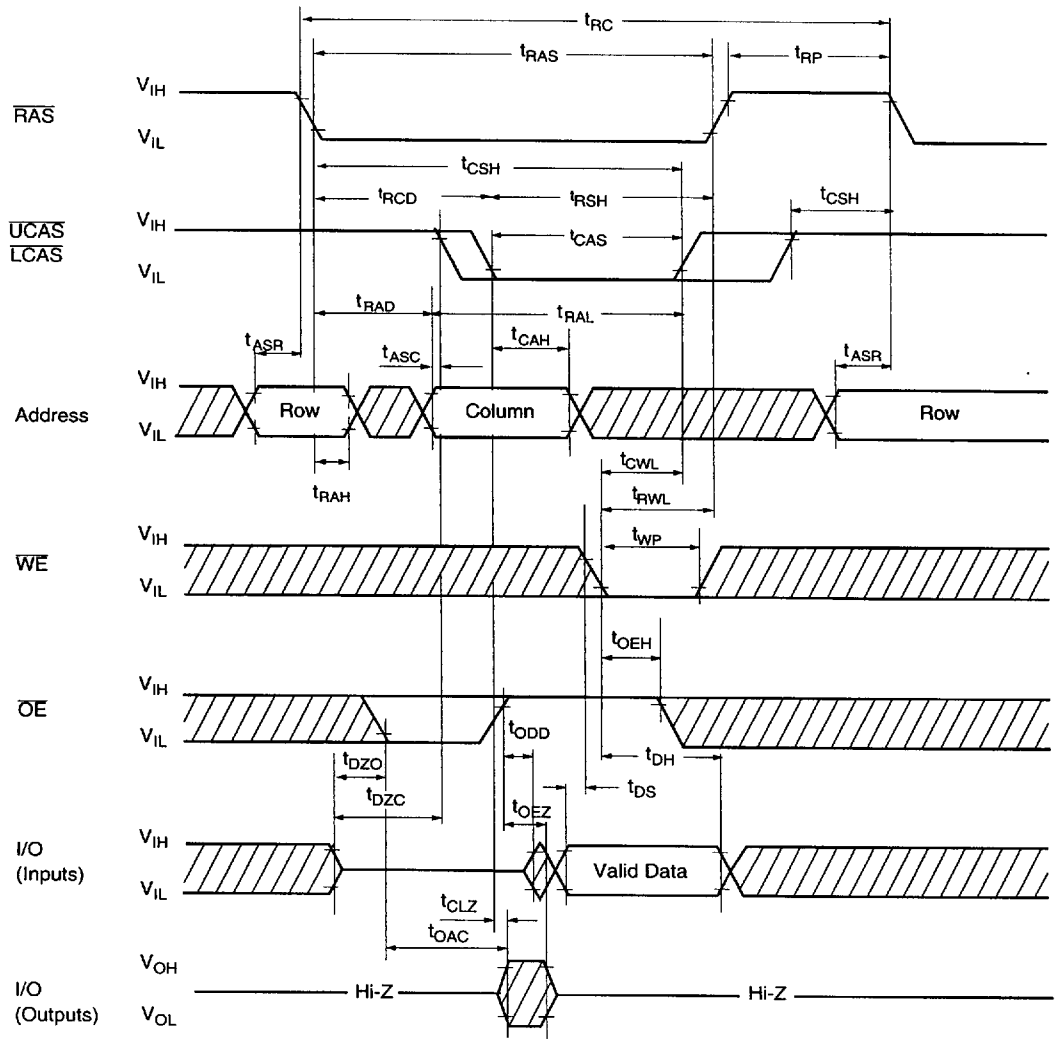
Waveforms of Read Cycle



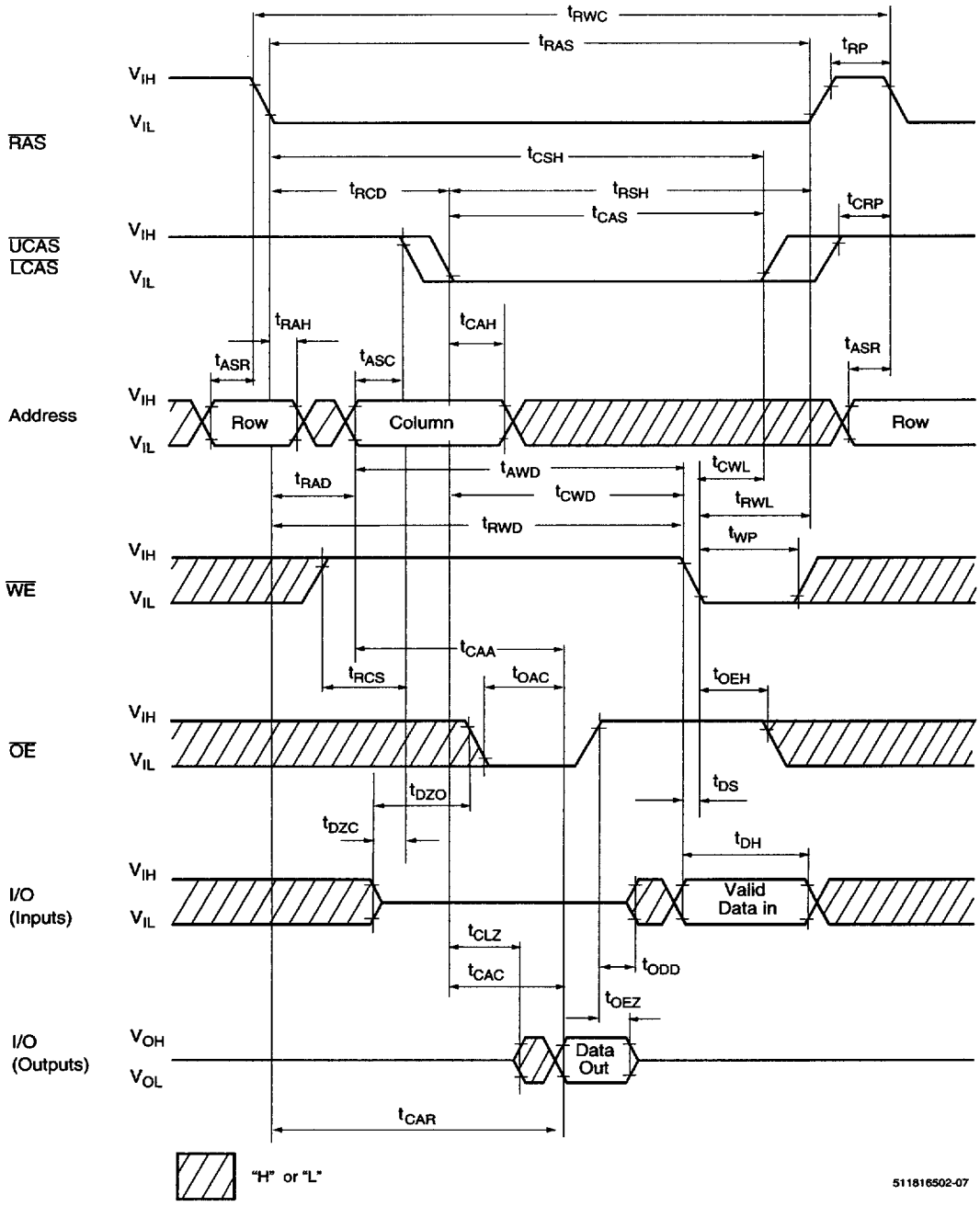
Waveforms of Write Cycle (Early Write)



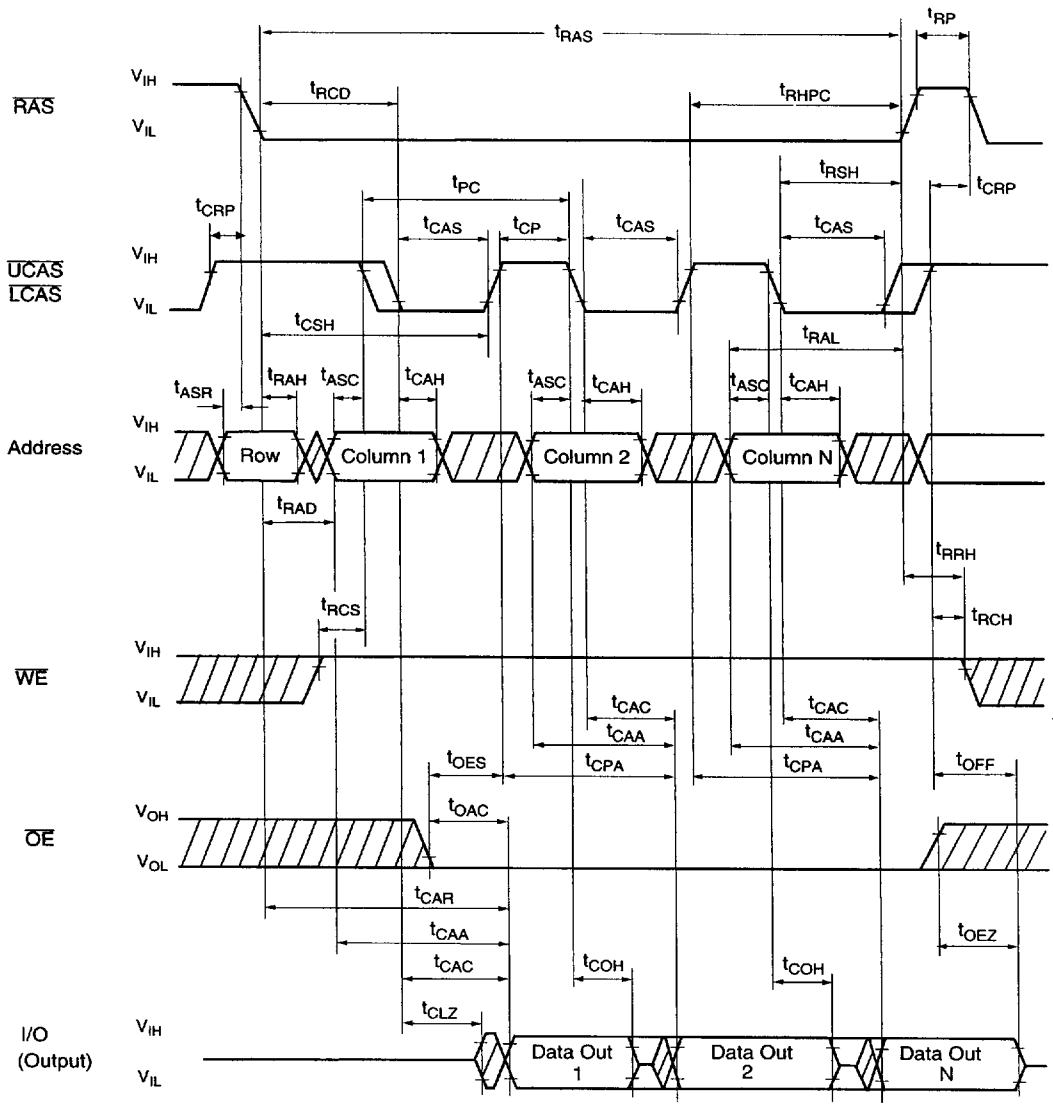
Waveforms of Write Cycle ($\overline{OE}$ Controlled Write)



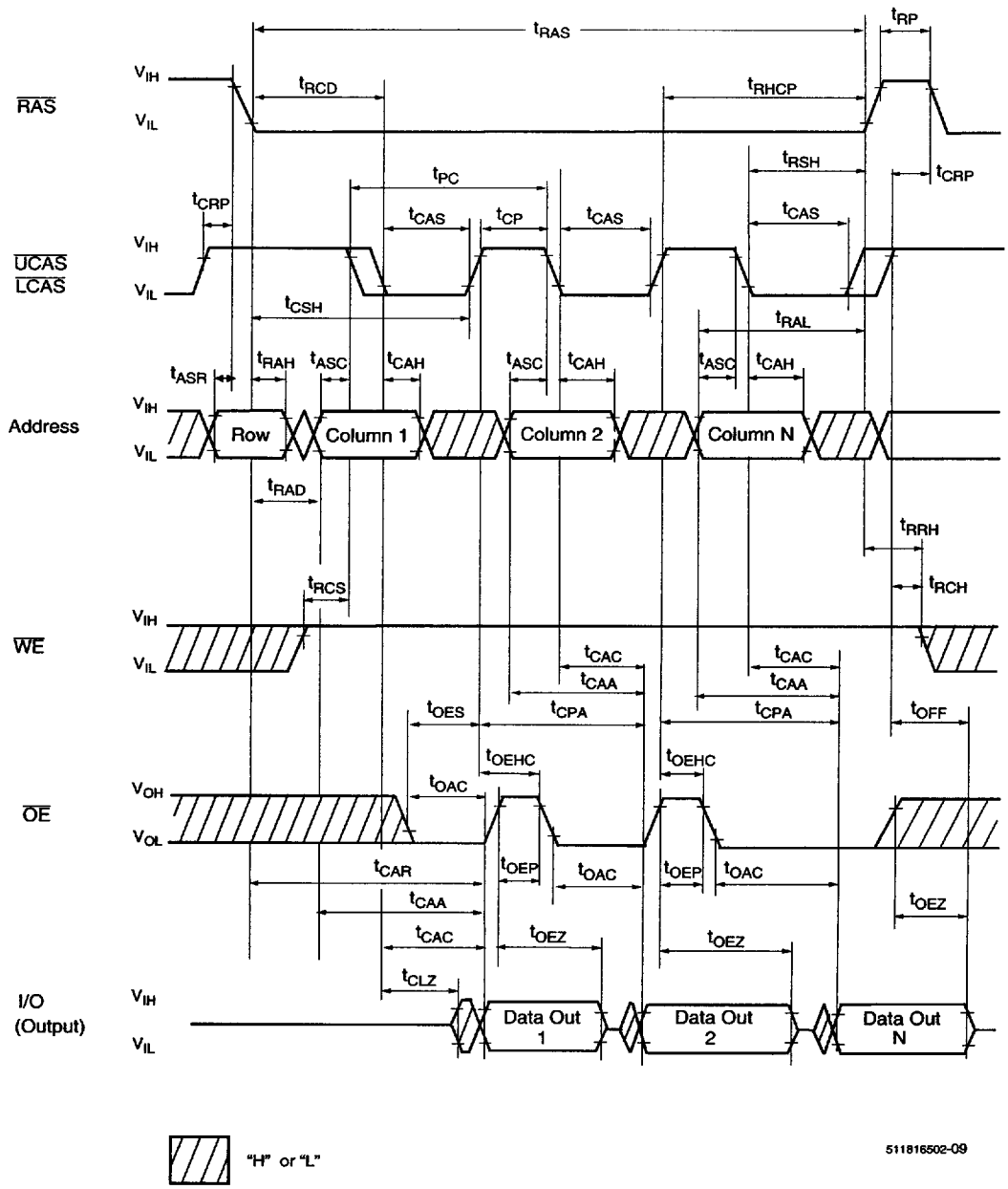
Waveforms of Read-Write (Read-Modify-Write) Cycle



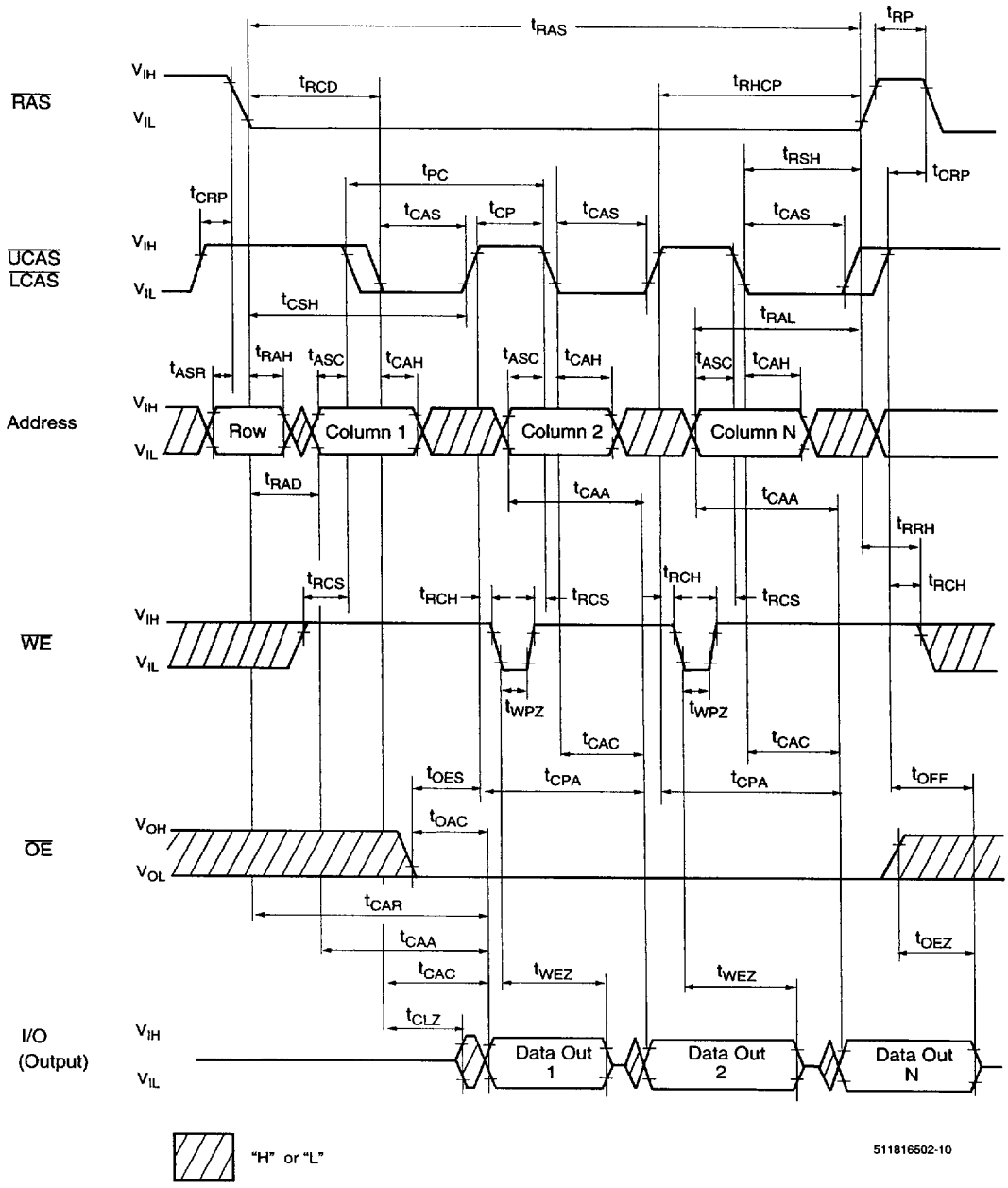
Waveforms of EDO Page Mode Read Cycle



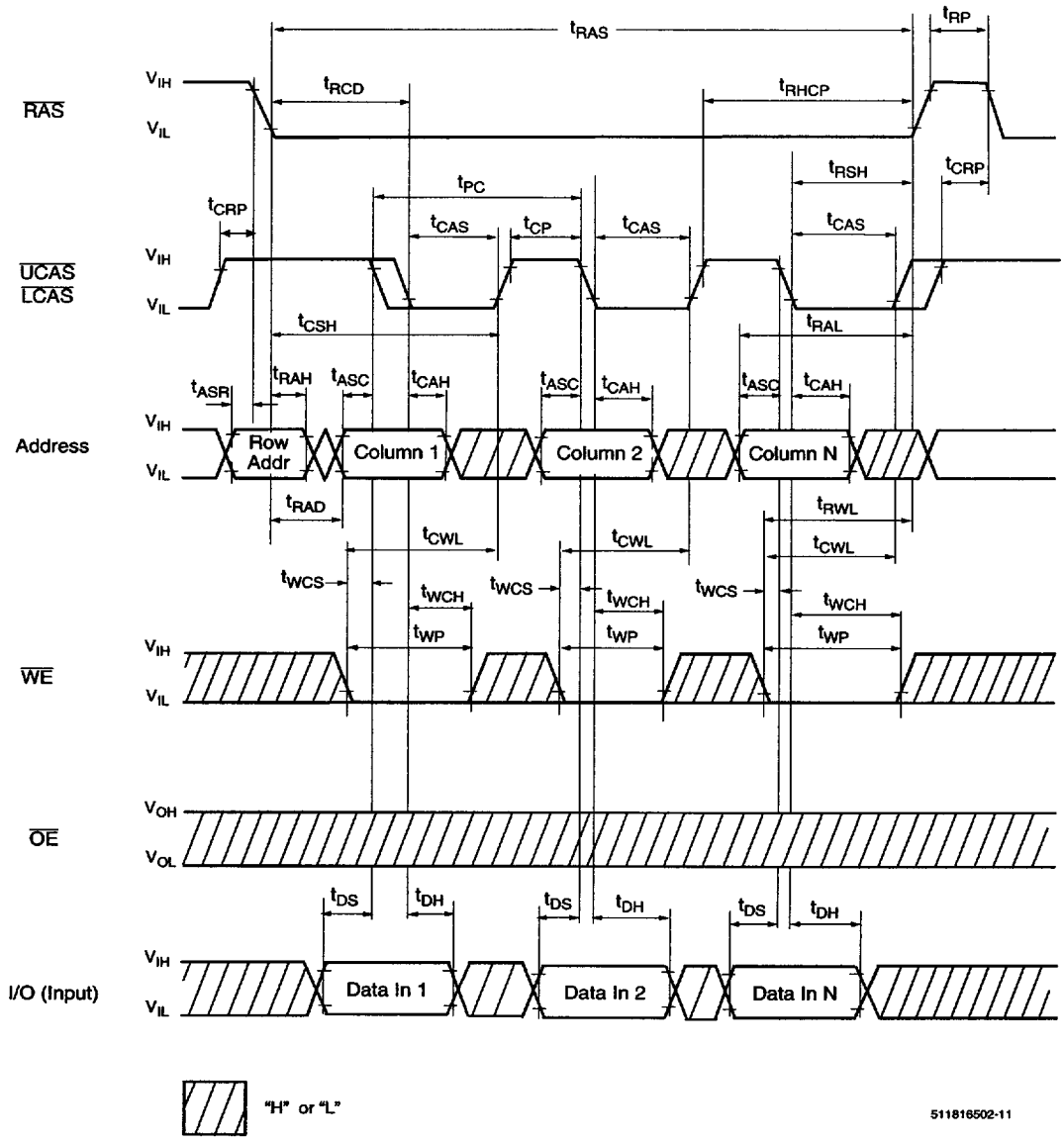
Waveforms of EDO Page Mode Read Cycle ($\overline{OE}$ Control)



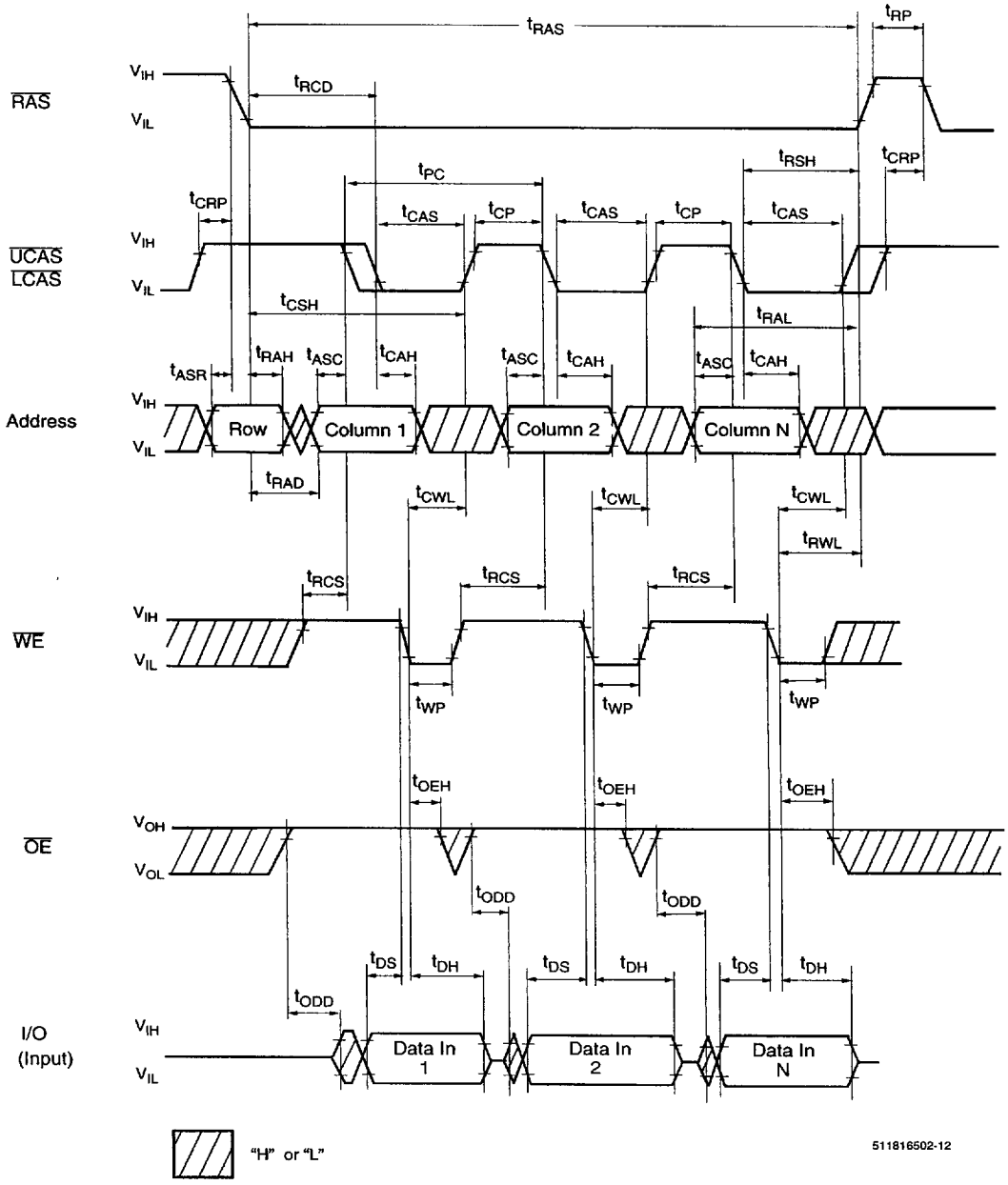
Waveforms of EDO Page Mode Read Cycle ($\overline{WE}$ Control)



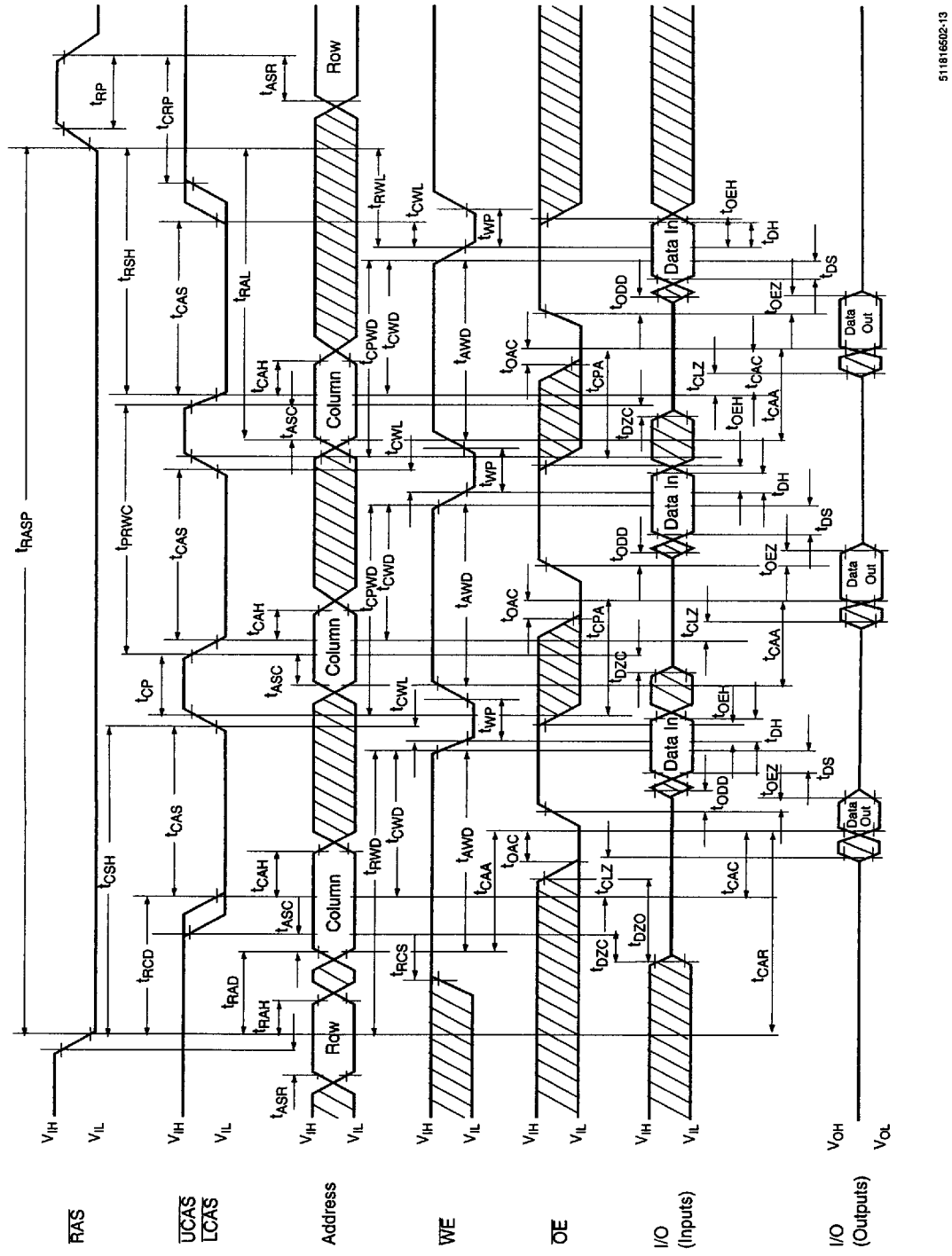
Waveforms of EDO Page Mode Early Write Cycle



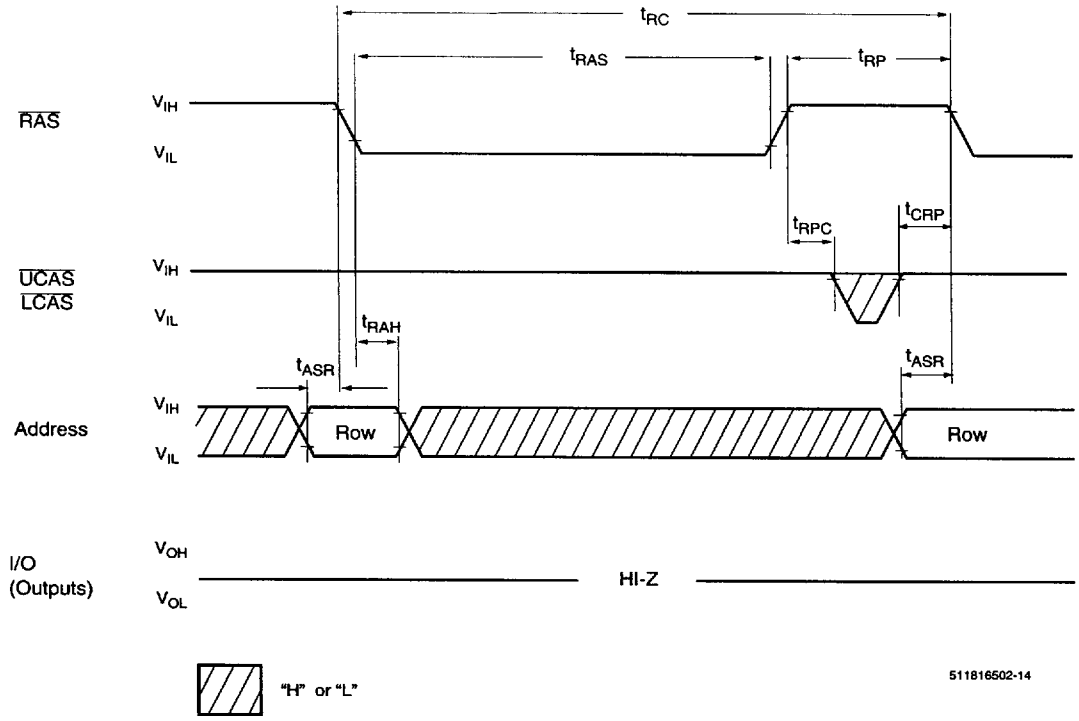
Waveforms of EDO Page Mode Late Write Cycle



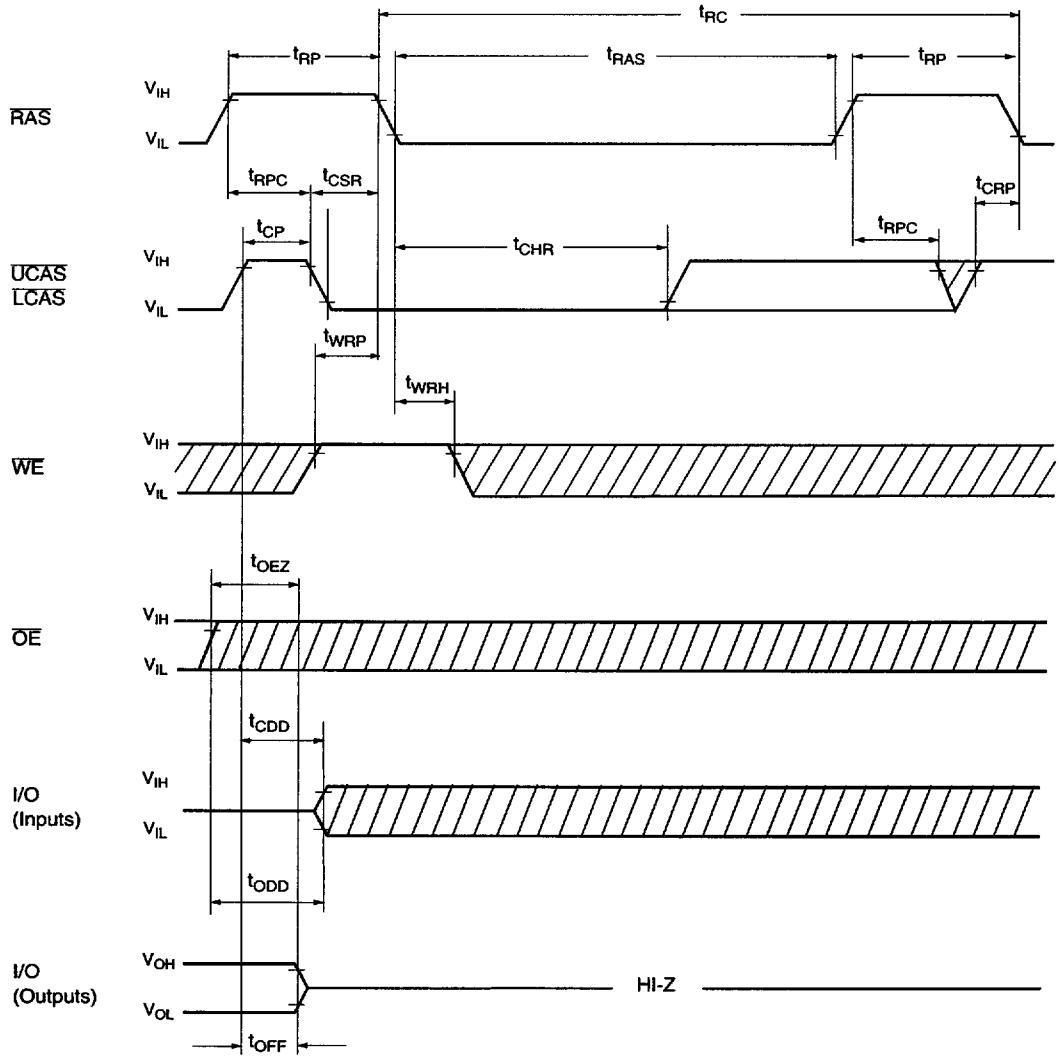
Waveforms of EDO Page Mode Read-Modify-Write Cycle



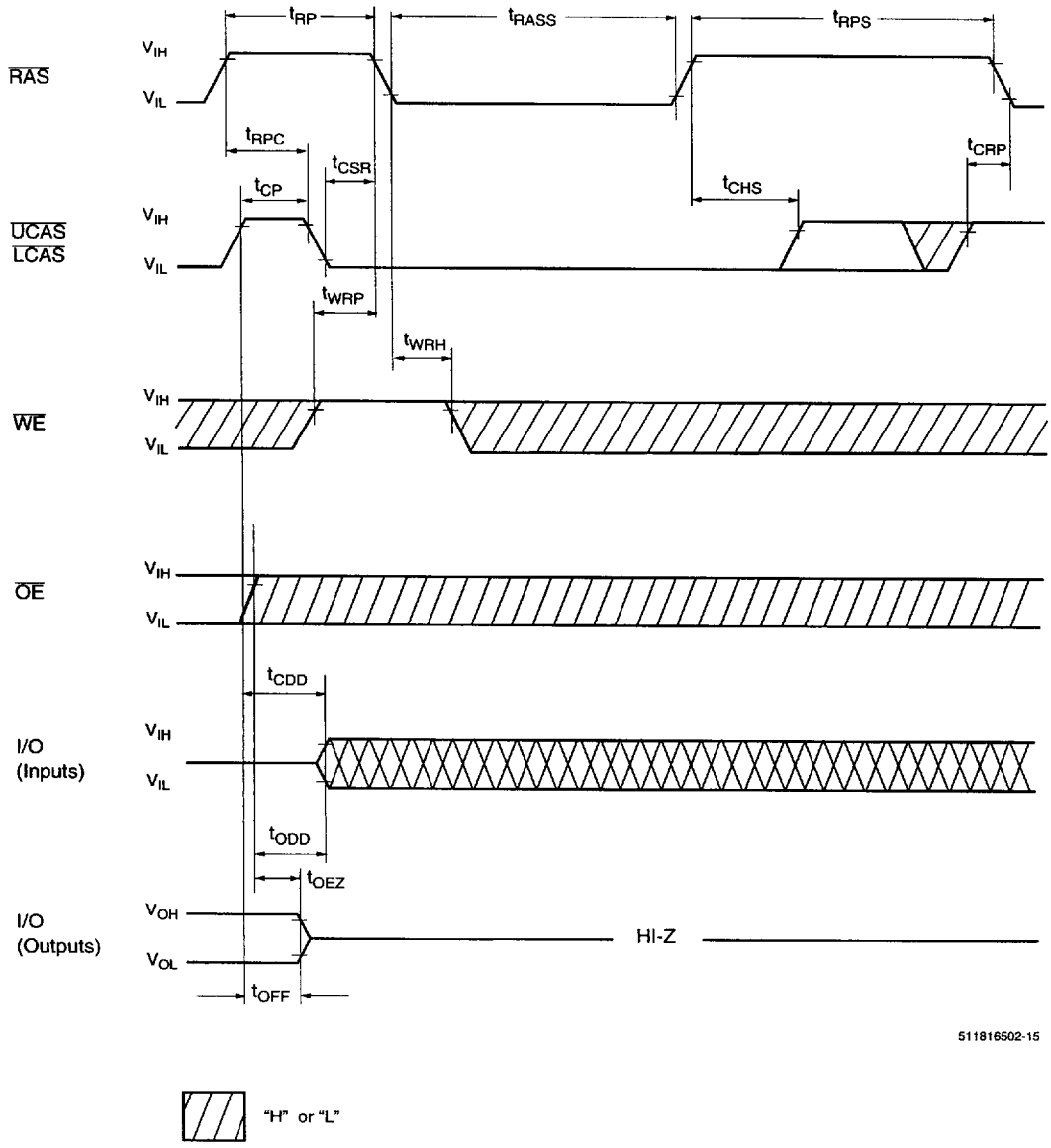
Waveforms of $\overline{RAS}$ Only Refresh Cycle



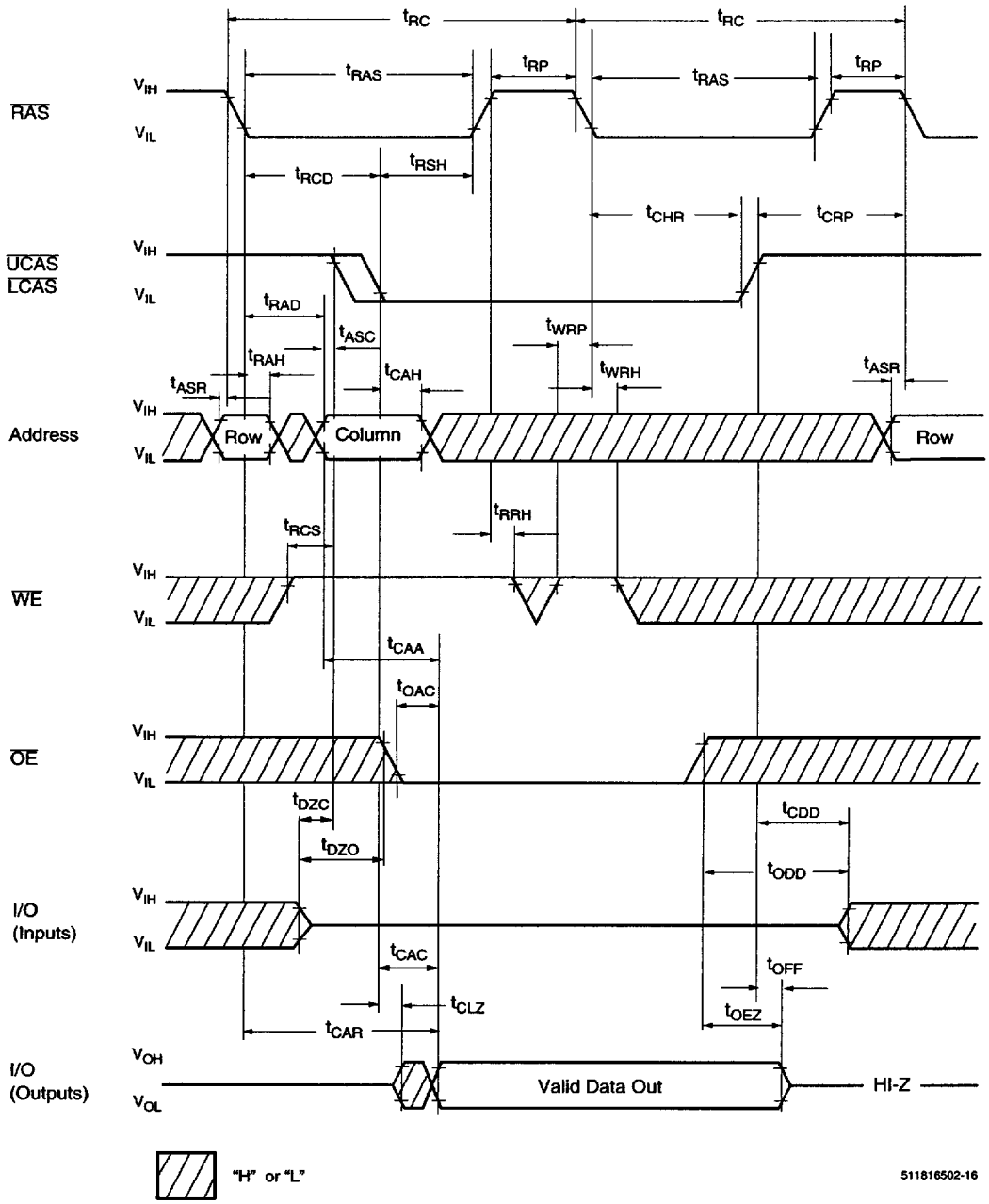
Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle



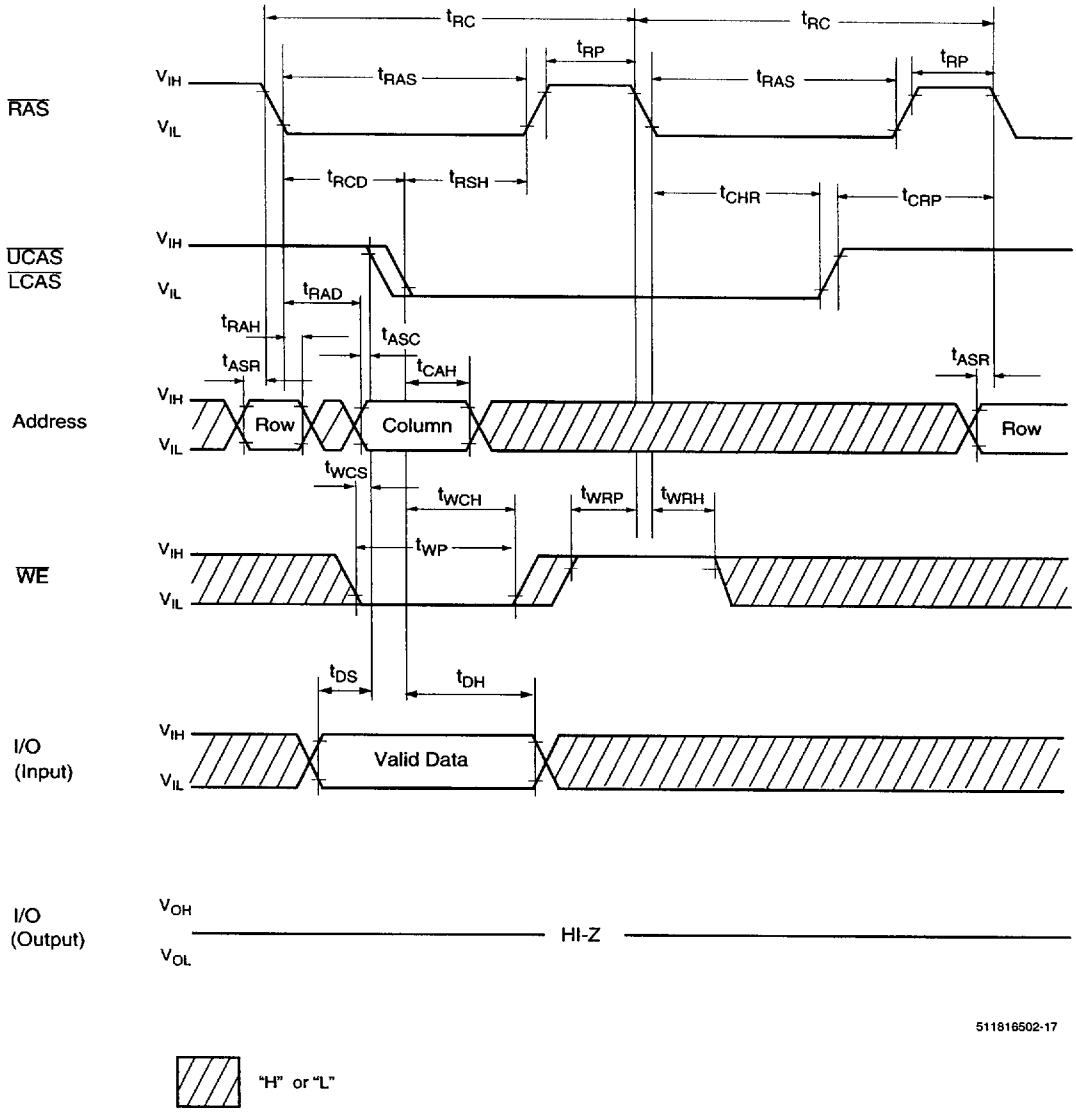
Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Self Refresh Cycle (Optional)



Waveforms of Hidden Refresh Read Cycle



Waveforms of Hidden Refresh Early Write Cycle



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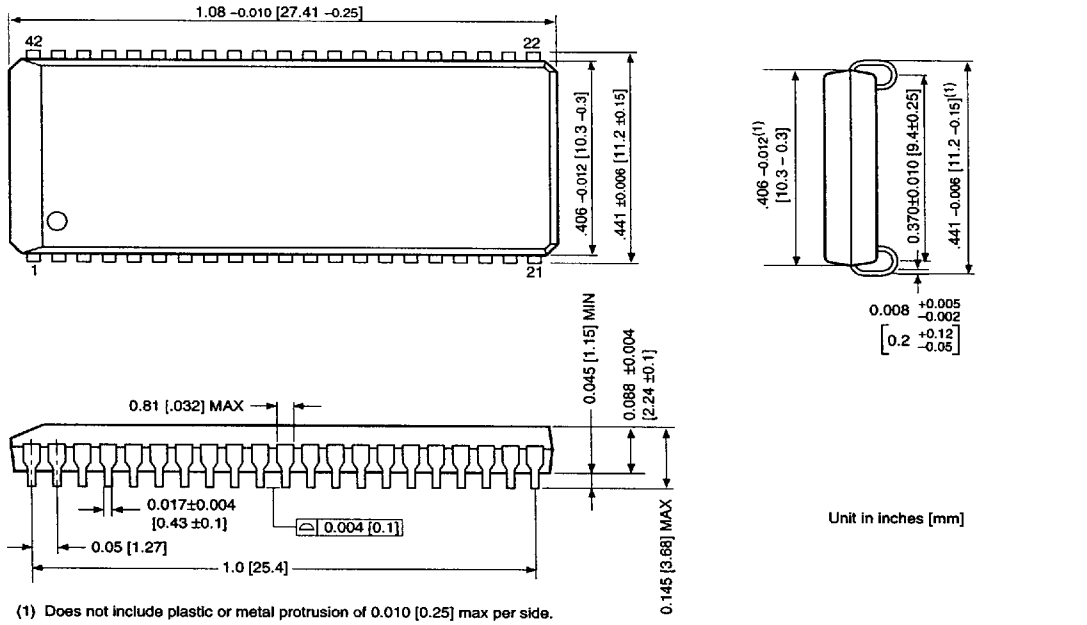
Package Diagrams

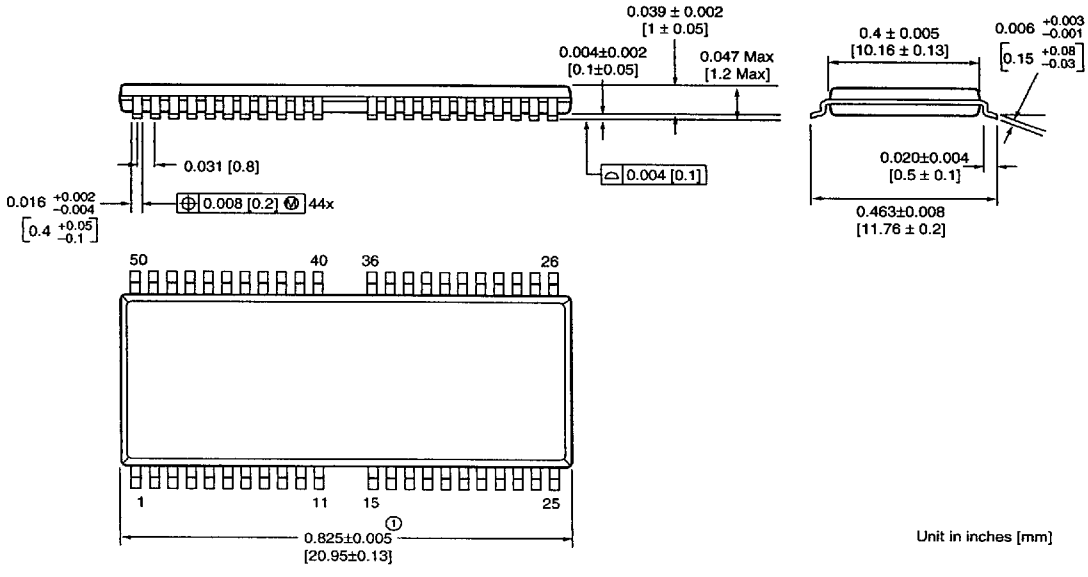
42-Pin 400 mil SOJ



Unit in inches [mm]

(1) Does not include plastic or metal protrusion of 0.010 [0.25] max per side.

44/50-Pin 400 mil TSOP-II



Unit in inches [mm]

① Does not include plastic or metal protrusion of 0.010 [0.25] max. per side