WM2331

10-bit 30MSPS ADC with PGA and Clamp

DESCRIPTION

The WM2331 is a high speed, 10-bit pipeline analogue-to-digital converter (ADC) with on-chip programmable gain amplifier (PGA) and clamp circuit, and internal voltage references. Conversion is controlled by a single clock input.

The device has a high bandwidth differential sample and hold input, which gives excellent common-mode noise immunity and low distortion. Alternatively, it can be driven in single ended fashion with an optional voltage clamp for DC restoration that can take its reference from an on-chip 10-bit DAC or an external source.

The WM2331 provides internal reference voltages for setting the ADC full-scale range without the requirement for external circuitry. However, it can also accept external references for applications where common or high-precision references are required.

A bidirectional 10-bit parallel interface is used both to control the device and to read ADC conversion data. ADC data can be output in unsigned binary or two's complement format. An out-of-range output pin indicates when the input signal is outside the converter's range.

The WM2331 operates with independent analogue and digital supplies of 3V to 5.5V and is supplied in a 28-pin TSSOP package.
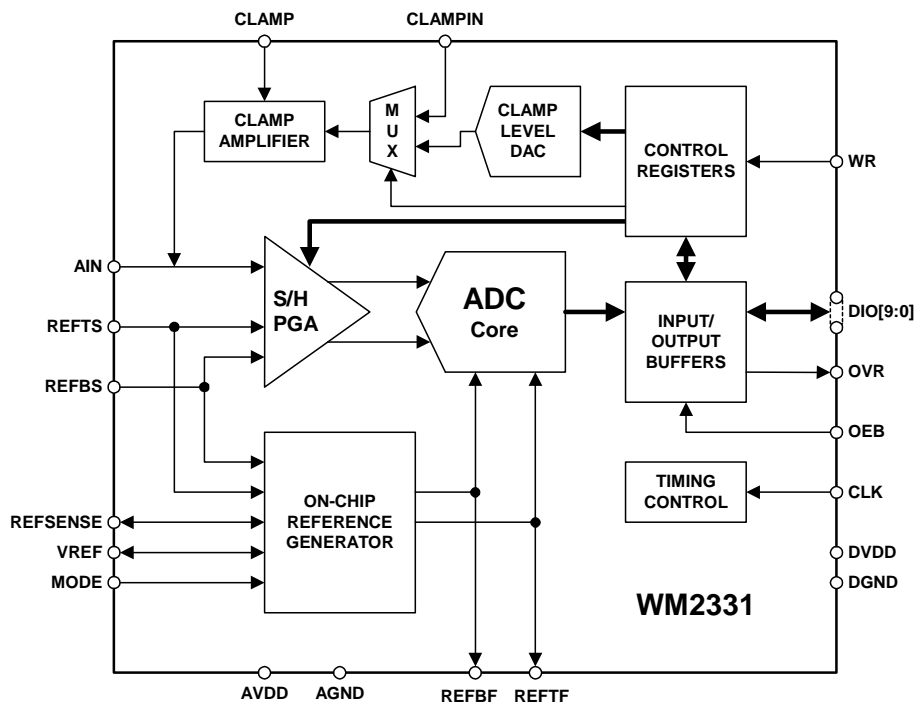
FEATURES

- 10-bit resolution ADC
- 30MSPS conversion rate
- Programmable Gain Amplifier (PGA)
- Built in clamp function (DC restore) with 10-bit DAC
- Adjustable internal voltage references
- Wide Input Bandwidth - 150MHz
- Unsigned Binary or Two's complement output format
- Programmable via parallel interface
- Independent analogue and digital supplies, 3V to 5.5V
- Low power - 92mW typical at 3.0V supplies
- Powerdown mode to 3mW typical
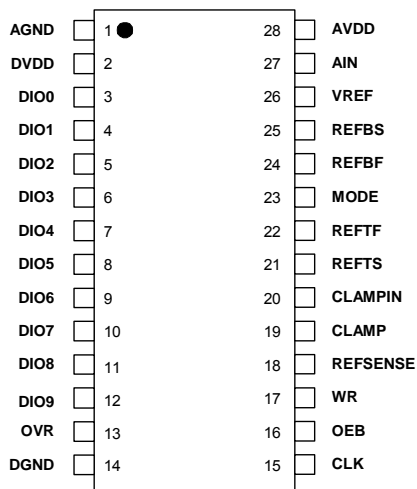- 28-pin TSSOP package

APPLICATIONS

- Composite Video Digitisation
- Digital Copiers
- Digital Video Cameras
- Set Top Box (STB)
- IF and Baseband Digitisation
- Medical Imaging
- High Speed Data Acquisition

BLOCK DIAGRAM

PIN CONFIGURATION

AGND	1 ●	28	AVDD
DVDD	2	27	AIN
DIO0	3	26	VREF
DIO1	4	25	REFBS
DIO2	5	24	REFBF
DIO3	6	23	MODE
DIO4	7	22	REFTF
DIO5	8	21	REFTS
DIO6	9	20	CLAMPIN
DIO7	10	19	CLAMP
DIO8	11	18	REFSENSE
DIO9	12	17	WR
OVR	13	16	OEB
DGND	14	15	CLK

ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE
WM2331CDT/V	0 to +70°C	28-pin TSSOP
WM2331IDT/V	-40 to +85°C	28-pin TSSOP

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	AGND	Ground	Negative Analogue Supply
2	DVDD	Supply	Positive Digital Supply
3	DIO0	Digital Input/Output	Digital input/output bit 0 (LSB)
4	DIO1	Digital Input/Output	Digital input/output bit 1
5	DIO2	Digital Input/Output	Digital input/output bit 2
6	DIO3	Digital Input/Output	Digital input/output bit 3
7	DIO4	Digital Input/Output	Digital input/output bit 4
8	DIO5	Digital Input/Output	Digital input/output bit 5
9	DIO6	Digital Input/Output	Digital input/output bit 6
10	DIO7	Digital Input/Output	Digital input/output bit 7
11	DIO8	Digital Input/Output	Digital input/output bit 8
12	DIO9	Digital Input/Output	Digital input/output bit 9 (MSB)
13	OVR	Digital Output	Overrange output (tri-state)
14	DGND	Ground	Negative Digital Supply
15	CLK	Analogue Input	Clock input
16	OEB	Digital Input	Output enable bar – low to enable DIO[9:0] and OVR
17	WR	Digital Input	Write strobe
18	REFSENSE	Analogue Input	VREF mode control
19	CLAMP	Digital Input	Clamp control – high to enable clamp amplifier
20	CLAMPIN	Analogue Input	Clamp reference input
21	REFTS	Analogue Input/Output	Top reference sense
22	REFTF	Analogue Input/Output	Top reference force
23	MODE	Analogue Input	Input mode select
24	REFBF	Analogue Input/Output	Bottom reference force
25	REFBS	Analogue Input/Output	Bottom reference sense
26	VREF	Analogue Input/Output	Reference voltage
27	AIN	Analogue Input	Analog Input
28	AVDD	Supply	Positive Analogue Supply

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

As per JEDEC specifications A112 and A113, this product requires specific storage conditions prior to surface mount assembly. It has been classified as having a Moisture Sensitivity Level of 2 and as such will be supplied in vacuum-sealed moisture barrier bags.

CONDITION		MIN	MAX
Digital supply voltage, DVDD to DGND		-0.3V	+6.5V
Analogue supply voltage, AVDD to AGND		-0.3V	+6.5V
Supply voltage difference, AVDD to DVDD		-6.5V	+6.5V
Ground difference, AGND to DGND		-0.3V	+0.3V
Voltage range digital inputs (DIO[9:0], WR, CLAMP, OEB)		DGND - 0.3V	DVDD + 0.3V
Voltage range analogue inputs (REFTS, REFBS, REFTF, REFBF, AIN, VREF, REFSENSE, CLK, MODE)		AGND - 0.3V	AVDD + 0.3V
Operating temperature range, T_A	WM2331CDT	0°C	+70°C
	WM2331IDT	-40°C	+85°C
Storage temperature		-65°C	+150°C
Lead temperature (1.6mm from package body for 10 seconds)			+300°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Digital supply range	DVDD		3.0	3.0	5.5	V
Analogue supply range	AVDD		3.0	3.0	5.5	V
Ground	DGND,AGND			0		V
Clock frequency	f_{CLK}		5		30	MHz
Clock duty cycle			45	50	55	%
Operating Free Air Temperature	T_A	WM2331C	0		70	°C
		WM2331I	-40		85	°C

ELECTRICAL CHARACTERISTICS

Test Conditions:
AVDD = DVDD = 3.0V, f_{CLK} = 30MHz, 50% duty cycle, MODE = AVDD, REFTS = 2.5V, REFBS = 0.5V, PGA gain = 1.0,
T_A = T_{MIN} to T_{MAX}, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Accuracy						
Integral nonlinearity	INL			±1.0	±2.0	LSB
Differential nonlinearity	DNL			±0.3	±1.0	LSB
Offset error				0.4	2.0	% of FS
Gain error				1.4	3.5	% of FS
Missing codes		No missing codes guaranteed				
Analogue Input Signal to AIN pin						
Input signal range for unity PGA gain (see Note 1)		MODE = AGND	REFBS		REFTS	V
		MODE = AVDD / 2, V_{CMCS} fixed	V_{CMCS} - VREF/2		V_{CMCS} + VREF/2	
		MODE = AVDD	REFBS		REFTS	
AIN voltage limits			AGND		AVDD	V
Switched input capacitance				1.2		pF
Analogue input bandwidth		-3dB amplitude		150		MHz
DC leakage current		± Full-scale input		±100		µA
Conversion Characteristics						
Conversion frequency	f_{CLK}		5		30	MHz
Pipeline delay				3		cycles of CLK
Aperture delay	t_A			4.0		ns
Aperture jitter				2.0		ps rms
Dynamic Performance						
Effective number of bits	ENOB	f_{IN} = 3.5MHz	8.2	9.0		bits
		f_{IN} = 15MHz		7.7		
Spurious free dynamic range	SFDR	f_{IN} = 3.5MHz	55	60		dB
		f_{IN} = 15MHz		48		
Total harmonic distortion	THD	f_{IN} = 3.5MHz		-58	-54.7	dB
		f_{IN} = 15MHz		-47		
Signal to noise ratio	SNR	f_{IN} = 3.5MHz	51.2	56		dB
		f_{IN} = 15MHz		53		
Signal to noise and distortion ratio	SNDR	f_{IN} = 3.5MHz	51.1	56		dB
		f_{IN} = 15MHz		48		
PGA						
Gain range (linear scale)			0.5		4	V/V
Gain step size (linear scale)				0.5		V/V
Gain error from nominal					3	%
Clamp						
Clamp DAC resolution				10		bits
Clamp DAC output voltage			REFBF		REFTF	V
Clamp DAC DNL			-1		1	LSB
Clamp DAC DNL				±1		LSB
External clamp reference on CLAMPIN			0.1		AVDD - 0.1	V
Clamp output voltage error			-40		40	mV

Test Conditions:
AVDD = DVDD = 3.0V, f_{CLK} = 30MHz, 50% duty cycle, MODE = AVDD, REFTS = 2.5V, REFBS = 0.5V, PGA gain = 1.0,
T_A = T_{MIN} to T_{MAX}, unless otherwise stated.

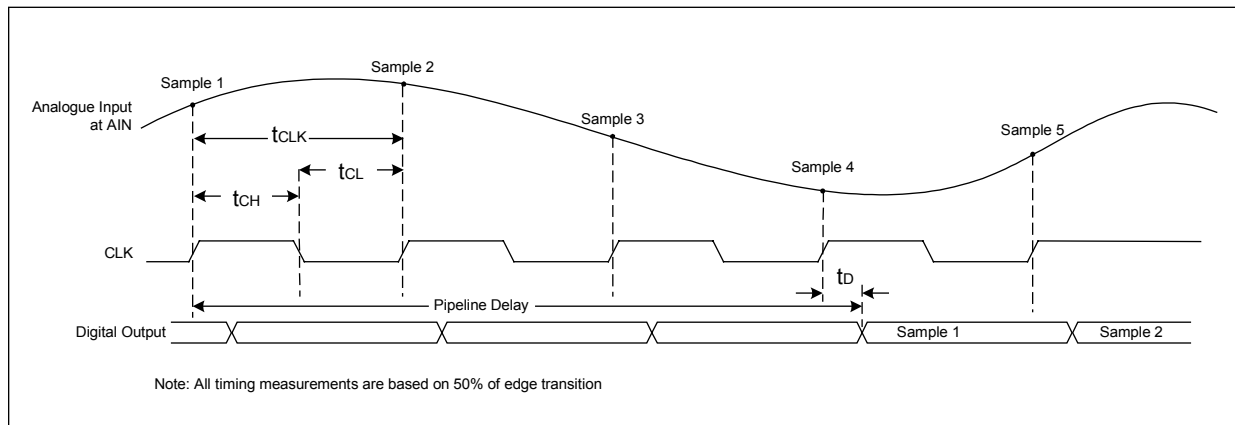| PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Reference Inputs / Outputs in Top/Bottom Mode (MODE=AVDD)						
Bottom reference voltage applied to REFBS			0		AVDD - 1	V
Top reference voltage applied to REFTS			1		AVDD	V
Differential reference input (REFTS – REFBS)	V_{TB}		1		2	V
Reference input common mode (REFTS + REFBS) / 2	V_{CMTB}		0.5		AVDD - 0.5	V
Switched input capacitance on REFBS				0.6		pF
Switched input capacitance on REFTS				0.6		pF
REFBF output voltage				(AVDD - V_{TB})/2		V
REFTF output voltage				(AVDD + V_{TB})/2		V
Analogue Reference Inputs / Outputs in Centre-Span Mode (MODE=AVDD/2)						
Reference voltage derived or applied to VREF			1		2	V
REFBF output voltage				(AVDD - VREF)/2		V
REFTF output voltage				(AVDD + VREF)/2		V
Non-AIN side of differential input applied to REFTS and REFBS	V_{CMCS}	(Note 2)	0.5		AVDD - 0.5	V
Analogue Reference Inputs / Outputs in Full External Reference Mode (MODE=AGND) (Note 3)						
Differential reference voltage applied (REFTF – REFBF)			1		2	V
Reference input common mode (REFTF + REFBF) / 2		AVDD = 3.0V	1.3	1.5	1.7	V
		AVDD = 5.0V	2.0	2.5	3.0	V
Reference input resistance				680		Ω
VREF Input / Output specifications						
Internal 1V reference to VREF		REFSENSE = VREF	0.95	1.0	1.05	V
Internal 2V reference to VREF		REFSENSE = AGND	1.9	2.0	2.1	V
External reference applied to VREF pin in centre-span mode		REFSENSE = AVDD, MODE = AVDD / 2	1		2	V
Input impedance in centre-span mode		REFSENSE = AVDD, MODE = AVDD / 2		18		kΩ

Test Conditions:

AVDD = DVDD = 3.0V, f_{CLK} = 30MHz, 50% duty cycle, MODE = AVDD, REFTS = 2.5V, REFBS = 0.5V, PGA gain = 1.0,
T_A = T_{MIN} to T_{MAX}, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supplies						
Analogue supply current	I_{AVDD}	MODE = AGND, REFSENSE = AVDD		31	45	mA
		MODE = AVDD/2, REFSENSE = VREF		37		mA
		MODE = AVDD, REFSENSE = AVDD		36		mA
Digital supply current	I_{DVDD}	C_L = 10pF		6		mA
Standby power consumption (digital and analogue combined)	I_{VDD}(STBY)			3	5	mW
Digital Logic Levels (CMOS Levels)						
Input LOW level	V_{IL}	(Note 2)			0.2 x VDD	V
Input HIGH level	V_{IH}	(Note 2)	0.8 x VDD			V
Output LOW	V_{OL}	I_{OL} = -50µA			0.2	V
Output HIGH	V_{OH}	I_{OH} = 50µA	VDD – 0.2			V

Notes

1. V_{CMCS} can be applied as a single voltage source to REFTS and REFBS with these two pins connected together. Alternatively the common mode of the input can be set by applying different voltage sources to these two pins, in which case the common mode voltage is effectively the average of these two voltages, V_{CMCS} = (REFTS + REFBS)/2.

2. Digital input and output levels refer to the supply used for the input/output buffer on the relevant pin. CLK and MODE refer to the AVDD supply, all other digital input/output refers to the DVDD supply.

3. In full external reference mode the REFTF and REFTS pins should be shorted together, and the REFBF and REFBS pins should be shorted together. Please refer to device operation examples in the device description section of the datasheet.
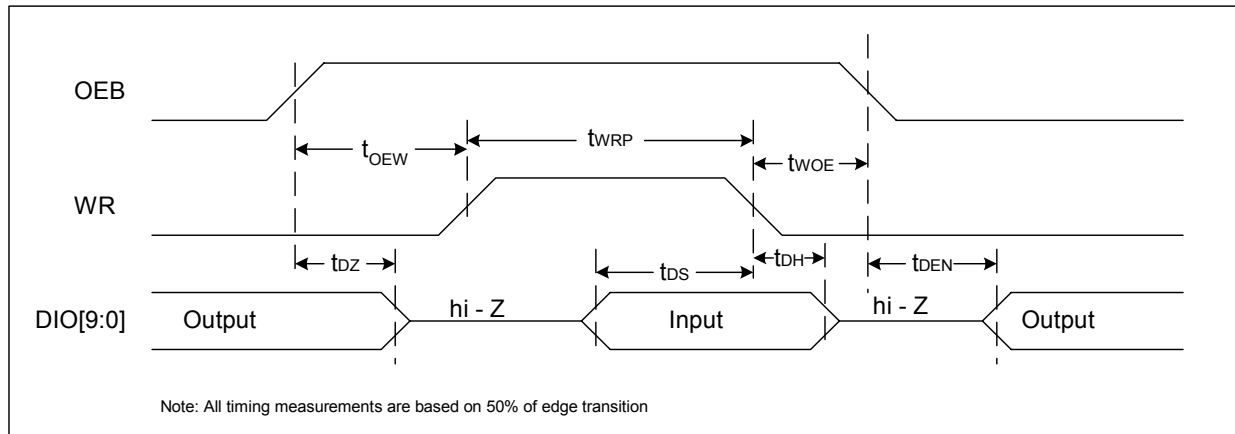
Figure 1 Write Timing

Figure 2 Output Timing

Test Conditions:
AVDD = DVDD = 3.0V, f_{CLK} = 30MHz, 50% duty cycle, MODE = AVDD, REFTS = 2.5V, REFBS = 0.5V, PGA gain = 1.0,
T_A = T_{MIN} to T_{MAX}, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Clock						
Clock period	t_{CLK}		33			ns
Clock high time	t_{CH}		15	16.5		ns
Clock low time	t_{CL}		15	16.5		ns
Timing						
Pipeline delay				3		CLK cycles
Clock to data valid	t_D				25	ns
Output disable to hi-Z output	t_{DZ}		0		20	ns
Output enable to data valid	t_{DEN}		0		20	ns
Output disable to write enable	t_{OEW}		12			ns
Write disable to output enable	t_{WOE}		12			ns
Write pulse width	t_{WRP}		15			ns
Input data setup time	t_{DS}		5			ns
Input data hold time	t_{DH}		5			ns

TYPICAL SYSTEM PERFORMANCE
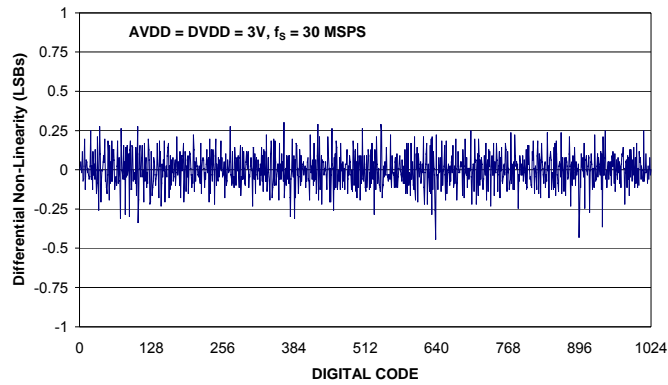
Figure 3 Differential Non-Linearity
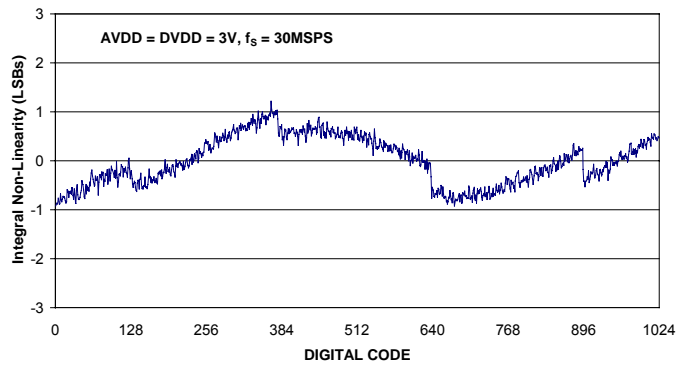
Figure 4 Integral Non-Linearity
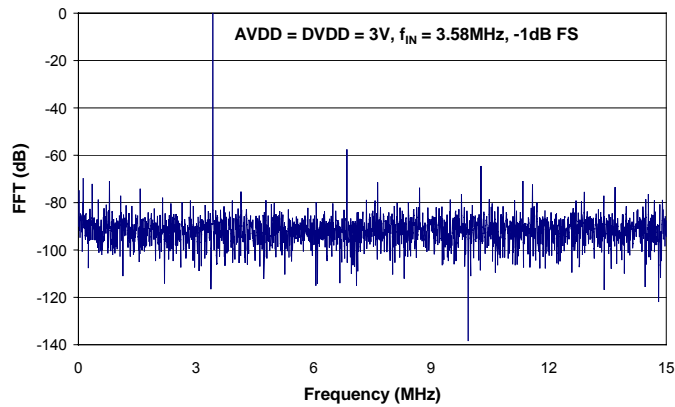
Figure 5 Fast Fourier Transform (FFT)

DEVICE DESCRIPTION

INTRODUCTION

The WM2331 is a high speed analogue-to-digital converter (ADC) with on-chip analogue pre-processing and reference generation, designed for applications such as composite video digitisation, digital copiers and and high speed data acquisition. The chip architecture consists of:

- High bandwidth sample and hold input, which can operate in differential or single-ended mode

- Programmable gain amplifier (PGA)

- Voltage clamp for DC restoration that can take its reference from an on-chip 10-bit DAC or an external source

- 10-bit, 30MSPS pipeline analogue-to-digital converter (ADC) core

- On-chip reference generator and reference buffer (external references can also be used for applications where common or high precision references are required)

- Bidirectional 10-bit parallel interface to read ADC conversion data and control the device. ADC data can be output in unsigned binary or two's complement format. An out-of-range output pin indicates when the input signal is outside the converter's range

ANALOGUE SIGNAL PATH

The WM2331 analogue signal path consists of a DC clamp with a 10-bit clamp level DAC (discussed under 'DC Clamp', below), a high-bandwidth sample and hold unit followed by a programmable gain amplifier (PGA) and a fast 10-bit pipelined analogue to digital converter (ADC core).
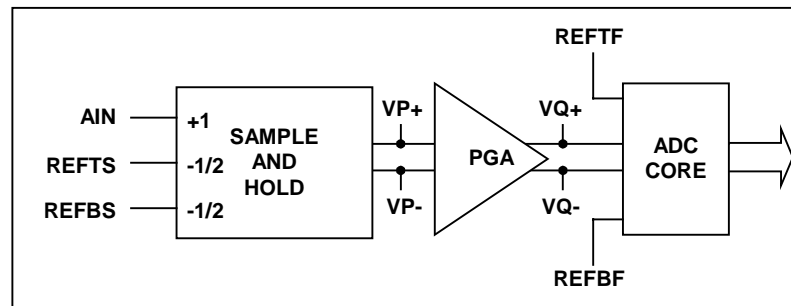
Figure 6 Analogue Input Signal Flow

Figure 6 shows the signal flow through the sample and hold unit and the PGA to the ADC core, where the process of analogue to digital conversion is performed against the ADC reference voltages, REFTF and REFBF (their generation from internal or external reference sources is described later).

SAMPLE AND HOLD

The analogue input voltage V_{IN} is applied to the AIN pin, either DC coupled, AC coupled, or AC coupled with DC restoration using the WM2331 clamp circuit.

The differential sample and hold processes V_{IN} with respect to the voltages applied to the REFTS and REFBS pins, and produces a differential output $V_P = V_{P+} - V_{P-}$ given by:

$$V_P = V_{IN} - V_M \qquad \text{where} \qquad V_M = \frac{REFTS + REFBS}{2}$$

For single-ended input signals, V_M is a constant voltage; usually the AIN mid-scale input voltage. However, in differential mode (see 'ADC Reference Modes', below), REFTS and REFBS can be connected together to operate with AIN as a complementary pair of differential inputs.

PROGRAMMABLE-GAIN AMPLIFIER

V_P is amplified by the PGA and fed into the ADC as a differential voltage $V_Q = V_{Q+} - V_{Q-}$

$$V_Q = Gain \times V_P = Gain \times (V_{IN} - V_M)$$

The PGA gain defaults to 1.0 at power-up, but can be programmed from 0.5 to 4.0 in steps of 0.5.

ANALOGUE-TO-DIGITAL CONVERTER

Regardless of the reference configuration, V_Q is digitised against ADC Reference Voltages REFTF and REFBF, full scale values of V_Q being given by:

$$V_{QFS+} = \frac{REFTF - REFBF}{2} \qquad \text{and} \qquad V_{QFS-} = -\left(\frac{REFTF - REFBF}{2} \right)$$

Attempts to convert V_Q voltages outside the range of V_{QFS-} to V_{QFS+} are signalled to the application by driving the OVR output pin high. If V_Q is less than V_{QFS-}, the ADC output code is 0. If V_Q is greater than V_{QFS+}, the output code is 1023.

SIGNAL CHAIN SUMMARY

Combining the above equations and referring back to the input, the positive and negative full-scale voltages at the AIN pin are:

$$V_{INFS+} = V_M + \frac{REFTF - REFBF}{2 \times Gain} \qquad \text{and} \qquad V_{INFS-} = V_M - \frac{REFTF - REFBF}{2 \times Gain}$$

Therefore the input signal span is given by:

$$V_{INFS+} - V_{INFS-} = \frac{REFTF - REFBF}{Gain}$$

In order to match the ADC input range to the input signal amplitude, REFTF and REFBF should be set such that:

$$REFTF - REFBF = (V_{INFS+} - V_{INFS-}) \times Gain$$

ADC REFERENCE MODES

The WM2331 supports three basic modes of reference generation, selected by the voltage applied to the MODE pin. These are summarised and explained in Table 1.

In differential, Centre Span and Top/Bottom modes, the internally generated ADC references are intened solely for WM2331 internal use and REFTF and REFBF must not be used as voltage references for any other device in the application.

MODE PIN	MODE	FUNCTION	COMMENTS
AGND	Full external	$REFTF = REFTS$ $REFBF = REFBS$	On-chip reference generator and reference buffer are not used.
AVDD/2	Differential	$REFTF = \dfrac{AVDD + V_{REF}}{2}$ $REFTF = \dfrac{AVDD - V_{REF}}{2}$	V_{REF} can be internally or externally generated. REFTS and REFBS are joined together and connected either to the negative end of the input signal (true differential mode) or to the AIN mid-scale voltage (centre-span mode).
AVDD	Top/Bottom	$REFTF = \dfrac{AVDD + (REFTS - REFBS)}{2}$ $REFBF = \dfrac{AVDD - (REFTS - REFBS)}{2}$	On-chip reference generator is not used. Reference buffer centers external reference voltages around AVDD/2.

Table 1 WM2331 Reference Generation Modes

FULL EXTERNAL REFERENCE MODE (MODE = AGND)

When MODE is connected to AGND, the WM2331 operates in full external reference mode. The internal reference buffer is powered down and bypassed, so that the ADC core takes the user-supplied reference voltages at pins REFTS and REFBS (REFTS and REFBS are internally connected to REFTF and REFBF). The mean of REFTF and REFBF must be equal to AVDD/2. Only single-ended input is possible in this mode.
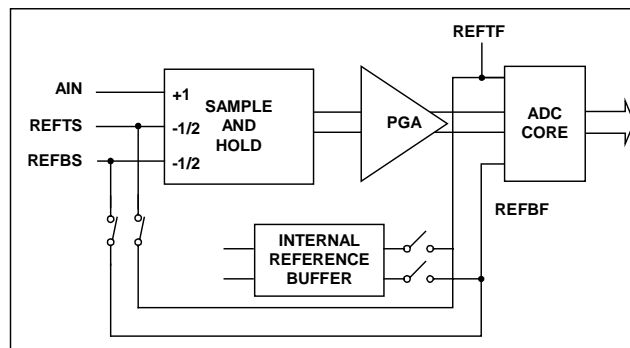
Figure 7 ADC Reference Generation in Full External Mode

The full external mode of operation is useful when the application requires more accurate or lower drift reference voltages than the WM2331 can provide, or when devices need to share common reference voltages for best ADC matching. It also offers the possibility of using REFTS and REFBS as sense lines to drive the REFTF and REFBF lines (**Kelvin mode**) to eliminate any voltage drops from remote references within the system (see Figure 9). In Kelvin configurations, take care when choosing the external op-amps to ensure that they can drive large capacitive loads without oscillating.

Although the on-chip reference generator is not used by the WM2331 in full external mode, its output is available on the VREF pin and can be used by other parts of the system. Note that in addition to the internal connections from REFTS to REFTF and REFBS to REFBF, external wire connections must also be made as shown in Figure 8 to minimise resistance (except in Kelvin mode).
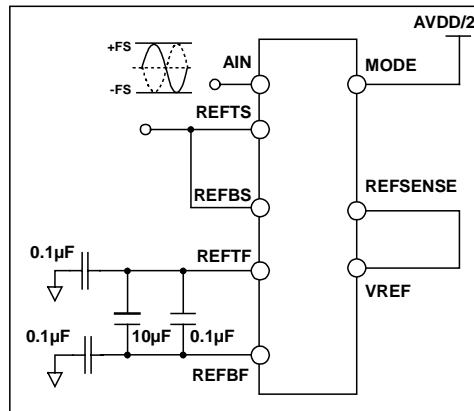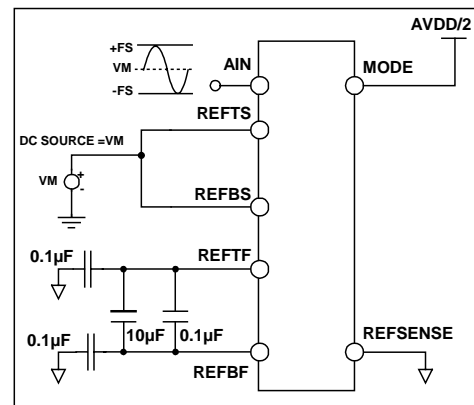
Figure 8 Full External Reference Mode (Reference Generator Disabled)

Figure 9 Full External Mode with Kelvin connections (Reference Generator Disabled)

DIFFERENTIAL MODE (MODE = AVDD/2)

The WM2331 operates in differential mode when the voltage at the MODE pin is AVDD/2 (mid-supply). The ADC reference voltages REFTF and REFBF are generated by the internal reference buffer from V_{REF}. Depending on the connection of the REFSENSE pin, V_{REF} may be supplied by the on-chip reference generator or driven by an external source, as discussed under 'On-chip Reference Voltage Generation', below. REFTF and REFBF are centred around AVDD/2 by the internal reference buffer and the voltage difference between them equals V_{REF}.

Figure 10 ADC Reference Generation in Differential Mode

This mode is suitable for handling differentially presented inputs, which are applied to the AIN and REFTS/REFBS pins. A special case of differential mode is **centre span mode**, in which the user applies a single-ended signal to AIN and applies the mid-scale input voltage (V_M) to the REFTS and REFBS pins.

Figure 11 Differential Mode, 1V Reference Span

Figure 12 Centre Span Mode, 2V Reference Span

TOP/BOTTOM MODE (MODE = AGND)

Top/Bottom mode is enabled by connecting the MODE pin to AVDD. In this mode, the ADC Reference voltages REFTF and REFBF are generated by the internal reference buffer from the externally supplied voltages REFTS and REFBS. Only single-ended input is possible in TOP/BOTTOM Mode.
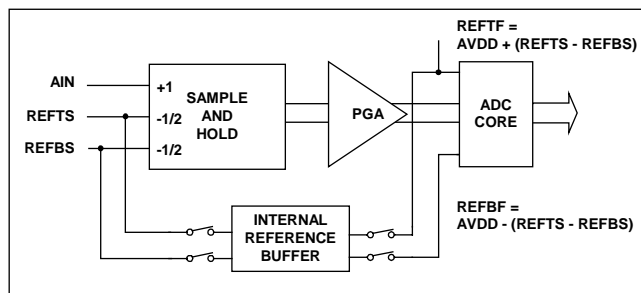
Figure 13 ADC Reference Generation in Top/Bottom Mode

The voltage difference between REFTS and REFBS should equal the peak-to-peak input signal amplitude times the PGA gain (see 'Analogue Signal Path', above). A smaller voltage difference would give rise to out-of-range conditions, whereas a larger one would not fully utilise the ADC resolution. The average of REFTS and REFBS must be the AIN mid-scale voltage, V_M.

Typically, REFSENSE is tied to AVDD to disable the on-chip reference generator, but the user can also choose to use its output to drive either REFTS or REFBS.

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Figure 14 Top/Bottom Mode (Reference Generator Disabled)

ON-CHIP REFERENCE VOLTAGE GENERATOR

The On-chip Reference Generator (ORG) can provide a reference voltage on the VREF pin that is independent of temperature and supply voltage. External connections to the REFSENSE pin control the ORG's output to VREF, as shown in Table 2.

REFSENSE CONNECTION	ORG OUTPUT TO VREF
VREF pin	1 Volt
AGND	2 Volts
External divider junction	$(1 + R_A/R_B)$ Volts – see Figure 15
AVDD	None (VREF becomes input pin)

Table 2 Controlling the On-chip Reference Generator

Connecting REFSENSE to AVDD powers the ORG down, saving power when the ORG function is not required.

In differential mode (MODE = AVDD/2), the voltage on VREF determines the ADC reference voltages as follows:

$$REFTF = \frac{AVDD + V_{REF}}{2}$$

$$REFBF = \frac{AVDD - V_{REF}}{2}$$

$$REFTF - REFBF = V_{REF}$$

When the ORG is enabled, the VREF pin should be decoupled to the circuit board's analogue ground plane close to the WM2331 AGND pin via a 1μF tantalum capacitor and a 0.1μF ceramic capacitor. The ORG can source currents up to 1mA into external grounded loads when it is not used by the WM2331. Typical buffer load regulation is about 0.5Ω.

Figure 15 ORG Operating with External Divider (for Intermediate Reference Voltages)

DC CLAMP
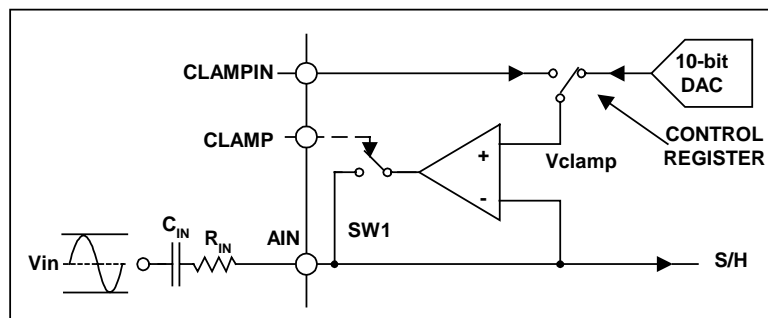
Figure 16 Schematic of Clamp Circuitry

The WM2331 provides a clamp function for restoring the DC reference level of AC coupled input signals. Figure 17 shows an example of using the clamp to restore the black level of a composite video input AC coupled to AIN. While the clamp pin is held high, the clamp amplifier forces the voltage at AIN to equal the clamp reference voltage, setting the DC voltage at AIN for the video black level.
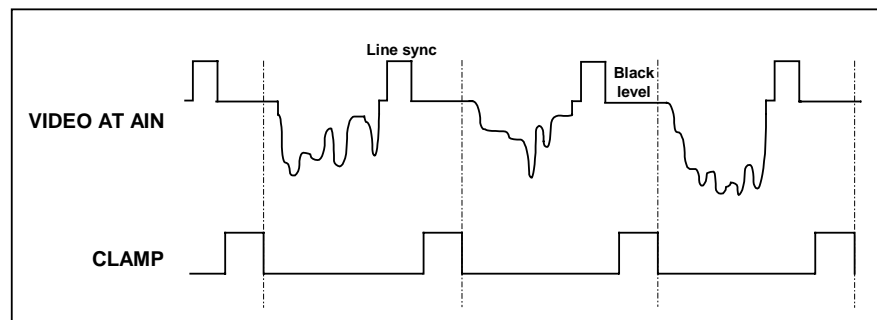
Figure 17 Example Waveforms for Line-Clamping to a Video Input Black Level

After power up, the clamp reference voltage is the voltage supplied on the CLAMPIN pin. However, it can also be generated by the on-chip 10-bit clamp level DAC by suitably programming the WM2331 clamp and control registers (see Digital Control Registers, below).

Clamp design for minimum acquisition time and droop is discussed in Applications Information.

CLAMP DAC OUTPUT VOLTAGE RANGE AND LIMITS

Important: When using the internal clamp DAC in Top/Bottom or Centre Span Mode, the user must ensure that the desired DC clamp level at AIN lies within the voltage range REFBF to REFTF. This is because the clamp DAC voltage is constrained to lie within this range REFBF to REFTF. Specifically:

$$V_{DAC} = REFBF + (REFTF - REFBF) \times (0.006 + 0.988 \times (DAC\ code)/1024)$$

DAC codes can range from 0 to 1023. Figure 18 shows the clamp DAC output voltage versus the DAC code.
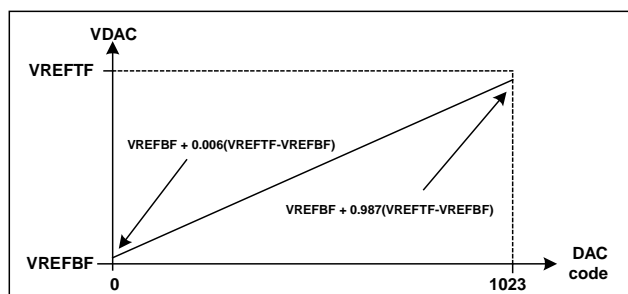
Figure 18 Clamp DAC Output Voltage versus DAC Register Code Value

If the desired DC level at AIN does not lie within the range REFTF to REFBF, then either:

- the CLAMPIN pin can be used instead to provide a suitable reference voltage or
- it may be possible to re-design the application to move the AIN input range into the CLAMP DAC voltage range. This is achieved in both Top/Bottom and Centre Span Modes by shifting both REFTS and REFBS up or down by the voltage through which the AIN input range is to be moved.

DIGITAL CONTROL REGISTERS

The WM2331 contains two clamp registers and a control register for user programming. Binary data can be written into these registers using pins DIO0 to DIO9 and the WR and OEB pins. When writing to a device register, DIO9 and DIO8 select the destination register (see Table 3) and the remaining DIO pins are data bits.

ADDRESS DIO[9:8]	DESCRIPTION	DEFAULT (HEX)	READ/ WRITE	DATA BITS DIO[7:0]							
				DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
00	Clamp Reg. 1	00	RW	DAC[7]	DAC[6]	DAC[5]	DAC[4]	DAC[3]	DAC[2]	DAC[1]	DAC[0]
01	Clamp Reg. 2	00	RW							DAC[9]	DAC[8]
10	Control Reg.	01	RW		CLDIS	TWOC	CLINT	PDWN	PGA[2]	PGA[1]	PGA[0]
11	Reserved										

Table 3 Register Map

WRITING TO THE INTERNAL REGISTERS THROUGH THE DIGITAL I/O BUS

Pulling the OEB pin high disables the data and out-of-range indicator (OVR) pins' output drivers, setting the driver outputs to a high impedance state. This allows control register data to be loaded into the WM2331 by presenting it on the DIO0 to DIO9 pins and pulsing the WR pin high then low to latch the data into the chosen control or DAC register.

The data is latched into the register on the falling edge of the WR pulse (see Figure 1 for timing details). The new device configuration takes effect as soon as the data is latched into the register.

Figure 19 shows an example register write where the clamp DAC code is set to 199 (hex) by writing to clamp registers 1 and 2 (see 'Digital Control Registers', below). Pins DIO0 to DIO7 are driven to the clamp DAC code lower byte (0F hex) and pins DIO8 and DIO9 are both driven to 0 to select clamp register 1 as the data destination. The clamp low-byte data is then loaded into this register by pulsing WR. The top 2 bits of the DAC word are then loaded by driving 01(hex) on pins DIO0 to DIO7 and by driving pin DIO8 to 1 and pin DIO9 to 0 to select clamp register 2 as the data destination. WR is pulsed a second time to latch this second control word into clamp register 2.
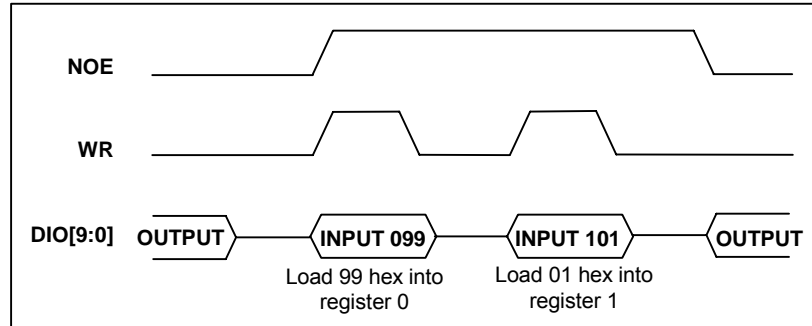
Figure 19 Example Register Write Cycle to Clamp DAC Register

REGISTER	BIT NO	BIT NAME(S)	DEFAULT	DESCRIPTION
Clamp Register 1 DIO[9:8] = 00	7:0	DAC[7:0]	0	Clamp DAC voltage (DAC[0] = LSB.) DAC[9:0] = 00h: Clamp voltage = REFBF DAC[9:0] = 3Fh: Clamp voltage = REFTF
Clamp Register 2 DIO[9:8] = 01	7:2			Unused
	1:0	DAC[9:8]	01	Clamp DAC voltage (DAC[9] = MSB)
Control Register DIO[9:8] = 10	2:0	PGA[2:0]	001	PGA gain: 000 = 0.5 001 = 1.0 010 = 1.5 011 = 2.0 100 = 2.5 101 = 3.0 110 = 3.5 111 = 4.0
	3	PDWN	0	Power down 0 = WM2331 powered up 1 = WM2331 powered down
	4	CLINT	0	Clamp voltage internal/external 0 = external analogue clamp voltage from CLAMPIN pin. 1 = from on-chip DAC (see Clamp Register)
	5	TWOC	0	Output format 0 = unsigned binary 1 = two's complement
	6	CLDIS	0	Clamp Amplifier Disable (for power saving) 0 = Enable 1 = Disable
	7			Unused

Table 4 Register Contents

POWER MANAGEMENT

In power-sensitive applications (such as battery-powered systems) where the WM2331 ADC is not required to convert continuously, power can be saved between conversion intervals by placing the WM2331 into Power Down mode. This is achieved by setting bit 3 (PDWN) of the control register to 1. In Power Down mode, the device typically consumes less than 3mW of power. Power down mode is exited by resetting control register bit 3 to 0. On power up from long periods of power down, the WM2331 typically requires 5ms of wake up time before valid conversion results are available.

In systems where the ADC must run continuously, but where the clamp is not required, the supply current can be reduced by approximately 1.2mA by setting the control register bit 6 (CLDIS), which disables the clamp circuit. Similarly, when REFSENSE is tied to AVDD, the reference generator is disabled and supply current reduced by approximately 1.2mA.

DATA OUTPUT FORMAT

While the OEB pin is held low, ADC conversion results are output at the data I/O pins DIO0 (LSB) to DIO9 (MSB). The default output data format is unsigned binary (output codes 0 to 1023). This can be switched to two's complement format (output codes -512 to 511) by setting control register bit 5 (TWOC) to 1.

APPLICATIONS INFORMATION

DRIVING THE CLOCK INPUT

Obtaining good performance from the WM2331 requires care when driving the clock input.

Different sections of the Sample-and-Hold and ADC operate while the clock is low or high. The user should ensure that the clock duty cycle remains near 50% to ensure that all internal circuits have as much time as possible in which to operate.

The CLK pin should also be driven from a low jitter source for best dynamic performance. To maintain low jitter at the CLK input, any clock buffers external to the WM2331 should have fast rising edges. Use a fast logic family such as AC or ACT to drive the CLK pin, and consider powering any clock buffers separately from any other logic on the PCB to prevent digital supply noise appearing on the buffered clock edges as jitter.

As the CLK input threshold is nominally around AVDD/2, any clock buffers need to have an appropriate supply voltage to drive above and below this level.

DRIVING THE SAMPLE AND HOLD INPUTS

DRIVING THE AIN PIN

Figure 20 shows an equivalent circuit for the WM2331 AIN pin. The load presented to the system at the AIN pin comprises the switched input sampling capacitor, C_{Sample}, and various stray capacitances, C_{P1} and C_{P2}.
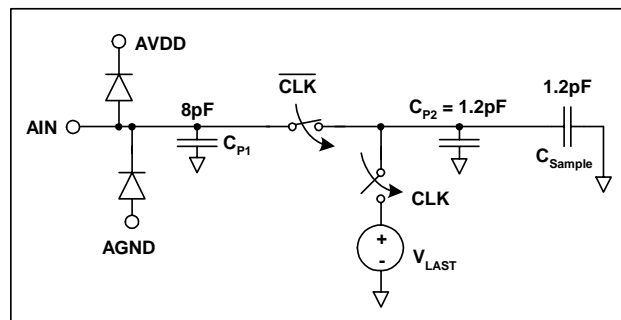
Figure 20 Equivalent Circuit for Analogue Input Pin AIN

The input current pulses required to charge C_{Sample} can be time averaged and the switched capacitor circuit modelled as an equivalent resistor

$$R_{IN2} = \frac{1}{C_S \times f_{CLK}}$$

where C_S is the sum of C_{Sample} and C_{P2} (see Figure 21). This model can be used to approximate the input loading versus source resistance for high impedance sources.
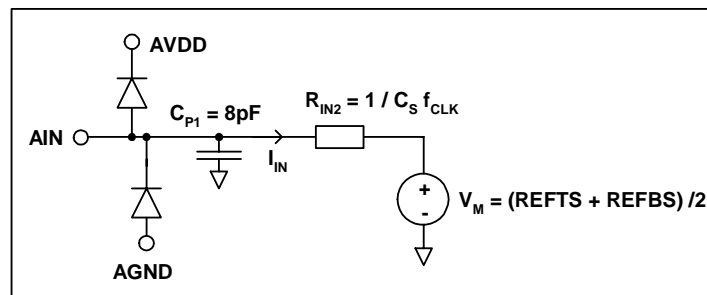
Figure 21 Equivalent Circuit for the AIN Switched Capacitor Input

AIN INPUT DAMPING

The charging current pulses into AIN can make the signal source jump or ring, especially if the source is slightly inductive at high frequencies. Inserting a small series resistor of 20Ω or less in the input path can damp source ringing (see Figure 22). The resistor can be made larger than 20Ω if reduced input bandwidth or distortion performance is acceptable.
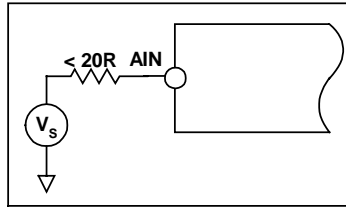
Figure 22 Damping Source Ringing Using a Small Resistor

DRIVING THE SAMPLE & HOLD REFERENCE INPUTS

The sample and hold reference inputs (connected to pins REFTS and REFBS) present switched-capacitor loads similar to the AIN pin, but with smaller capacitors (see Figure 23 below). Note that in Top/Bottom mode, the internal reference buffer is also driven from REFTS and REFBS and the total load on these pins is therefore the parallel combination of the sample and hold circuit and the reference buffer.
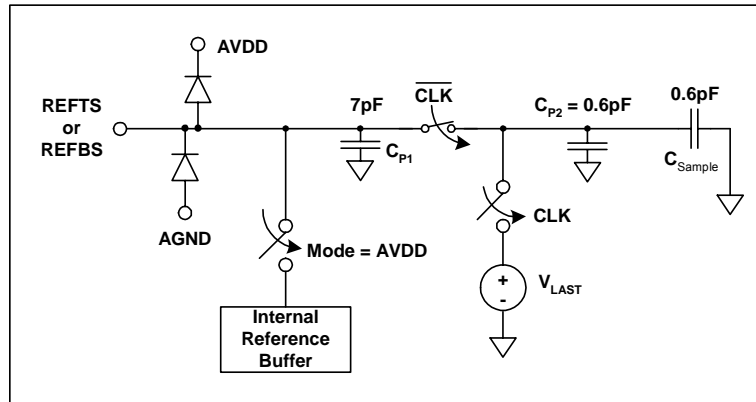
Figure 23 Equivalent Circuit of REFTS and REFBS Sample & Hold Inputs

DRIVING THE INTERNAL REFERENCE BUFFER

DRIVING THE VREF PIN (DIFFERENTIAL MODE)

Figure 24 shows the equivalent load on the VREF pin when driving the internal reference buffer via this pin (MODE = AVDD/2 and REFSENSE = AVDD).
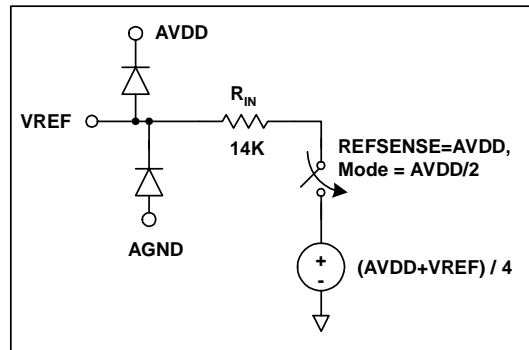
Figure 24 Equivalent Circuit of VREF

The input current I_{REF} is given by

$$I_{REF} = \frac{3V_{REF} - AVDD}{4 \times R_{IN}}$$

Tolerance on this current is $\pm$ 30 % or greater. The user should ensure that VREF is driven from a low noise, low drift source, well-decoupled to analogue ground and capable of driving I_{REF}.

DRIVING THE INTERNAL REFERENCE BUFFER (TOP/BOTTOM MODE)

Figure 25 shows the loading on the REFTS and REFBS pins in Top/Bottom mode due to the internal reference buffer. Note that the sample and hold circuit must also be driven via these pins, which adds additional load (see Driving the Sample & Hold Reference Inputs, above).
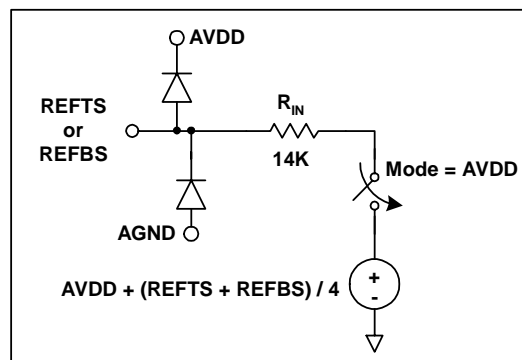
Figure 25 Equivalent Circuit of Inputs to Internal Reference Buffer

The input currents are given by:

$$I_{INTS} = \frac{3REFTS - AVDD - REFBS}{4 \times R_{IN}}$$

and

$$I_{INBS} = \frac{3REFBS - AVDD - REFTS}{4 \times R_{IN}}$$

These currents must be provided by the sources on REFTS and REFBS in addition to the requirements of driving the sample and hold.

DRIVING REFTF AND REFBF (FULL EXTERNAL REFERENCE MODE)
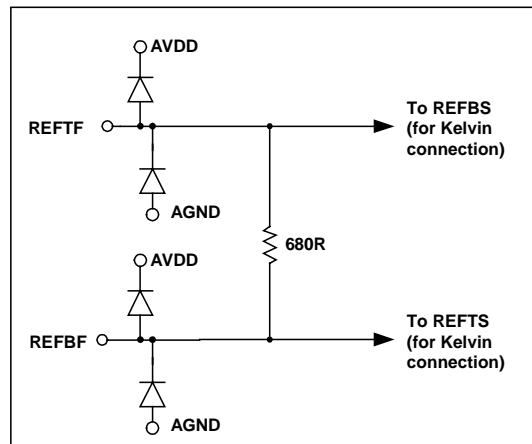
Figure 26 Equivalent Circuit of REFTF and REFBF Inputs

DESIGNING THE DC CLAMP

Figure 16 (in Device Description) shows the basic operation of the clamp circuit with the analog input AIN coupled via an RC circuit. The clamp voltage output level may be established by an analog voltage on the CLAMPIN pin or by programming the on-chip clamp DAC.

INITIAL CLAMP ACQUISITION TIME

Initial acquisition time is defined as the time required to reach the target clamp voltage at AIN when the clamp switch SW1 is closed for the first time (clamp re-acquisition during normal operation is discussed in Steady-state Clamp Voltage Error, below). This time is given by

$$T_{ACQ} = C_{IN} \times R_{IN} \times \ln\left(\frac{V_C}{V_E}\right)$$

where Vc is the difference between the DC level of the input V_{IN} and the target clamp output voltage, V_{Clamp}. V_E is the difference between the ideal Vc and the actual Vc obtained during the acquisition time. The maximum tolerable error depends on the application requirements.

For example, consider clamping an incoming video signal that has a black level near 0.3V to a black level of 1.3V at the WM2331 input. The voltage V_C required across the input coupling capacitor is thus 1.3 - 0.3 = 1V. If a 10mV or less clamp voltage error V_E will give acceptable system operation, the source resistance Rin is 20Ω and the coupling capacitor Cin is 1μF, then the total clamp pulse duration required to reach this error is:

$$T_{ACQ} = 1\mu F \times 20\Omega \times \ln(1/0.01) = 92\mu s \ \ (\text{approx.})$$

Note that during continuous operation, the clamping time would typically be much shorter, as the voltage difference wolud be smaller (depending on droop, see next section.

Initial acquisition can be performed in two ways:

- Pulsing the CLAMP pin as in normal operation. Provided that clamp droop (see below) is negligible, initial acquisition is complete when the total clamped (CLAMP = HIGH) time equals T_{ACQ}.
- Pulling the CLAMP pin high for the required acquisition time before starting normal operation. This method is faster.

CLAMP DROOP

The charging currents drawn by the Sample-and-Hold switched capacitor input can charge or discharge C_{IN}, causing the DC voltage at AIN to drift towards V_M (the average of REFTS and REFBS) during the time between clamp pulses. This effect is called clamp droop.

Voltage droop is a function of the AIN input current to the WM2331, I_{IN}, and the time between clamp intervals, t_D:

$$V_{DROOP} \approx \left(\frac{I_{IN}}{C_{IN}}\right) \times t_D \quad \text{(approx.)}$$

Worst case droop between clamping intervals occurs for maximum input bias current. Maximum input current is I_{INFS}, which occurs when the input level is at its maximum or minimum.

For example, at 30 MSPS I_{INFS} is approximately 40µA for a 2V input range at AIN (see 'Driving the Sample and Hold Reference Inputs, above, to calculate I_{IN}). Note that I_{INFS} may vary from this by $\pm$ 30% because of processing variations and voltage dependencies. Designs should allow for this variation. If the time t_D between clamping intervals is 63.5µs and C_{IN} is 1µF then the maximum clamp level droop between clamp pulses is

$$V_{DROOP} = 40µA / 1µF \times 63.5µs = 2.5mV \text{ (approx.)}$$

$$= 1.25LSB \text{ at PGA gain=1, 2V ADC references}$$

If this droop is greater than can be tolerated in the application, then increase C_{IN} to slow the droop and hence reduce the voltage change between clamp pulses.

If a high leakage capacitor is used for coupling the input source to the AIN pin then the droop may be significantly worse than calculated above. Avoid using electrolytic and tantalum coupling capacitors as these have higher leakage currents than non-polarised capacitor types. Electrolytic and tantalum capacitors also tend to have higher parasitic inductance, which can cause problems at high input frequencies.

STEADY-STATE CLAMP VOLTAGE ERROR

During the clamp pulse (CLAMP = HIGH), the DC voltage on AIN is refreshed from the clamp voltage. Provided that droop is not excessive, clamping fully reverses the effect of droop. However, using very short clamp pulses with long intervals between pulses (t_D) can result in a steady-state voltage difference, V_{COS}, between the DC voltage at AIN and Vclamp.

Figure 27 shows the approximate voltage waveform at AIN resulting from a a large clamp droop during t_D and clamp voltage re-acquisition during the clamp pulse time, t_C.
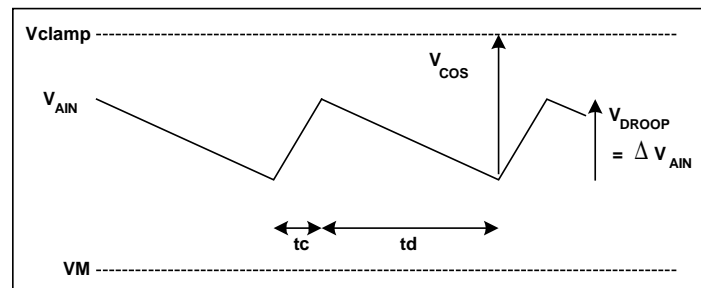
Figure 27 Approximate Waveforms at AIN During Droop and Clamping

The voltage change at AIN during acquisition has been approximated as a linear charging ramp by assuming that almost all of V_{COS} appears across R_{IN}, giving a charging current V_{COS}/R_{IN} (this is a reasonable approximation when V_{COS} is large enough to be of concern). The voltage change at AIN during clamp acquisition is then

$$\Delta V_{AIN} = \frac{V_{COS} \times t_D}{R_{IN} \times C_{IN}}$$

The peak-to-peak voltage variation at AIN must equal the clamp droop voltage at steady state. Equating the droop voltage to the clamp acquisition voltage change gives

$$V_{COS} = \frac{R_{IN} \times I_{IN} \times t_D}{t_C}$$

Thus for low offset voltage, keep R_{IN} low, design for low droop and ensure that the ratio t_D/t_C is not unreasonably large.

REFERENCE DECOUPLING

VREF PIN

When the on-chip reference generator is enabled, the VREF pin should be decoupled to the circuit board's analogue ground plane close to the WM2331 AGND pin via a 1µF tantalum capacitor and a 0.1µF ceramic capacitor.

REFTF AND REFBF PINS

In any mode of operation, the REFTF and REFBF pins should be decoupled as shown in Figure 28 below. Use short board traces between the WM2331 and the capacitors to minimise parasitic inductance.
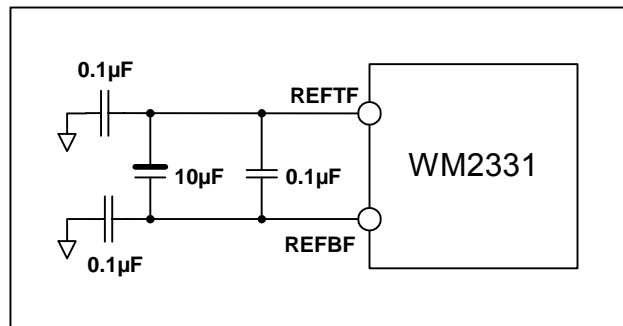

Figure 28 Recommended Decoupling for the ADC Reference Pins REFTF and REFBF

SUPPLY DECOUPLING

The analogue (AVDD, AGND) and digital (DVDD, DGND) power supplies to the WM2331 should be separately decoupled for best performance. Each supply needs at least a 10µF electrolytic or tantalum capacitor (as a charge reservoir) and a 100nF ceramic type capacitor placed as close as possible to the respective pins (to suppress spikes and supply noise).

DIGITAL OUTPUT LOADING AND CIRCUIT BOARD LAYOUT

The WM2331 outputs are capable of driving rail-to-rail with up to 20pF of load per pin at 30MHz clock and 3V digital supply. Minimising the load on the outputs will improve WM2331 signal-to-noise performance by reducing the switching noise coupling from the WM2331 output buffers to the internal analogue circuits. The output load capacitance can be minimised by buffering the WM2331 digital outputs with a low input capacitance buffer placed as close to the output pins as physically possible, and by using the shortest possible tracks between the WM2331 and this buffer.

Noise levels at the output buffers, which may affect the analogue circuits within WM2331, increase with the digital supply voltage. Where possible, consider using the lowest DVDD that the application can tolerate.

Use good layout practices when designing the application PCB to ensure that any off-chip return currents from the WM2331 digital outputs (and any other digital circuits on the PCB) do not return via the supplies to any sensitive analogue circuits. The WM2331 should be soldered directly to the PCB for best performance. Socketing the device will degrade performance by adding parasitic socket inductance and capacitance to all pins.

USER TIPS FOR OBTAINING BEST PERFORMANCE FROM THE WM2331

- Choose differential input mode for best distortion performance.
- Choose a 2V ADC input span for best noise performance.
- Choose a 1V ADC input span for best distortion performance.
- Drive the clock input CLK from a low-jitter, fast logic stage, with a well-decoupled power supply and short PCB traces.

PACKAGE DIMENSIONS

DT: 28 PIN TSSOP (9.7 x 4.4 x 1.0 mm)   **DM022.A**
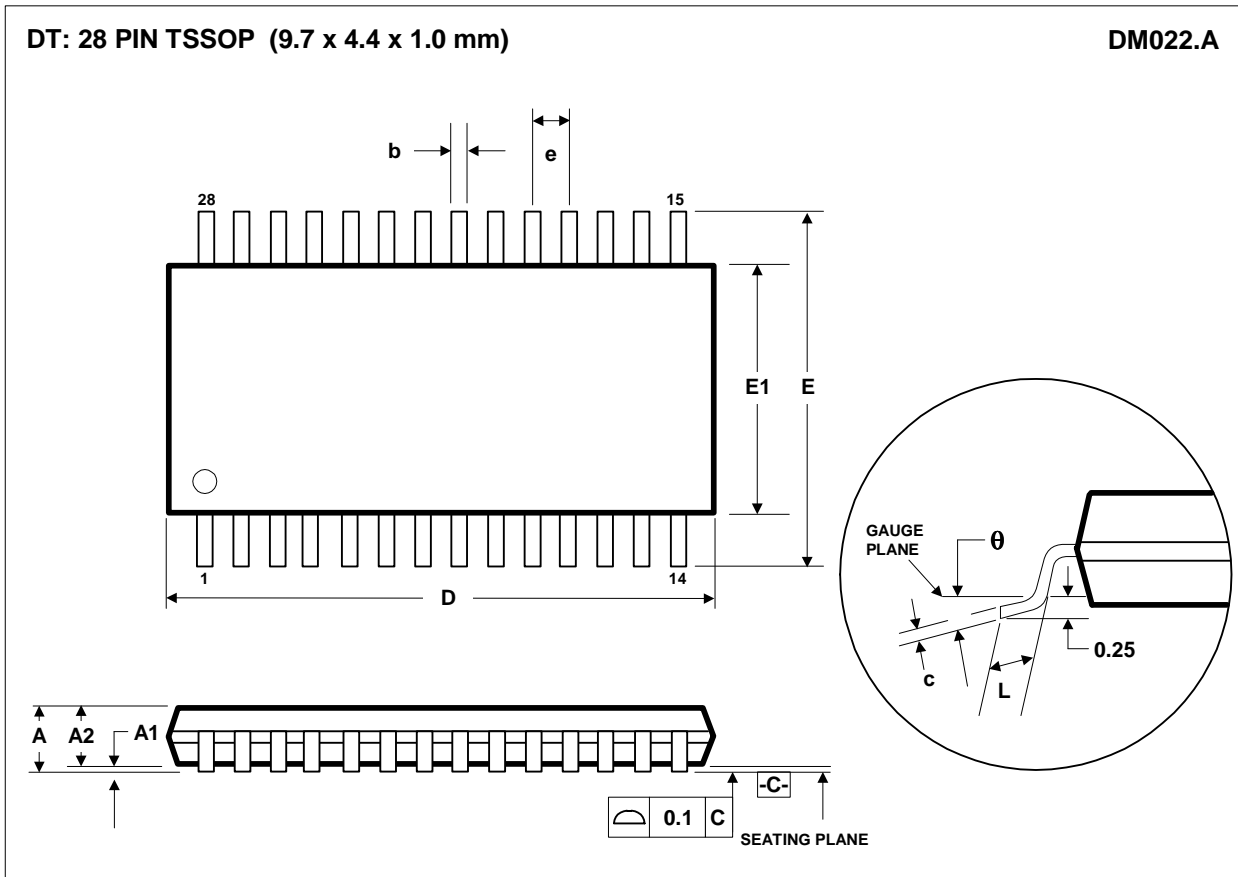
Symbols	Dimensions (mm)		
	MIN	**NOM**	**MAX**
A	-----	-----	1.20
A$_1$	0.05	-----	0.15
A$_2$	0.80	1.00	1.05
b	0.19	-----	0.30
c	0.09	-----	0.20
D	9.60	9.70	9.80
e	0.65 BSC		
E	6.4 BSC		
E$_1$	4.30	4.40	4.50
L	0.45	0.60	0.75
θ	0°	-----	8°
REF:	JEDEC.95, MO-153		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM.
D. MEETS JEDEC.95 MO-153, VARIATION = AE. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

IMPORTANT NOTICE

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