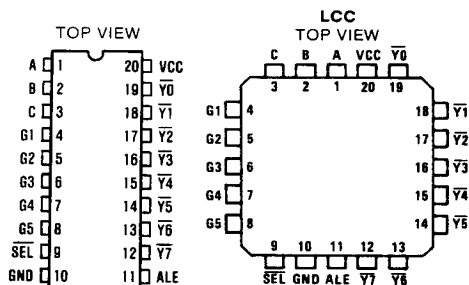


## Programmable Chip Select Decoder (PCSD™)

### Features

- Memory or I/O Chip Select Decoding, Replaces 3-6 ICs
- Superset of the Industry Standard 74138
- Microprocessor Bus Oriented Interface
- Harris Advanced Scaled SAJI IV CMOS Process
- Faster than Low-Power Schottky at CMOS Power Consumption
- 20 Pin Slimline DIP
- Wide Operating Temperature Ranges:
  - ▶ HPL-82C338-5.....0°C to +75°C
  - ▶ HPL-82C338-9.....-40°C to +85°C
  - ▶ HPL-82C338-8.....-55°C to +125°C
- Simple Programming Algorithm
- Mask Programmable for Volume Users

### Pinouts



### Description

The HPL-82C338 is a high performance Programmable Chip Select Decoder (PCSD) which is intended to be used for both memory and I/O chip select decoder applications. Utilizing the Harris advanced scaled SAJI IV CMOS process, this circuit provides bipolar speed with CMOS power consumption.

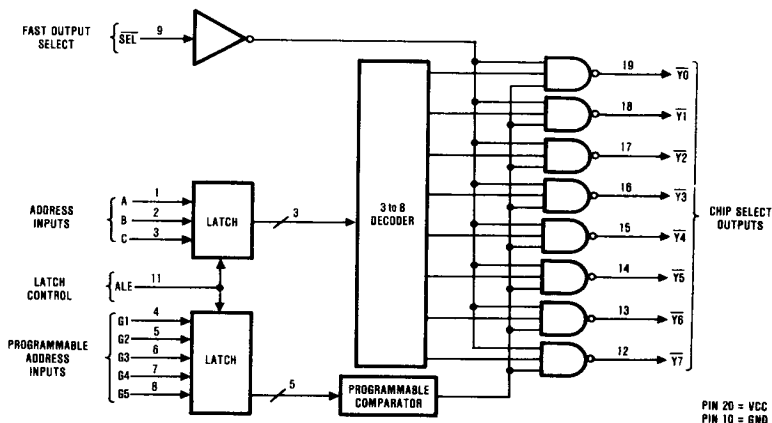
In a typical application, this circuit can replace six 74HCXX SSI/MSI ICs. The associated reductions in board area, chip count and power consumption result in a substantial increase in system reliability and an attendant decrease in system cost. A speed improvement of a factor of four over an equivalent implementation with 74HCXX logic is also realized. The faster decode provided by the

82C338 can result in improved system performance or a dramatic reduction in total system cost since less expensive, slower memories and I/O devices can be used.

The five "Gx" inputs are field programmable for either high or low true address decoding. The Harris fuse link technology used in this product provides a permanent fuse with stable storage characteristics over the full temperature ranges of 0°C to +75°C, -40°C to +85°C and -55°C to +125°C.

Transparent latches are utilized on all address inputs which permits the 82C338 to be used with both multiplexed and non-multiplexed address/data bus microprocessors.

### Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

# Specifications HPL-82C338

HPL-82C338

## Absolute Maximum Ratings

Supply Voltage .....	+7.0 Volts
Input, Output or I/O Voltage Applied .....	GND -0.3V to VCC +0.3V
Storage Temperature Range .....	-65°C to +150°C
Maximum Package Power Dissipation .....	1 Watt
$\theta_{JA}$ .....	24°C/W (CERDIP Package), 19°C/W (LCC Package) 29°C/W (Plastic DIP Package)
$\theta_{JC}$ .....	81°C/W (CERDIP Package), 76°C/W (LCC Package) 75°C/W (Plastic DIP Package)
Gate Count .....	500 Gates
Junction Temperature .....	+150°C
Lead Temperature (Soldering, Ten Seconds) .....	+275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

## Operating Conditions

Operating Voltage Range .....	+4.5V to +5.5V
Operating Temperature Range	
HPL-82C338-5 .....	0°C to +70°C
HPL-82C338-9 .....	-40°C to +85°C
HPL-82C338-8 .....	-55°C to +125°C

## D.C. Electrical Specifications

(Operating)	HPL-82C338-5 (VCC = 5.0V $\pm$ 10%, TA = 0°C to +75°C)
	HPL-82C338-9 (VCC = 5.0V $\pm$ 10%, TA = -40°C to +85°C)
	HPL-82C338-8 (VCC = 5.0V $\pm$ 10%, TA = -55°C to +125°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
IIH	Dedicated "1"		+1	$\mu$ A	VIH = VCC MAX
IIL	Input Current "0"		-1	$\mu$ A	VIL = 0V VCC = VCC MAX
VIH	Input Threshold "1"	2.0		V	VCC = VCC MAX HPL-82C338-5/-9
VIL	Voltage "0"	2.2	0.8	V	VCC = VCC MAX HPL-82C338-8
VOH1	Output Voltage "1"	3.0		V	IOH1 = -5mA
VOH2	"1"	VCC-0.4		V	IOH2 = -1mA
VOL	Output Voltage "0"		0.4	V	VCC MIN, VIL MAX, VIH MIN
ICCSB*	Standby Power Supply Current		50	$\mu$ A	IOL = +5mA
ICCOP*	Operating Power Supply Current		2	mA/MHz	VIH = VCC MAX
					IF = 0.0 $\mu$ A, VCC = VCC MAX
					VI = VCC or GND
					IF = 0.0 $\mu$ A, VCC = VCC MAX

\* ICCSB, ICCOP specifications are achieved only after complete programming of the device. These specifications are sampled and guaranteed but not 100% tested. While testing these specifications, output pins should be left open circuit.

## A.C. Switching Specifications

(Operating)	HPL-82C338-5 (VCC = 5.0V $\pm$ 10%, TA = 0°C to +75°C)
	HPL-82C338-9 (VCC = 5.0V $\pm$ 10%, TA = -40°C to +85°C)
	HPL-82C338-8 (VCC = 5.0V $\pm$ 10%, TA = -55°C to +125°C)

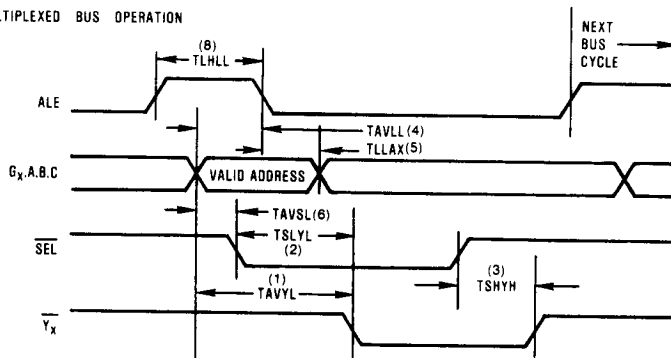
SYMBOL	PARAMETER	HPL-82C338-5		HPL-82C338-9		HPL-82C338-8		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
(1) TAVYL	Propagation delay A, B, C, or G to Output Low	—	50	—	50	—	50	ns
(2) TSLYL	Select Access Time to Output Low	—	35	—	35	—	35	ns
(3) TSHYH	Select Access Time to Output High	—	35	—	35	—	35	ns
(4) TAVLL	Address Set-Up to ALE Trailing Edge	15	—	15	—	15	—	ns
(5) TLLAX	Address Hold From ALE Trailing Edge	15	—	15	—	15	—	ns
(6) TAVSL	Address Set-Up to SEL Low (Glitch-Free Operation)	15	—	15	—	15	—	ns
(7) TSHAX	Address Hold From SEL High (Glitch-Free Operation)	15	—	15	—	15	—	ns
(8) TLHLL	ALE Pulse Width	15	—	15	—	15	—	ns

**Capacitance**  $T_A = +25^\circ\text{C}$  (NOTE: Sampled and guaranteed - but not 100% tested.)

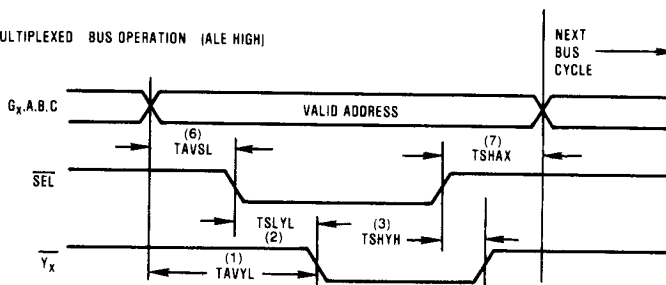
SYMBOL	PARAMETER	TYP	UNITS	TEST CONDITIONS
CI	Input Capacitance	5	pF	$V_I = V_{CC}$ or GND, $f = 1\text{ MHz}$
CO	Output Capacitance	10	pF	$V_O = V_{CC}$ or GND, $f = 1\text{ MHz}$

### Switching Time Definitions

MULTIPLEXED BUS OPERATION

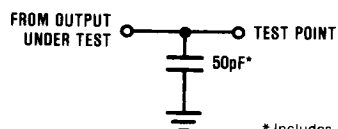


DEMUTIPLEXED BUS OPERATION (ALE HIGH)



- NOTES: 1. In order to ensure glitch-free operation of the  $\overline{Y}_x$  outputs, set-up and hold times should be observed.  
2. AC switching characteristics are measured with inputs switching between GND and 3.0V.  $t_r, t_f = 5\text{ ns}$  (10% -90%).

### A.C. Test Load



\* Includes Jig and Probe Total Capacitance.

## Programming

Following is the programming procedure which is used for the HPL-82C338 programmable logic device. This device is manufactured with all fuses intact. Any desired fuse can be programmed by following the simple procedure shown on the following page. One may build a pro-

grammer to satisfy the specifications described in the table, or use any of the commercially available programmers which meets these specifications. Please contact Harris for a list of approved programmers.

## Programming Specifications

TABLE 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
VCCP	VCC Voltage During Programming		11.50	12.00	12.00	V
VCCV	VCC Voltage During Verify		4.75	5.00	5.25	V
ICCP	ICC Limit During Programming		—	100	200	mA
VNEG	Edit Enable & Mode Select Voltage		-6.00	-6.00	-7.00	V
INEG	Edit Enable & Mode Select Current		—	—	-5.00	mA
VIL	Input Voltage Low		0.00	0.00	0.80	V
VIHV	Input Voltage High	verify	VCCV-2	VCCV	VCCV	V
VIHP	Input Voltage High	programming	VCCP-2	VCCP	VCCP	V
IILP	Input Current Low	VIL = 0.0V	—	0	1	μA
IIHV	Input Current High	verify	—	0	1	μA
IIHP	Input Current High	programming	—	0	1	μA
PWP	Programming Width		4.5	5.0	5.5	msec
TD	Pulse Seq. Delay		1	1	—	μsec
tr1	Signal Rise Time	10% to 90%	0.01	0.1	1	μsec
tr2	VCC Rise Time	10% to 90%	0.01	0.1	5	μsec
tf1	Signal Fall Time	90% to 10%	0.01	0.1	1	μsec
tf2	VCC Fall Time	90% to 10%	0.01	0.1	5	μsec
TPP	Programming Period		—	5.1	—	msec
FL	Fuse Attempts/Link		1	1	2	cycles

① Inputs defined as logic "1" (VIHV or VIHP) must track the VCC power supply when the supply is raised or lowered. The input levels should never exceed the level on the VCC Pin.

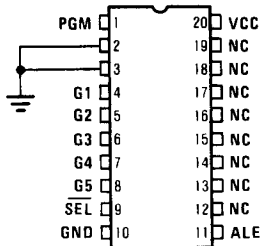


FIGURE 1. HPL-82C338 EDIT MODE PINOUT

NOTE: While programming the CMOS HPL device, no input pins should be left floating. Output pins (12-19) should be left unconnected. It is suggested that a 0.1μF capacitor be placed between VCC and GND to minimize VCC voltage spikes.

## Programming Procedure

### 1. Set Up:

- During programming or operation, no input pins should be left floating.
- No input pin voltage should ever be greater than the voltage applied to the device VCC pin.
- The device should be decoupled with a 0.1  $\mu$ F or greater capacitor located at the device socket and placed between the VCC and GND pins.

### 2. Power up:

- Initially, all input pins including power supply pins should be at ground potential.
- Normally, the input pins (pins 4-9, 11) are driven with an open collector driver with a pull-up resistor to the VCC pin (pin 20) so that these inputs automatically track the voltage on the VCC pin when they are set to the high state. This prevents the voltage level on the input pins from exceeding the voltage applied to the VCC pin.
- Ramp the VCC pin (pin 20) to VCCV and the input pins (pins 4-9, 11) to VIH.

### 3. Programming Sequence

- After a delay  $T_D$ , the programming mode is entered by taking the programming enable pin (pin 1) to VNEG. Pin 1 must remain at VNEG throughout the entire programming sequence.
- Wait  $T_D$  and raises pin 20 to VCCP and pins 4-8, 11 to VIH. At the same time, the SEL input (pin 9) is set to either VIH or VIL in order to select the desired polarity of the input which is to be programmed. When SEL is at VIH, the input will be programmed high true. When SEL is at VIL, the input will be programmed low true.

- Wait  $T_D$  and pulse the input to be programmed to ground for PWP milliseconds. It should be noted that only one input should be programmed at a time.
- After a delay  $T_D$ , return pin 20 to VCCV and pins 4-8, 11 to VIH.
- Repeat steps b), c), and d) until pins 4-8 have been programmed with the appropriate polarity.
- When all inputs have been programmed as explained above, wait  $T_D$  and return the programming enable pin (pin 1) to VIL.

### 4. Fuse Integrity Testing

- Correct programming of the device should be verified by applying test vectors to the input pins.
- Fuse integrity is tested by applying VCC to the device and measuring the static power consumption of the device. With all inputs at VCC or GND and the output pins unloaded, the measured ICCSB of the device should be less than 50  $\mu$ A at VCC = 5V and T = 25°C. This guarantees that all fuses have been blown to a final state which is not marginal and will not create a reliability problem over the life of the device.  
NOTE: Any device which fails this test should be rejected even if it passes functional testing in order to ensure no future reliability problems associated with marginally blown fuses.

**IMPORTANT:** All five inputs must be programmed regardless of desired high or low input polarity. The advanced design of the fuse select circuitry (Patent Pending) provides for ultra-low post programming ICCSB and requires that one fuse on each input be programmed.

## Programming Waveforms

