Dual/Quad Low Noise High Speed Precision Op Amps

DESCRIPTION

The LT1124M/883 dual and LT1125M/883 quad are high performance op amps that offer higher gain, slew rate, and bandwidth than the industry standard OP-27 and competing OP-270/OP-470 op amps. In addition, the LT1124M/883 and LT1125M/883 have lower I_B and I_{OS} than the OP27; lower V_{OS} and noise than the OP-270/OP-470.

In the design, processing, and testing of these devices, particular attention has been paid to the optimization of the entire distribution of several key parameters. Power comsumption of the LT1124M/883 is one half of two OP-27s.

For a decompensated version of these devices, with three times higher slew rate and bandwidth, please see the LT1126/LT1127 data sheet.

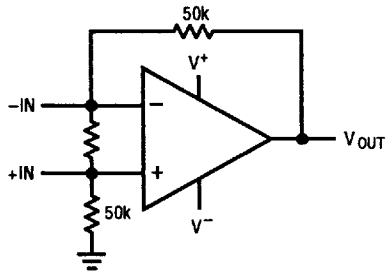
The devices are processed to the requirements of MIL-STD-883 Class B to yield circuits usable in precision military applications.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Input Voltage ..... Equal to Supply Voltage
Output Short Circuit Duration ..... Indefinite
Differential Input Current (Note 1) .....±25mA
Operating Temperature Range
  LT1124AM/883, LT1124M/883
  LT1125AM/883, LT1125M/883 ..... −55°C to 125°C
Storage Temperature Range
  All Grades ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

Protected by U.S. patents 4,775,884 and 4,837,496.

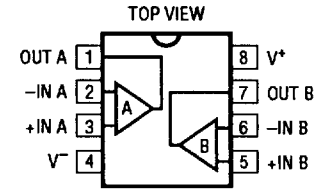
BURN-IN CIRCUIT



LT1124M/883	LT1125M/883
V_{CC} = ±22V	V_{CC} = ±16V
T_A = 125°C	T_A = 125°C
T_{JA} = 153°C	T_{JA} = 154°C

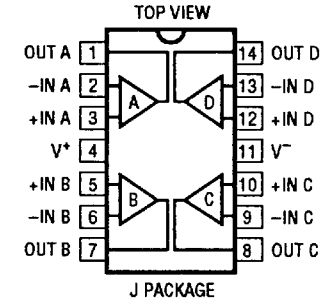
1124/25M/883 BI

PACKAGE/ORDER INFORMATION



J8 PACKAGE
8-LEAD CERAMIC DIP
T_{JMAX} = 160°C, θ_{JA} = 100°C/W

ORDER PART NUMBER
LT1124AMJ8/883
LT1124MJ8/883
PART MARKINGS†
LT1124AMJ8/883C
LT1124MJ8/883C



J PACKAGE
14-LEAD CERAMIC DIP
T_{JMAX} = 160°C, θ_{JA} = 80°C/W

ORDER PART NUMBER
LT1125AMJ8/883
LT1125MJ8/883
PART MARKINGS†
LT1125AMJ8/883C
LT1125MJ8/883C

† The suffix letter "C" of the part mark indicates compliance per MIL-STD-883, para 1.2.1.1.

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of circuits as described herein will not infringe on existing patent rights.

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TABLE 1: ELECTRICAL CHARACTERISTICS

VS = ±15V, T_A = 25°C, unless otherwise noted.(Note 1)

SYMBOL	PARAMETER	CONDITIONS	NOTES	LT1124AM/883 LT1125AM/883 MIN	TYP	MAX	LT1124M/883 LT1125M/883 MIN	TYP	MAX	SUB-GROUP	UNITS
V_{OS}	Input Offset Voltage	LT1124 LT1125				70 90			100 140	4 4	µV µV
I_{OS}	Input Offset Current	LT1124 LT1125				15 20			20 30	1 1	nA nA
I_B	Input Bias Current					±20			±30	1	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz	3			200					nV_{P-P}
	Input Noise Voltage Density	f_O = 10Hz f_O = 1000Hz				5.5 4.2			5.5 4.2		$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
V_{CM}	Input Voltage Range		4	±12.0			±12.0				V
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±12V		112			106			1	dB
PSRR	Power Supply Rejection Ratio	V_S = ±4V to ±18V		116			110			1	dB
A_{VOL}	Large-Signal Voltage Gain	$R_L \geq 10k$, V_O = ±10V $R_L \geq 2k$, V_O = ±10V		5.0 2.0			3.0 1.5			4 4	V/µV V/µV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k$		±13.0			±12.5			4	V
SR	Slew Rate	$R_L \geq 2k$	2	3.0			2.7			7	V/µs
I_S	Supply Current per Amplifier					2.75			2.75	1	mA
V_S = ±15V, −55°C ≤ T_A ≤ 125°C, unless otherwise noted.											
V_{OS}	Input Offset Voltage	LT1124 LT1125				170 190			250 290	2,3 2,3	µV µV
I_{OS}	Input Offset Current	LT1124 LT1125				45 55			60 70	2,3 2,3	nA nA
I_B	Input Bias Current					±55			±70	2,3	nA
V_{CM}	Input Voltage Range		4	±11.3			±11.3				V
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±11.3V		106			100			2,3	dB
PSRR	Power Supply Rejection Ratio	V_S = ±4V to ±18V		110			104			2,3	dB
A_{VOL}	Large-Signal Voltage Gain	$R_L \geq 10k$, V_O = ±10V $R_L \geq 2k$, V_O = ±10V		3.0 1.0			2.0 0.7			5,6 5,6	V/µV V/µV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k$		±12.5			±12.0			5,6	V
SR	Slew Rate	$R_L \geq 2k$	2	2.3			2.0			8A, 8B	V/µs
I_S	Supply Current per Amplifier					3.25			3.25	2,3	mA

Note 1: The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±1.4V, the input current should be limited to 25mA.

Note 2: Slew rate is measured in A_V = −1; input signal is ±7.5, output measured at ±2.5V.

Note 3: 0.1Hz to 10Hz noise can be inferred from the 10Hz noise voltage density test. See the test circuit and frequency response curve for 0.1Hz to 10Hz tester in the Applications Information section of the LT1007 or LT1028 data sheets.

Note 4: This parameter guaranteed by CMRR test.

TABLE 2: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
Final Electrical Test Requirements (Method 5004)	1*,2,3
Group A Test Requirements (Method 5005)	1,2,3
Group C and D End Point Electrical Parameters (Method 5005)	1,2,3

* PDA Applies to subgroup 1. See PDA Test Notes.

PDA Test Notes

The PDA is specified as 5% based on failures from group A, subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883 Class B. The verified failures of group A, subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.

Linear Technology Corporation reserves the right to test to tighter limits than those given.

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