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T-42-21

THOMSON SEMICONDUCTORS

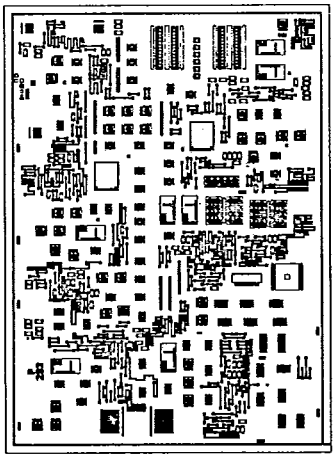
POLY-USE A
POLY-USE G

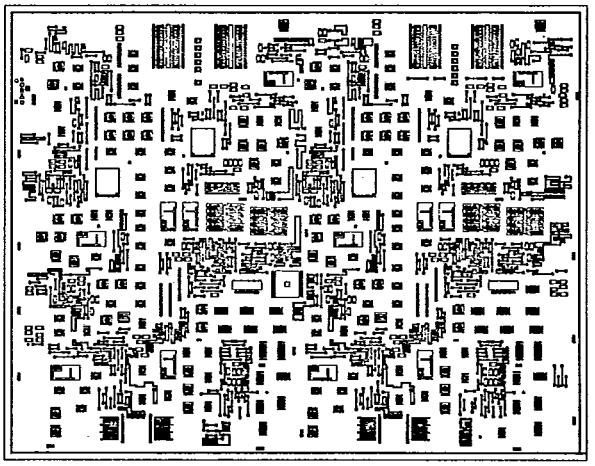
LINEAR COMPONENT ARRAYS

The THOMSON SEMICONDUCTORS **linear component arrays** are semicustom bipolar integrated circuits that contain an array of uncommitted discrete transistors, resistors and capacitors. A user can interconnect these individual components on second level metal to form a custom linear integrated circuit.

- 20 volt (max) supply operation
- Standard NPN f_T = 550 MHz typ.
- Wide variety of NPN and PNP transistor types on each array
- Base, pinched-base, and emitter resistors (10 ohm to 100K ohm)
- MOS and junction capacitors
- 2 layer metalization for ease of interconnect
- Digitized customer layout sheet for computer-aided routing

A unique feature of the POLY-USE A and G array is the two level metalization which simplifies routing, increases the percent utilization of the components on the array and provides improved electrical characteristics. First level metal is a standard, predefined pattern that provides low resistance distribution of the positive and negative supply voltages across the chip. All custom interconnection and routing is done on second level metal along a predefined routing grid which automatically maintains the proper metal pitch. All contact vias to the individual components and to the first level metal supply voltages lie on intersection points of this grid. This two layer system reduces layout time by a factor of 3 over single layer arrays and up to 90% of the components on the array may be utilized. Computer assisted layout, available as an option, further simplifies and speeds up layout and reduces the risk of errors.





POLY-USE A

- 150 X 106 mil die size (3.8 x 2.7mm)
- 424 components
- 24 pins max
- ≤20 Volt supply max
- 14,16,24 pin plastic or ceramic DIP

POLY-USE G

- 192 X 152 mil die size (4.88 x 3.85mm)
- 835 components
- 40 pins max
- ≤20 Volt supply max
- 22,24,28,40 pin plastic or ceramic DIP

Ref. 00695

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THOMSON COMPONENTS

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TABLE I — Summary of Components on POLY-USE A and G

CIRCUIT COMPONENTS	DESCRIPTION	A	G
NPN Transistors	QN1 — Standard 10 mA NPN	46	92
	QN2 — High frequency NPN (rbb' = 150 ohm)	12	23
	QN3 — Low noise NPN (rbb' = 70 ohm)	2	4
	QN4 — 100 mA NPN	2	4
	QN5 — Standard 10 mA NPN with merged PN junction capacitor (C2)	7	12
	Total NPN Transistors	69	135
PNP Transistors	QP6 — Standard lateral PNP (1 mA)	32	60
	QP7 — Multiple lateral PNP (5X)	1	2
	QP8 — Multiple lateral PNP (16X)	2	4
	QP9 — Substrate PNP (1 mA)	1	2
	QP10 — High Current Substrate PNP (5 mA)	2	4
	Total PNP Transistors	38	72
DIODES	D1 — P+N+ Zener	3	0
CAPACITORS	C1 — MOS Capacitor (8 pf)	2	4
	C2 — PN junction (merged with QN5)	7	12
	C3 — P+N+ isolated junction	1	2
	C4 — P+N+ junction (P+ connected to substrate)	1	1
	Total Capacitors	11	19
RESISTORS	P Base 100 ohm	24	45
	220 ohm	34	65
	470 ohm	41	83
	1 K ohm	70	142
	2.2K ohm	62	128
	4.7K ohm	30	59
	10 K ohm	26	53
	Pinched Base 40 K ohm	6	12
	100 K ohm	5	10
	N+Emitter 10 ohm	12	24
	Total Resistors	310	621
TOTAL COMPONENTS		431	847

THE LINEAR COMPONENTS

The POLY-USE A and G use the same family of NPN and PNP transistors, capacitors and resistors. These components are completely characterized in the linear component array Design Manual. A brief description of these components and their features follows.

NPN Transistors: There are five basic NPN transistor types on the arrays. QN1 is a standard NPN vertical structure designed for 10 mA nominal and 30 mA maximum collector current. QN2 is a higher frequency version NPN with two base contacts which reduce the series base resistance (rbb') to 150 ohm typ. QN3 is a low noise NPN that has a rbb' of only 70 ohm typ. The high current NPN, QN4 will handle 100 mA nominal and 300 mA maximum collector current. This transistor contains an extra deep collector diffusion which lowers the VCE(sat) to 250 mV at 100 mA. Finally, QN5 is a standard NPN transistor with an additional P diffusion in the collector which forms a merged PN junction capacitor (C2) off the collector. This is a convenient structure for use in designs requiring Miller capacitance.

PNP Transistors: The arrays have both lateral and substrate PNP transistors. QP6 is a standard lateral PNP designed to handle 1 mA nominal collector current. QP7 is a 5X multiple lateral PNP and QP8 is a 16X lateral PNP. These two PNP transistors contain multiple emitter-collector structures diffused into the same base for higher current handling capability. QP9 is a standard substrate PNP transistor that can handle 1 mA collector current. QP10 is a higher current substrate PNP designed for 5mA nominal collector current.

Diodes: The POLY-USE A also contains 3P+N+ zener diodes with a nominal voltage of 5.5 volts. Additionally, all NPN transistors can be used as zener diodes by connecting the emitter to the collector and using the emitter base junction breakdown for the zener voltage.

Resistors: Three types of resistor construction are used on the arrays; base, pinched-base and emitter. The resulting resistors are arranged in strings of 2 or 3 each in a wide range of standard discrete values. The majority of the resistors on the array are base diffused resistors of either 30 μm or 8 μm width with the values from 100 ohm to 10K ohm. For higher resistance, pinched-base resistors are available in 40K ohm and 100K ohm values. A maximum voltage of 5 volts can be applied to the pinched-base resistors. There are several low value emitter resistors on the arrays of 10 ohm each. Although the initial tolerance on these diffused resistors is not as close as with discrete components, the resistance matching of identical value resistors is superior to discrete versions.

Capacitors: The arrays contain both junction and MOS capacitors which may be used in ac coupling, Miller capacitance or compensation applications. The MOS capacitors are made with a layer of aluminum isolated from an N+ emitter diffusion by a thin layer of oxide. These capacitors have a nominal value of 8 pf which is voltage independent. They also exhibit very low series resistance (high Q). The junction capacitors C3 and C4 have voltage dependent capacitance and may be biased to several hundred picofarads. However, depending on the application, use of these junction capacitors may be limited due to non-negligible leakage currents. The P+N+ junction capacitor (C4) merged with a standard NPN transistor (QN5) provides Miller capacitance capability.

TABLE II — Typical Electrical Characteristics (T_{amb} = + 25°C)

Transistors	NPN (QN1, 2, 3, 4, 5)	Lateral PNP (QP6, 7, 8)	Substrate PNP (QP9, 10)
BVcbo	45 V	45 V	45 V
BVceo	20 V	40 V	45 V
BVebo	6.1 V	30 V	25 V
h_{FE}	140	35	60
f_T	550 MHz	3.5 MHz	14 MHz

Capacitors	MOS (C1)	Junction (C2)	Junction (C3)	Junction (C4)
Nominal value	8 pf	$\frac{5\text{ pf}}{(1 + Vc/0.5)^{0.4}}$	$\frac{30\text{ pf}}{(1 + Vc/0.75)^{0.33}}$	$\frac{100\text{ pf}}{(1 + Vc/0.75)^{0.33}}$
Max. Voltage	±20 V	20 V	2.0 V	2.0 V

Resistors	Base	Pinched Base	Emitter
Initial tolerance	±30%	+100% – 50%	+40% – 30%
Matching (Same value pairs)	±2%	±5%	±10%
Temperature coefficient (typ.)	+0.1%/°C	+0.5%/°C	+0.15%/°C

KIT PARTS

Successful linear component array design may require a bread board analysis of the custom circuit prior to committing to layout. A complete set of array components is available in kit part form for this purpose. In addition to kit parts for the various transistors and capacitors on the POLY USE A and G there are also several "linear functions" which have been built and characterized using the array components including a wide band differential amplifier, an active load differential amplifier, a 1.3 volt band gap reference voltage source, a temperature dependent current source and an NPN mixer configuration. All kit parts are packaged in standard 16 pin ceramic DIPs.

TABLE III — Available Breadboard Kit Parts

Kit Part #	Description
KP01	5 standard NPN transistor array (QN1)
KP02	4 standard lateral PNPs (QP6) 1 substrate PNP (QP9)
KP06	1 standard NPN (QN1) 1 standard PNP (PQ6) 1 high current NPN (QN4) 1 high current lateral PNP, 16x (QP8) 1 high current substrate PNP (QP10)
KP054	2 mixer configurations of standard NPNs (QN1)
KP121A	2 low noise NPNs (QN3) 1 wide band differential amplifier circuit
KP122	5 high frequency NPN transistor array (QN2)
KP124A	1 high current lateral PNP (QP8) 1 MOS capacitor (C1) 1 P+N+ capacitor (C4) 1 active load differential amplifier circuit
KP128A	1 P+N+ capacitor (C3) 1 temperature dependent current source circuit 1 wide band differential amplifier circuit 1 band gap 1.3 V voltage source

CIRCUIT MODELING AND SIMULATION

Instead of, or in addition to, bread board evaluation, the customer may want to perform computer analysis of the circuit to verify correct operation over a range of environmental and process variations. To assist with this analysis, a complete set of modeling parameters is available in the linear component array Design Manual for each component type on the POLY-USE A and G. The parameters are given for Ebers-Moll and Gummel-Poon bipolar transistor models which are used in simulation programs such as SPICE.

LAYOUT TECHNIQUES

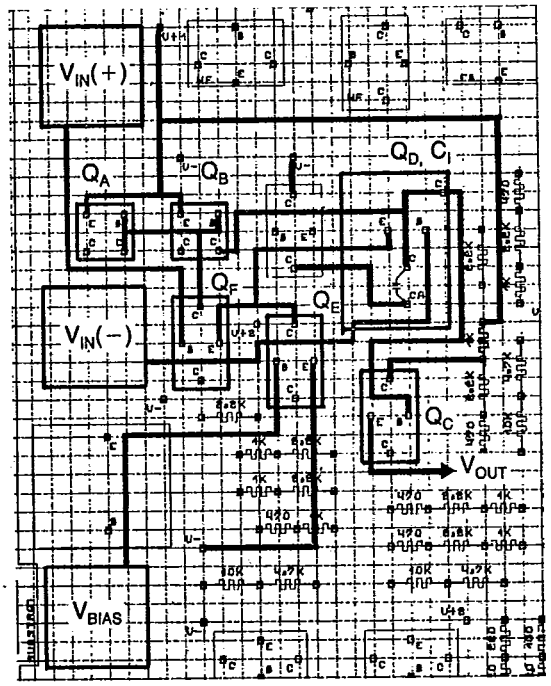
The linear component arrays may be routed manually by the customer on routing sheets provided by THOMSON SEMICONDUCTORS. The POLY-USE A and G arrays have been designed to be much easier for the customer to manually interconnect and route than competing single level metal linear arrays. All of the customization of each array is done on second metal. The first level metal pattern is standard on each array, and it provides low resistance distribution of the power and ground buses throughout the array. The POLY-USE G has two separate power buses (+5, +12 volts, for example) and one ground bus. This simplifies the required interconnection on second metal as all supply routing is already provided on first metal. Contact to any of the power supply buses is made by simply routing the interconnect to one of the many V− and V+ contact vias (V−, V+1, V+2 on the POLY-USE G located throughout the array.

Another feature that simplifies the manual layout is the grid on which all interconnect metal is placed. The grid pitch is 31 μm and by specifying the routing along the grid, proper metal spacing and metal width, (16 μm line width is standard), are automatically maintained. Where higher current handling is required (>40 mA) the line width may be drawn wider to indicate the necessary metal width.

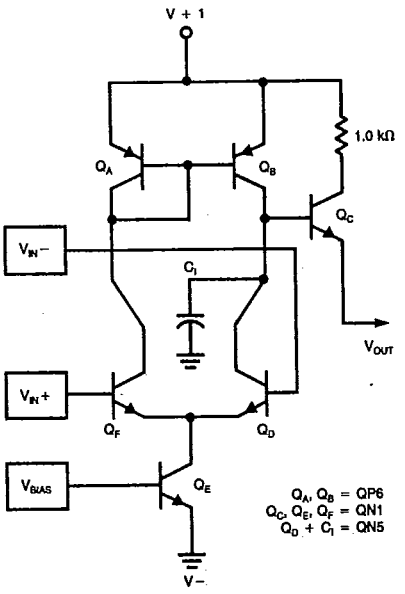
All contact vias to the individual component terminals as well as all power and ground contacts are

located on intersection points on the grid, further simplifying routing. All NPN transistors have two collector contacts which can be used as crossunder connections. There are also contacts to a number of first level metal crossunders throughout the array which are strategically located so as to simplify connections from the center of the array to the bonding pads on the periphery of the chip. These features reduce the average manual layout time by a factor of 3 over similar complexity single level metal arrays. A high percentage of component utilization is also possible on the POLY-USE A and G, typically 80 to 90 percent, and better electrical characteristics should be expected.

LAYOUT EXAMPLE: Differential Amplifier Circuit on the POLY-USE G



Completed Manual Layout on Routing Sheet



Circuit Schematic

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The layout example demonstrates some of the "user-friendly" features of the VSI routing sheets:

- Conveniently located supply and ground contacts (V + 1 and V−) simplify bias connections.
- Collector contacts of the unused NPN transistor form a handy crossunder connection.
- Both C_I and Q_D of the circuit schematic are implemented with the QN5, merged capacitor transistor.

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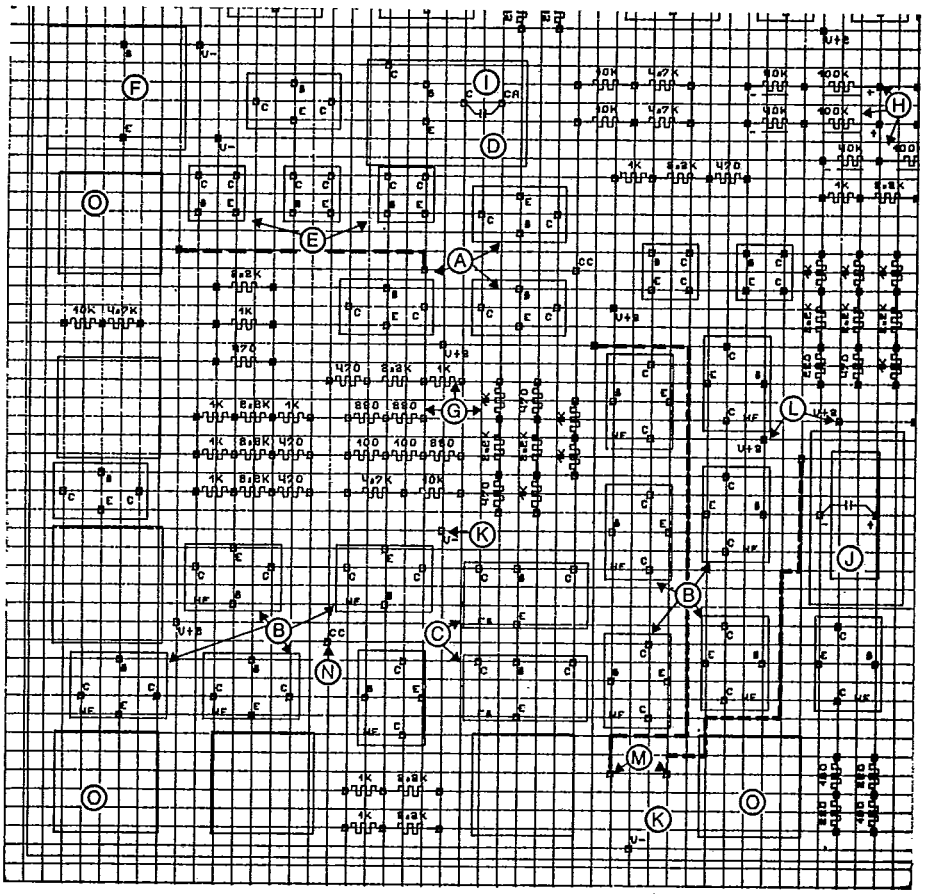
POLY-USE G ROUTING SHEET DETAIL



LEGEND

TRANSISTORS

- Ⓐ — Standard NPN — QN1
- Ⓑ — High Frequency NPN — QN2
- Ⓒ — Low Noise NPN — QN3
- Ⓓ — Standard NPN with Merged PN Junction Capacitor — QN5
- Ⓔ — Standard Lateral PNP — QP6
- Ⓕ — High Current Substrate PNP — QP10

RESISTORS

- Ⓖ — Base Resistor Strings
- Ⓗ — Pinched-base Resistor Strings

CAPACITORS

- Ⓘ — PN Junction Merged with QN5 — C2
- Ⓙ — P^+N^+ Isolated Junction — C3

OTHER CONTACTS

- Ⓚ — Negative Supply Voltage or Ground Contacts
- Ⓛ — Positive Supply Voltage Contacts
- Ⓜ — First Level Metal Crossunder Connections
- Ⓝ — Resistor Tub Biasing Contact
- Ⓞ — Bonding Pad Location.

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DESIGN MANUAL

The starting point in developing a custom linear circuit on the POLY-USE A and G is a review of the LINEAR COMPONENT ARRAY DESIGN MANUAL. The Manual contains all the information necessary for a customer to design and layout a custom linear circuit on the POLY-USE A and G arrays including:

- Description of the bipolar processing technology used
- Description of the basic linear component structures and their topology
- Electrical characteristics of the components
- Modeling parameters of the components for computer simulation
- Data sheets for the breadboard Kit Parts
- Explanation of layout and routing procedures
- Manual routing sheets for both the POLY-USE A and G

DESIGN DEVELOPMENT PROCEDURE

The development of a custom linear circuit is a joint effort involving THOMSON SEMICONDUCTORS and the customer. Typical development work is divided as follows:

The CUSTOMER Tasks:

- Review the Design Manual
- Generate a circuit schematic using POLY-USE A and G components
- Perform breadboard evaluation and/or computer simulation of the circuit
- Layout circuit on routing sheet
- Submit complete Design Package including: completed routing sheet, circuit schematic, breadboard schematic (if applicable), description of circuit operation, application, circuit performance and test specifications

THOMSON SEMICONDUCTORS Tasks:

- Review the Design Package
- Convert the completed routing sheet to custom metalization mask
- Process wafers and probe to basic process test patterns
- Assemble die into packages
- Test functional prototypes and ship to customer

THOMSON SEMICONDUCTORS will normally ship the prototypes within 6 to 10 weeks after receiving the customer's Design Package. The testing of the prototypes will be sufficient to ensure proper circuit functionality. After the customer completes evaluation and characterization of the prototypes, THOMSON SEMICONDUCTORS will work closely with the customer to finalize the test programs and procedures for use in volume production.

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