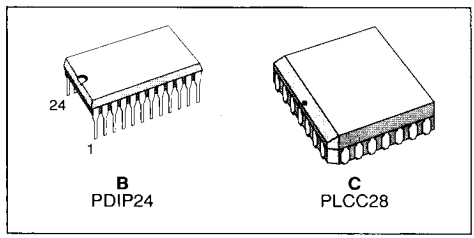
E²PROM CMOS PROGRAMMABLE LOGIC DEVICE

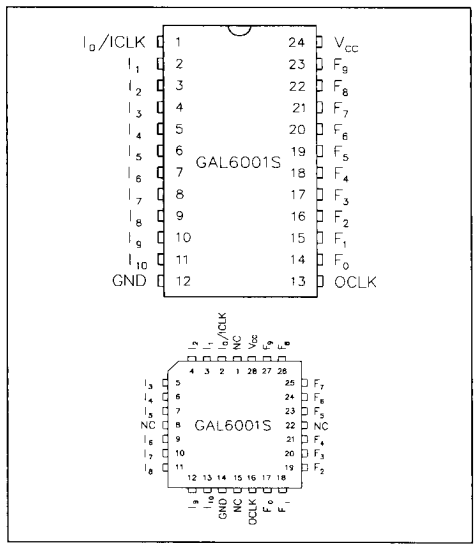
- ELECTRICALLY ERASABLE CELL TECHNOLOGY
  - Instantly reconfigurable logic
  - Instantly reprogrammable cells
  - Guaranteed 100% yields
- HIGH PERFORMANCE E²CMOS TECHNOLOGY
  - Low power: 90mA typical
  - High speed: 12ns max. clock to output delay, 25ns max. setup time, 30ns max. propagation delay
- TTL COMPATIBLE INPUTS AND OUTPUTS
- UNPRECEDENTED FUNCTIONAL DENSITY
  - 10 Output Logic Macrocells
  - 8 Buried Logic Macrocells
  - 20 Input and I/O Logic Macrocells
- HIGH-LEVEL DESIGN FLEXIBILITY
  - 78 × 64 × 36 FPLA Architecture
  - Separate buried register and input clock pins
  - Functionally supersets existing 24 pin PAL® and IFL™ devices
  - Asynchronous or Synchronous clocking
- SPACE SAVING 24 PINS, 300 MILS DIP
- HIGH SPEED PROGRAMMING ALGORITHM
- 20 YEAR DATA RETENTION



B
PDIP24

C
PLCC28

Pin Connections



Pin Names

I_0–I_{10}	Input
F_0–F_9	I/O
ICLK	Input Clock
OCLK	Output Clock
V_{CC}	Power
GND	Ground

DESCRIPTION

Using a high performance E²CMOS technology, SGS-THOMSON has produced a next-generation programmable logic device, the GAL6001S. Using FPLA architecture known for its superior flexibility in state machine design, the GAL6001S offers the highest degree of functional integration and flexibility currently available in a 24 pin, 300 mils package.

The GAL6001S has 10 programmable Output Logic Macrocells (OLMCs) and 8 programmable Buried Logic Macrocells (BLMCs). In addition, there are 10 Input Logic Macrocells (ILMCs) and 10 I/O Logic Macrocells (IOLMC). Two Clock inputs are provided for independent control of the Input and Output Macrocells.
Advanced features that simplify programming and reduce test time, coupled with E²PROM CMOS reprogrammable cells, enable complete AC, DC, programmability, and functionality test of each GAL6001S during manufacture. This allows SGS-THOMSON to guarantee 100% field programmability and functionality to datasheet specifications.

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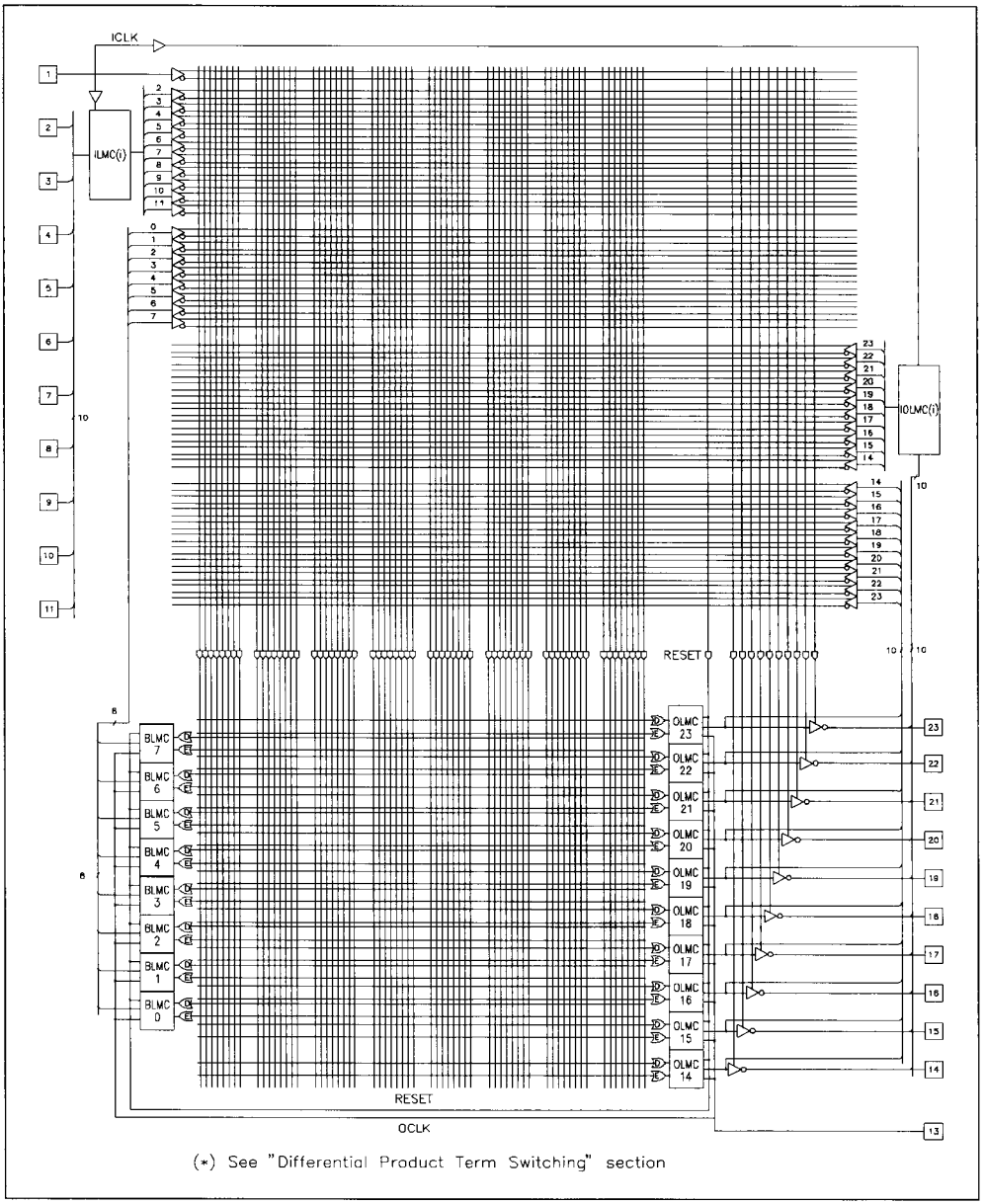
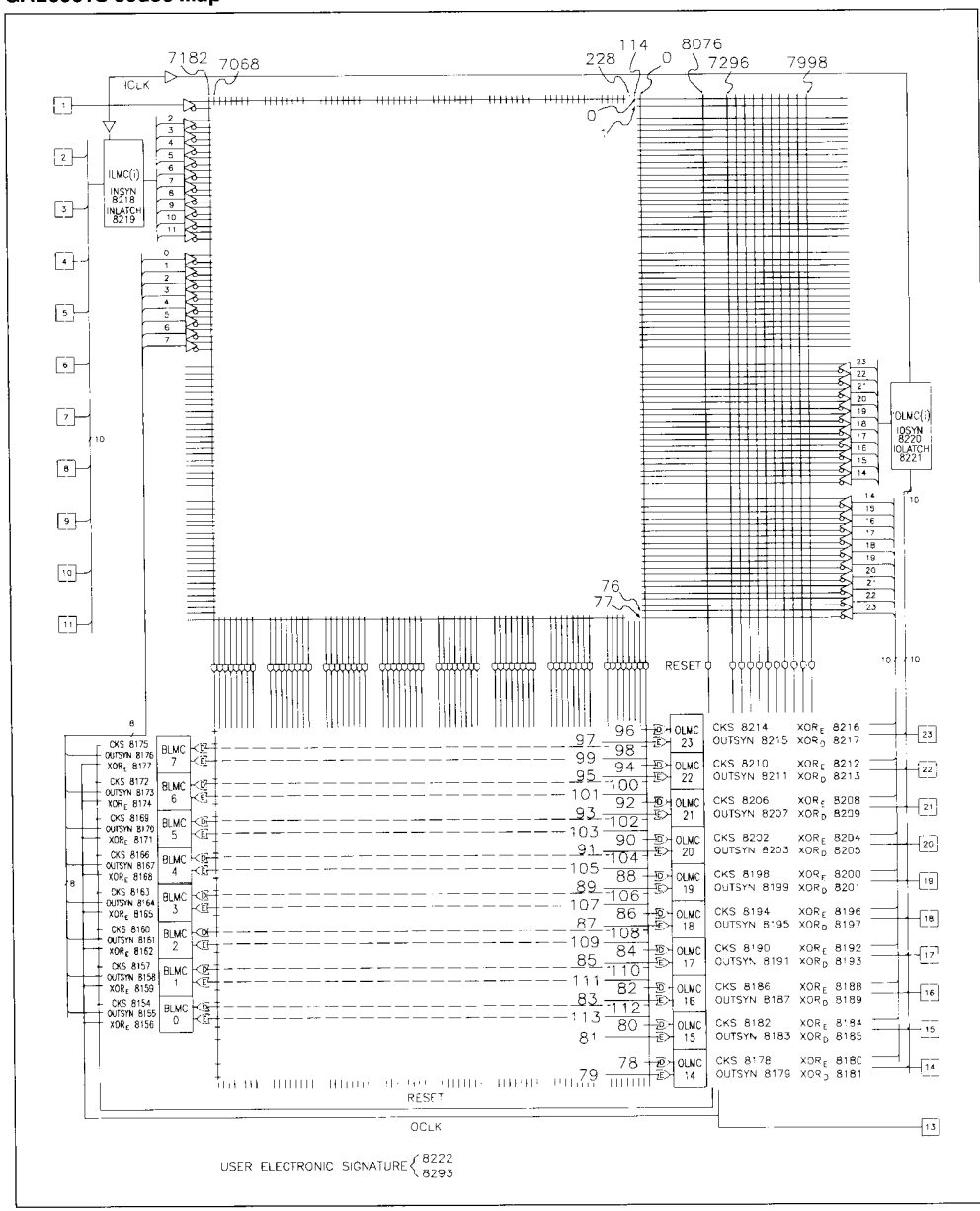
GAL6001S Logic Diagram

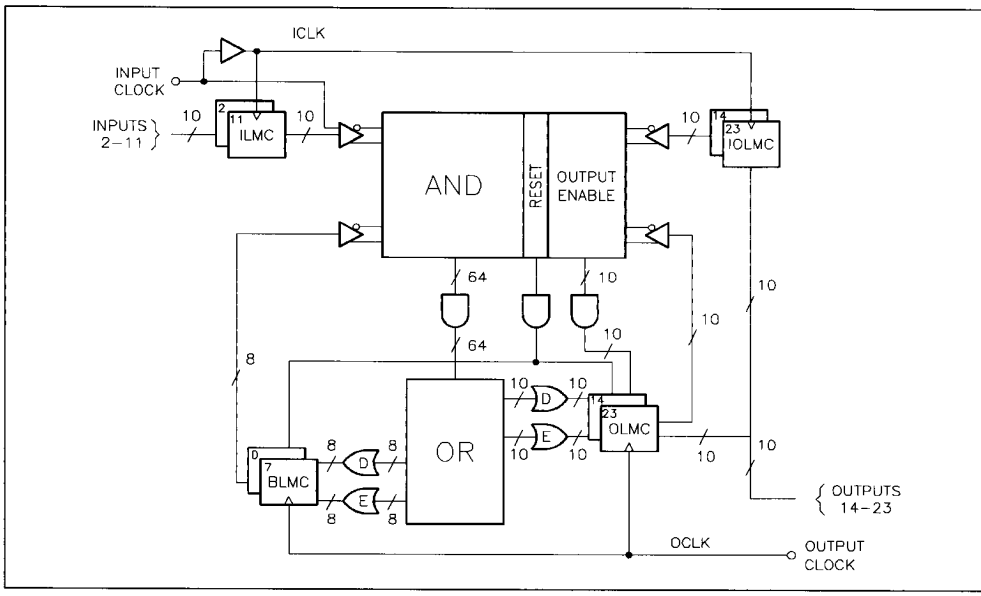


GAL6001S Jedec Map



Programming is accomplished using standard hardware and software tools. SGS-THOMSON guarantees a minimum of 100 erase write cycles, and data retention to exceed 20 years. An Electronic Signature word has been provided for user-defined data. In addition, a security cell is available to protect proprietary designs.

GAL6001S Functional Block Diagram



Macrocells Names

ILMC	Input Logic Macrocell
IOLMC	I/O Logic Macrocell
BLMC	Buried Logic Macrocell
OLMC	Output Logic Macrocell

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	Input Voltage Applied	-2.5 to V_{CC}+1	V
V_B	Off-State Output (Bidirectional) Voltage Applied	-2.5 to V_{CC}+1	V
T_{STG}	Storage Temperature	-65 to +125	°C
T_J	Junction Temperature (Operating)	-40 to +125	°C
T_L	Lead Temperature (Soldering)	260 (for 10s max.)	°C

Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.

Switching Test Conditions

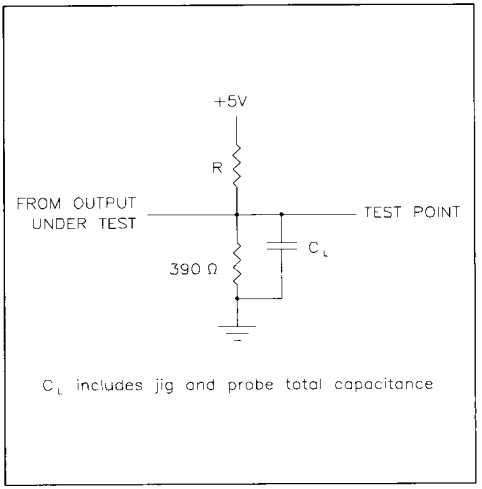
Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10%-90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See figure

3-state levels are measured 0.5V from steady-state active level.

Test Conditions

#	R [Ω]	C_L [pF]
1	300	50
2	Active High: ∞ Active Low: 300	50
3	Active High: ∞ Active Low: 300	5

Switching Test Circuit



Capacitance (T_A=25°C, f=1.0MHz, V_{CC}=5V)

Symbol	Parameter	Test Conditions	Maximum*	Units
C_I	Input Capacitance	V_I=2V	8	pF
C_B	Bidirectional Pin Capacitance	V_B=2V	10	pF

* Guarantied but not 100% tested.

DC Operating Conditions

Symbol	Parameter	Commercial Temperature Range		Industrial Temperature Range		Units
		Min.	Max.	Min.	Max.	
V_{CC}	Supply Voltage	4.75	5.25	4.5	5.5	V
T_A	Ambient Temperature	0	70	-40	85	°C
V_{IL}	Input Low Voltage	V_{SS}*-0.5	0.8	V_{SS}*-0.5	0.8	V
V_{IH}	Input High Voltage	2.0	V_{CC}+1	2.0	V_{CC}+1	V
I_{OL}	Low Level Output Current	–	16	–	16	mA
I_{OH}	High Level Output Current	-3.2	–	-3.2	–	mA

* V_{SS} is the voltage applied to the GND pin.

Electrical Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions	Commercial Temperature Range		Industrial Temperature Range		Units
			Min.	Max.	Min.	Max.	
I_{IH}, I_{IL}	Input Leakage Current	$GND \le V_I \le V_{CC\ Max}$	–	±10	–	±10	µA
I_{BH}, I_{BL}	Bidirectional Pin Leakage Current	$GND \le V_I \le V_{CC\ Max}$	–	±10	–	±10	µA
I_{CC}	Operating Power Supply Current	f=15MHz V_{IL}=0.5V V_{IH}=3.0V	–	150	–	180	mA
I_{OS}*	Output Short Circuit Current	V_{CC}=5.0V, V_B=0.5V	-130	-30	-130	-30	mA
V_{OL}	Output Low Voltage	–	–	0.5	–	0.5	V
V_{OH}	Output High Voltage	–	2.4	–	2.4	–	V

* One output at a time for a maximum duration of one second.

Switching Characteristics Over Operating Conditions

Symbol	Parameter	From	To	6001S-30	6001S-35	Units	Test Cond.♦
				Max.☆	Max.✲		
t_{pda}	Combinational Propagation Delay (ILMC Async.)	Input	Output	30	35	ns	1
t_{pdf}	Combinational Propagation Delay (With Feedback)	Output, Registered Output	Output	30	35	ns	1
t_{pdl}	Combinational Propagation Delay (ILMC Latch)	Input	Output	35	40	ns	1
t_{coir}	Input Clock to Output Delay (ILMC Reg., OLMC Comb.)	ICLK	Output	35	40	ns	1
t_{coil}	Input Clock to Output Delay (ILMC Latch, OLMC Comb.)	ICLK	Output	35	40	ns	1
t_{coo}	Output Clock to Registered Output Delay (OLMC D/E Reg.)	OCLK	Registered Output	12	13.5	ns	1
t_{cos}	Sum Term Clock to Registered Output Delay (OLMC D Reg.)	STCLK	Registered Output	35	40	ns	1
t_{en}	Product Term Output Enable to Output Delay	Input, I/O	Output, Registered Output	25	30	ns	2
t_{dis}	Product Term Output Disable to Output Delay	Input, I/O	Output, Registered Output	25	30	ns	3
t_{res}	Register Reset Delay	Input, I/O	Registered Output	35	35	ns	1

♦ Refer to Switching Test Conditions".

☆ Commercial Temperature range only.

✲ Industrial Temperature range only.

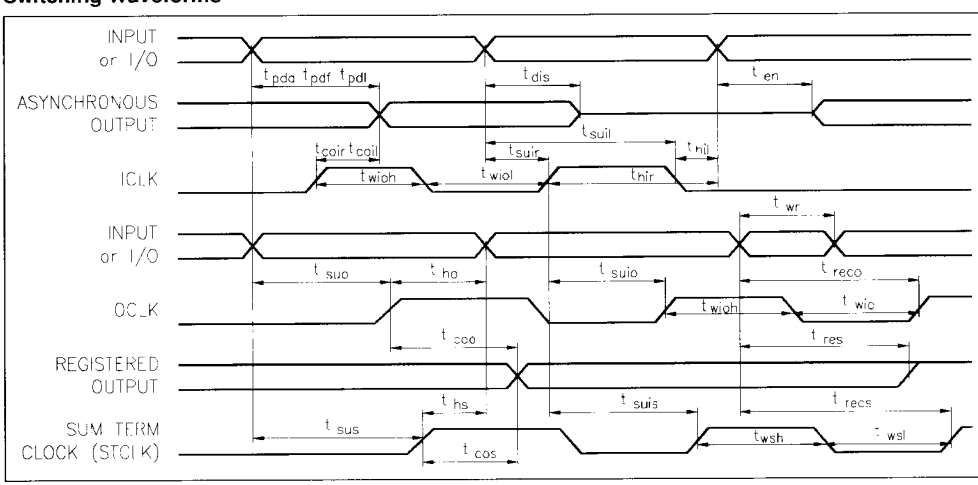
AC Operating Conditions

Symbol	Parameter	6001S-30*		6001S-35+		Units
		Min.	Max.	Min.	Max.	
t_{suil}	Input Setup Time Before ICLK Fall (ILMC Latch)	–	2.5	–	3.5	ns
t_{suir}	Input Setup Time Before ICLK Rise (ILMC Reg.)	–	2.5	–	3.5	ns
t_{suo}	Input or Feedback Setup Time Before OCLK Rise (OLMC D/E Reg.)	–	25	–	30	ns
t_{sus}	Input or Feedback Setup Time Before STCLK Rise (OLMC D Reg.)	–	7.5	–	10	ns
t_{suio}	ICLK Rise Setup Time Before OCLK Rise (OLMC D/E Reg.)	–	30	–	35	ns
t_{suis}	ICLK Rise Setup Time Before STCLK Rise (OLMC D Reg.)	–	15	–	17	ns
t_{hil}	Hold Time After ICLK Fall (ILMC Latch)	–	5	–	5	ns
t_{hir}	Hold Time After ICLK Rise (ILMC Reg.)	–	5	–	5	ns
t_{ho}	Hold Time After OCLK Rise (OLMC D/E Reg.)	–	5	–	5	ns
t_{hs}	Hold Time After STCLK Rise (OLMC D Reg.)	–	10	–	12.5	ns
t_{wioh}	ICLK or OCLK Pulse Duration High	–	10	–	10	ns
t_{wiol}	ICLK or OCLK Pulse Duration Low	–	10	–	10	ns
t_{wsh}	STCLK Pulse Duration High	–	15	–	15	ns
t_{wsl}	STCLK Pulse Duration Low	–	15	–	15	ns
t_{wr}	Reset Pulse Duration	–	15	–	15	ns
t_{reco}	Reset to OCLK Recovery Time	–	20	–	20	ns
t_{recs}	Reset to STCLK Recovery Time	–	10	–	10	ns
f_{clk}	OCLK or STCLK Maximum Frequency	27	–	22.9	–	MHz

* Commercial Temperature range only.

+ Industrial Temperature range only.

Switching Waveforms



INPUT LOGIC MACROCELL (ILMC) AND I/O LOGIC MACROCELL (IOLMC)

The GAL6001S features two configurable input sections.

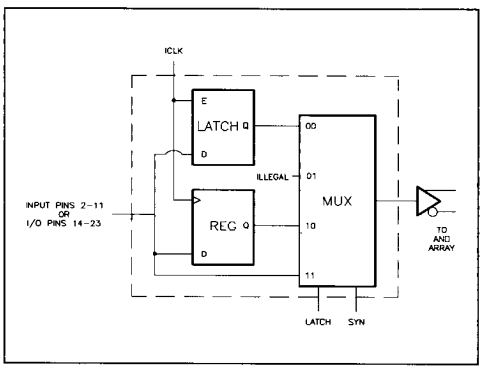
The ILMC section corresponds to the dedicated input pins (2-11) and the IOLMC section to the I/O pins (14-23). Each input section is configurable as a block for asynchronous, latched, or registered inputs. Pin 1 (ICLK) is used as an enable input for latched macrocells (transparent when high) and as a clock for registered macrocells (positive edge triggered).

Configurable input blocks can be used to advantage by system designers. Registered inputs are popular for synchronization and data merging. Transparent latches are useful when the input data is invalid outside a known time window. Direct inputs are used in systems where the input data is well ordered in time. With the GAL6001S, external registers and latches are not necessary.

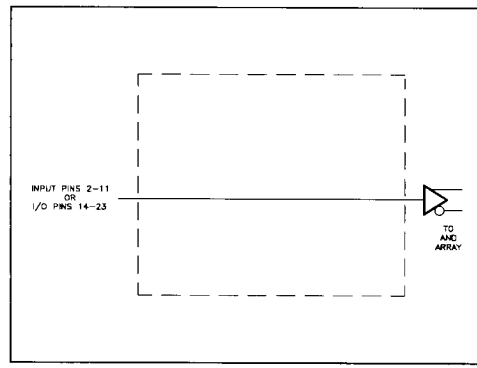
The various configurations of the Input and I/O Macrocells are controlled by programming four architecture control bits (LATCH and SYN both for Input and I/O Macrocells) within the 68 bits Architecture Control Word. The SYN bits determine whether the macrocells will have register/latch capability or will be strictly asynchronous. The LATCH bits select between latched and registered inputs.

The three valid macrocell configurations are shown in the macrocell equivalent diagrams shown below.

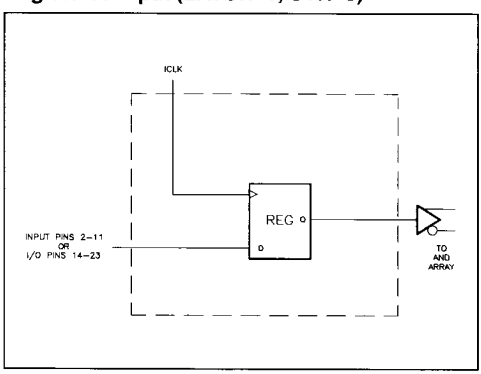
ILMC/IOLMC Generic Block Diagram



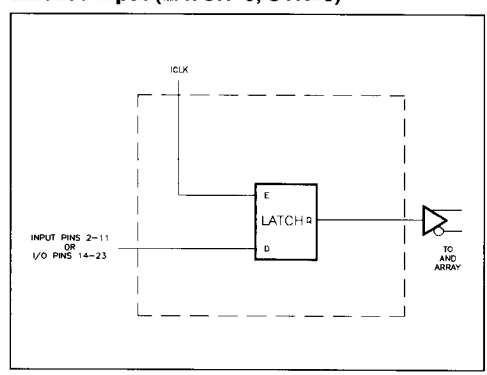
Asynchronous Input (LATCH=1, SYN=1)



Registered Input (LATCH=1, SYN=0)



Latched Input (LATCH=0, SYN=0)



OUTPUT LOGIC MACROCELL (OLMC) AND BURIED LOGIC MACROCELL (BLMC)

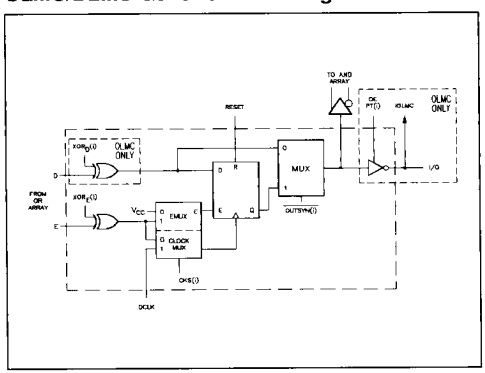
The outputs of the OR array feed two groups of macrocells. One group of eight macrocells is buried; its output feed back directly into the AND array rather than to device pins. These cells are called the Buried Logic Macrocells (BLMC): they are useful for building state machines. The second group of macrocells consists of 10 cells whose outputs, in addition to feeding back into the AND array, are available at the device pins. Cells in this group are known as Output Logic Macrocells (OLMC).

Like the ILMCs and IOLMCs discussed above, Output and Buried Logic Macrocells are configured by programming specific bits in the Architecture Control Word (CKS(i), OUTSYN(i), $XOR_D(i)$, $XOR_E(i)$), but unlike the Input Macrocells which must be configured in blocks, these macrocells are configurable on a macrocell-by-macrocell basis. Throughout this data sheet, i=[14..23] for OLMCs and i=[0...7] for BLMCs.

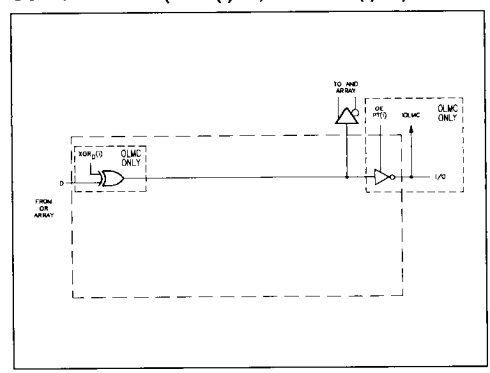
Buried and Output Logic Macrocells may be set to one of three valid configurations: combinational, D type registered with sum term (asynchronous) clock or D/E type registered.

Output macrocells always have I/O capability, with directional control provided by the 10 output enable (OE) product terms. Additionally, the polarity of each OLMC output is selectable through the $XOR_D(i)$ architecture bits. Polarity selection is available for BLMCs, since both the true and complemented forms of their outputs are available in the AND array.

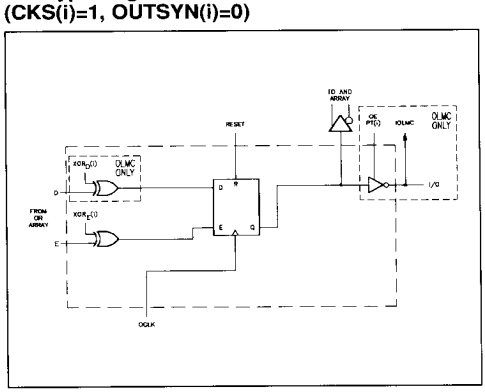
OLMC/BLMC Generic Block Diagram

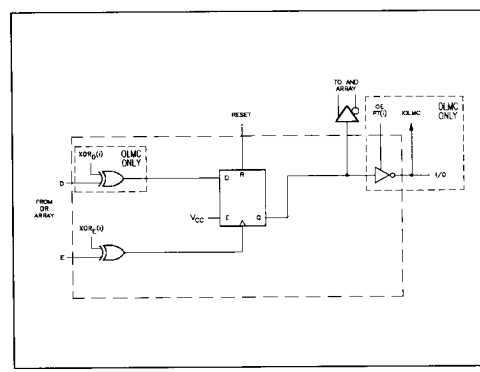


Combinational (CKS(i)=0, OUTSYN(i)=1)



D/E Type Registered (CKS(i)=1, OUTSYN(i)=0)





Polarity of all "E" sum terms is selectable through the $XOR_E(i)$ architecture control bits.
When CKS(i) = 1 and OUTSYN(i) = 0, macrocell "i" is set as "D/E type registered". In this configuration, the register is clocked from the common OCLK and the register clock enable input is controlled by the associated "E" sum term. This configuration is useful for building counters and state-machines with state hold functions.
When the macrocell is configured as a "D type registered with a sum term asynchronous clock" (CKS(i) = 0 and OUTSYN(i) = 0), the register is always enabled and its "E" sum term is routed directly to the clock input. This permits asynchronous programmable clocking, selected on a register-by-register basis.
When CKS(i) = 0 and OUTSYN(i) = 1, macrocell "i" is set as "combinational". Configuring a BLMC in this manner turns it into a complement array. Complement arrays are used to construct multi-level logic.
Registers in both the Output and Buried Logic Macrocells feature a common RESET product term. This active high product term allows the registers to be asynchronously reset. Registers are reset to a logic zero. If connected to an output pin, a logic one will occur because of the inverting output buffer.
There are two possible feedback paths from each OLMC: one directly from the OLMC (this feedback is before the output buffer and always present), and one from OLMC after the output buffer through the IOLMC. The second path is usable as a feedback only when the associated bidirectional pin is being used as an output. With this dual feedback arrangement, the OLMC can be permanently buried (the associate OLMC pin is an input), or dynamically buried with the use of the output enable product term.
The D/E registers used in this device offer the designer the ultimate in flexibility and utility. The D/E register architecture can emulate RS, JK, and T type registers with the same efficiency as a dedicated RS, JK, or T register.
The three valid macrocell configurations are shown in the macrocell equivalent diagrams shown in the previous page.

ARRAY DESCRIPTION

The GAL6001S E^2 reprogrammable array is subdivided into two smaller arrays; the first is an AND and the second is an OR array. These arrays are described in detail below.

AND ARRAY

The AND array is organized as 78 input terms by 75 product term outputs. The 10 ILMC, 10 I/O Logic Macrocells, 8 BLMC feedbacks, 10 OLMC feedbacks, and ICLK comprise the 39 inputs to this array (each available in true and complemented forms). Product terms 0-63 serve as inputs to the OR array. Product term 64 is the RESET PT; it generates the RESET signal described in the earlier discussion of Output and Buried Logic Macrocells. Product terms 65-74 are the output enable product terms; they control the output buffers, thus enabling device pins 14-23 to be bidirectional or 3-state.

OR ARRAY

The OR array is organized as 64 inputs by 36 sum term outputs. 64 product terms from the AND array serve as the inputs to the OR array. Of the 36 sum term outputs, 18 are data ("D") terms and 18 are enable/clock ("E") terms. These terms feed into the 10 OLMCs and 8 BLMCs, one "D" term and one "E" term to each.
The programmable OR array offers unparalleled versatility in product term usage. This programmability allows from 1 to 64 product terms to be connected to a single sum term. A programmable OR array is more flexible than a fixed, shared, or variable product term architecture.

ARCHITECTURE CONTROL WORD

The various configurations of the GAL6001S are enabled by programming cells within the Architecture Control Word. This 68 bits word contains all of the chip configuration data. This data includes: $XOR_D(i)$, $XOR_E(i)$, CKS(i), OUTSYN(i), and LATCH and SYN bits both for ILMCs and IOLMCs. The function of each of these bits has been previously explained.

USER ELECTRONIC SIGNATURE WORD

An User Electronic Signature word (UES) is provided with GAL6001S device. The User Electronic Signature word is a 72 bits user definable storage area, which can be used to save inventory control data, pattern revision numbers, manufacture date, etc. Signature data is always available to the user, regardless of the state of the security cell.
Note: UES is included in checksum calculations. Changing the UES will alter the checksum.

SECURITY CELL

A security cell is provided with GAL6001S device as a deterrent to unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the AND and OR arrays. This cell can be erased only during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. User Electronic Signature data is always available to the user, regardless of the state of this control cell.

BULK ERASE

Before writing a new pattern into a previously programmed part, the old pattern must first be erased. This erasure is done automatically by the programming hardware as part of the programming cycle and takes only 50 milliseconds.

REGISTERED PRELOAD

When testing state machine designs, all possible states and state transitions must be verified, not just those required during normal operations. This verification is necessary because in system operation

certain events may occur that cause the logic to assume an illegal state: power-up, brown out, line voltage glitches, etc. To test a design for proper management of these conditions, a method must be provided to break the feedback paths and force any desired state (e.g. an illegal state) into the registers. Then the machine can be sequenced and the outputs tested for correct next state generation. All registers in the GAL6001S can be preloaded, including the ILMC, IOLMC, OLMC, and BLMC registers. The programming hardware takes care or all preload timing and voltage requirements.

INPUT BUFFERS

GAL devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, load driving logic much less than traditional bipolar devices.
This allows for a greater fan out from the driving logic.
GAL6001S does not include active pull-ups within its input structures. As a result, SGS-THOMSON recommends that all unused inputs and 3-state I/O pins be connected to another active input, V_{CC}, or GND. This precaution improves the noise immunity and reduces the I_{CC} consumption.

POWER-UP RESET

Circuitry within the GAL6001S provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{reset}=10µs). As a result, the state on the registered output pins (if they are enabled) will always be high after power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state upon power-up.
The timing diagram for power-up is shown below. Because of the asynchronous nature of system power-up, the V_{CC} rise must be monotonic to guarantee a valid power-up reset of the GAL6001S. The registers will reset within a maximum of t_{reset} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have elapsed (i.e. avoid clocking before the t_{pr}=t_{reset}+t_{su} time interval).

DIFFERENTIAL PRODUCT TERM SWITCHING (DPTS)

The number of "Differential Product Term Switching" (DPTS) for a given design is calculated by taking the absolute value of:

- the total number of product terms that are switching from a logical level high to a logical level low
- minus the total number of those switching from a logical level low to a logical level high

within a 5ns time window.

$$DPTS = | PT_{LH} - PT_{HL} |$$

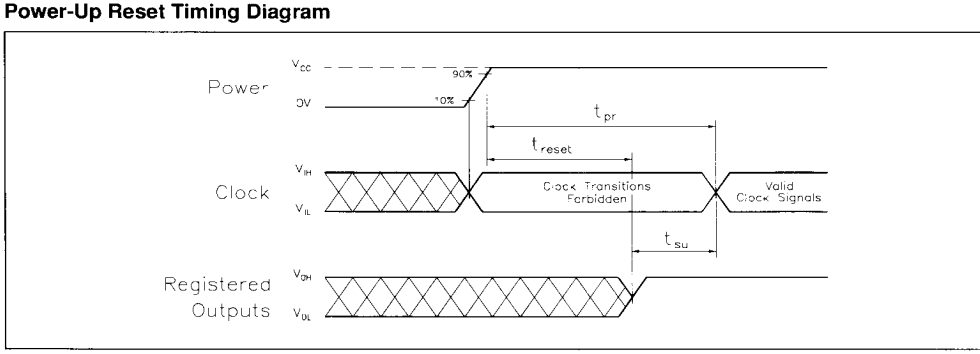
The correct behaviour of the device is guaranteed for applications where the number of DPTS is not greater than 15. This limit is believed to be largely conservative. For the device to exhibit an incorrect behaviour, other conditions of supply voltage, clock timing, temperature, etc., should be simultaneously present. As each of these conditions may, to some extent, lay partly within the operating range limits, it is simpler to refer to a DPTS boundary that ensures ample margin in all conditions for a correct operation.

There is no limit on the number of product terms that can be used at the same time.

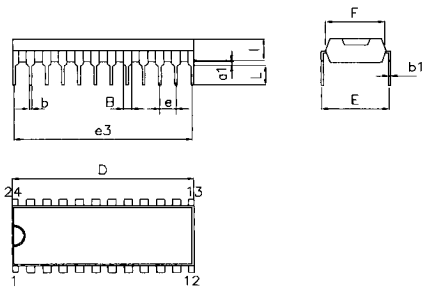
LATCH-UP PROTECTION

GAL6001S devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent external disturbances from causing the circuitry to latch. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups to eliminate any possibility of SCR induced latching.

Power-Up Reset Timing Diagram

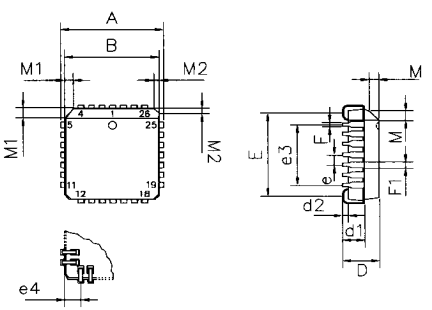


PDIP 24 Pins



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
a1	0.38			0.015		
B	1.27		1.65	0.050		0.065
b		0.46			0.018	
b1		0.25			0.010	
D			31.88			1.255
E		7.62			0.300	
e		2.54			0.100	
e3		27.94			1.100	
F			6.86			0.27
I			4.32			0.170
L		3.30			0.130	

PLCC 28 Pins



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	12.32		12.57	0.485		0.495
B	11.43		11.58	0.450		0.456
D	4.20		4.57	0.165		0.180
d1	2.29		3.04	0.090		0.120
d2	0.51			0.020		
E	9.91		10.92	0.390		0.430
e		1.27			0.050	
e3		7.62			0.300	
e4			1.99			0.078
F		0.46			0.018	
F1		0.71			0.028	
M		1.24			0.049	
M1		1.143			0.045	
M2			0.51			0.020

Seating Plane: 0.101 mm/0.004 inches

Ordering Informations*

SGS-THOMSON GAL®s are available in a variety of package and temperature ranges.
General ordering code is reported below.

GAL6001S - s w p t

Temperature	**1**	0°C to +70°C (only for 30ns Speed selection)
	3	- 40°C to +85°C (only for 35ns Speed selection)
Package	**B**	24 Pins PDIP
	C	28 Pins PLCC
Power	**H**	Half Power
Speed	**30**	30ns (Commercial Temperature range only)
	35	35ns (Industrial Temperature range only)

Example: ordering code for a GAL6001S, 30ns speed and Half Power in PDIP is **GAL6001S-30HB1**

* Please contact local Product Marketing for latest update on package / temperature range availability.