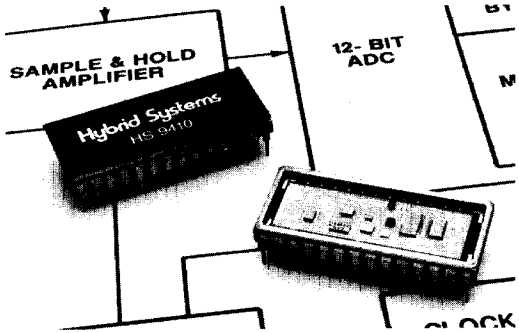
8 CHANNEL, 12-BIT DATA ACQUISITION SYSTEM WITH μP INTERFACE

FEATURES

- Complete 8 channel, 12-bit data acquisition system with MUX, S/H, REF, clock and three-state outputs
- Full 8- or 16-bit microprocessor bus interface
- Guaranteed linearity over temperature
- High throughput rate: 25kHz
- Hermetic 28-pin ceramic or low cost epoxy DIP
- Low Power: 400mW



DESCRIPTION

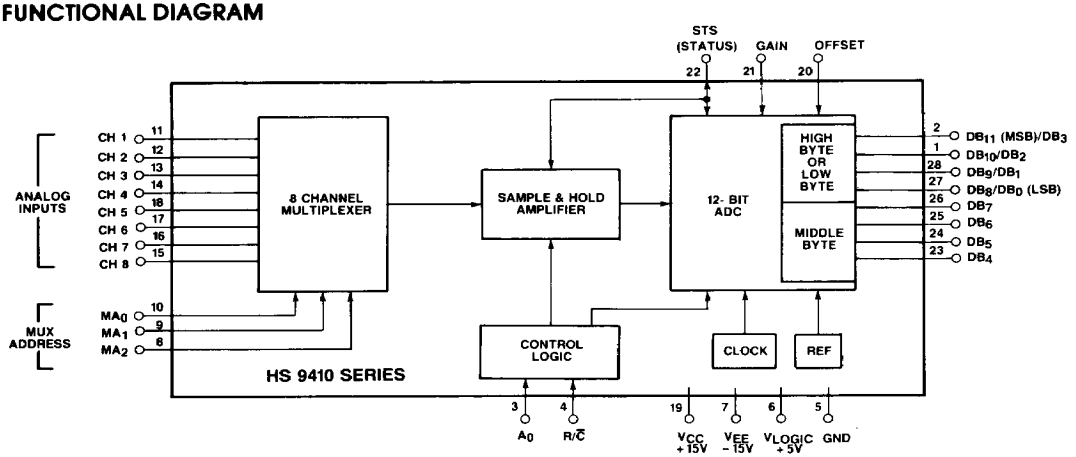
The HS9410 Series is a complete 8 channel, microprocessor compatible, 12-bit data acquisition system with all the interface logic to connect directly to 8- or 16-bit microprocessor buses. It is contained in a 28-pin DIP and includes an 8 channel multiplexer, a sample-and-hold amplifier, and a 12-bit A/D converter along with the control logic needed to perform a complete data acquisition function. System throughput rate is 25kHz for full rated accuracy.

The analog-to-digital converter section contains the HS574 12-bit ADC. The HS9410 Series is offered in a hermetically-sealed package for use over a wide temperature range and for MIL-STD-883 requirements.

The HS9410 Series operates from ±15V* and +5V with a total power consumption of 400mW. To take advantage of the 28-pin package the user must specify an input range of 0 to +10V, ±5V or ±10V when ordering. Four basic product grades are available; J and K models are specified over a temperature range of 0°C to +70°C while the S and T models are specified over an extended temperature range of −55°C to +125°C. Full screening to MIL-STD-883C and processing in accordance with Method 5008.1 is available with models specified as "B."

* ±12V operation possible; consult factory for further information.

FUNCTIONAL DIAGRAM



SPECIFICATIONS

(Typical @ + 25°C with V_{CC} = + 15V, V_{EE} = - 15V, V_{LOGIC} = + 5V, unless otherwise specified.)

MODEL	HS 941XJ	HS 941XK	HS 941XS	HS 941XT
TRANSFER CHARACTERISTICS				
Resolution	12-Bits	•	•	•
Number of Channels	8 Single-Ended	•	•	•
Throughput Rate	25 kHz	•	•	•
ANALOG INPUTS				
Input Ranges[1] (Specified as a suffix in the model number. See Ordering Guide.)		•	•	•
HS 9410	0 to + 10V	•	•	•
HS 9411	± 5V	•	•	•
HS 9412	± 10V			
Input Bias Current per Channel		•	•	•
I_{IB} 25°C	± 10nA		± 250nA max	•
- 55°C to + 125°C				
Input Impedance		•	•	•
ON Channel	$10^{10}\ \Omega$ || 100pf	•	•	•
OFF Channel	$10^{10}\ \Omega$ || 10pf			
DIGITAL INPUTS				
Logic Inputs				
R/C, A_0		•	•	•
V_{IH} min	+ 2.4V	•	•	•
V_{IH} max	+ 5.5V	•	•	•
V_{IL} max	+ 0.8V	•	•	•
V_{IL} min	- 0.5V	•	•	•
I_{IL} max	± 5μA max	•	•	•
I_{IH} max	± 5μA max			
Multiplexer Inputs		•	•	•
V_{IL} max	+ 0.8V	•	+ 4.0V[2]	+ 4.0V[2]
V_{IH} min	+ 2.4V	•	•	•
Input Capacitance (All Digital Inputs)	5pF typ			
Minimum Start Pulse		•	•	•
R/C-Negative	50ns			
SIGNAL DYNAMICS				
Conversion Time		•	•	•
12-Bit Conversion	25μs max	•	•	•
8-Bit Conversion	19μs max			
DIGITAL OUTPUTS				
Logic Outputs				
DB_{11}-DB_0, STS		•	•	•
Logic 0	+ 0.4V max, $I_{OL} \leq$ 1.6mA	•	•	•
Logic 1	+ 2.4V min, $I_{OH} \leq$ 0.5mA	•	•	•
Leakage (High Z State)	± 5μA typ (DB_{11}-DB_0 only)	•	•	•
Capacitance	5pF typ			
Output Code Configuration		•	•	•
Unipolar	Positive True Binary	•	•	•
Bipolar	Positive True Offset Binary			
POWER SUPPLY				
V_{LOGIC}	+ 4.5 to + 5.5 Volts @ 11mA max	•	•	•
V_{CC}	+ 13.5 to + 16.5 Volts @ 16mA max	•	•	•
V_{EE}	- 13.5 to - 16.5 Volts @ 7mA max	•	•	•
Power Dissipation	400mW max		700mW typ, 1W max	700mW typ, 1W max
Rejection[3]		•	•	•
V_{LOGIC}	0.002%/% typ, 0.005%/% max	•	•	•
V_{CC}	0.002%/% typ, 0.005%/% max	•	•	•
V_{EE}	0.002%/% typ, 0.005%/% max	•	•	•
ACCURACY				
Linearity Error (% of F.S.R. max)	± 0.025	± 0.012	± 0.025	± 0.012
Offset[4]		•	•	•
Unipolar (% of F.S.R. max)	± 0.05	•	•	•
Bipolar (% of F.S.R. max)	± 0.25	± 0.1	± 0.25	± 0.1
Gain[4] (% to F.S.R. max)	± 0.3	•	•	•
STABILITY				
Linearity (ppm/°C max)	± 0.5	± 0.5	± 2.5	± 2.5
Unipolar Offset (ppm/°C max)	± 10	± 5	± 25	± 20
Bipolar Offset (ppm/°C max)	± 25	± 20	± 25	± 20
Gain (Scale Factor)(ppm/°C max)	± 50	± 20	± 50	± 25
TEMPERATURE RANGE				
Operating	0°C to + 70°C	•	- 55°C to + 125°C	- 55°C to + 125°C
Storage	- 25°C to + 85°C	•	- 65°C to + 150°C	- 55°C to + 125°C

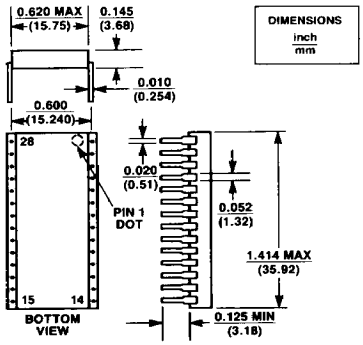
NOTES

1. For J and K models, positive analog input voltage should not exceed V_{CC} - 4 volts. Exceeding V_{CC} - 4 volts can cause an OFF channel to be turned ON. Negative input voltages and input voltages for S and T models may go to supply voltages. Input voltages exceeding these values will not result in permanent damage as long as the absolute maximum ratings are not exceeded. 2. 1K pullup to + 5V recommended for MA_0-MA_2 when driven by TTL. 3. Maximum change over rated supply voltage. 4. Externally adjustable to zero. See Applications Information.

*Specifications same as HS 9410J

PACKAGE OUTLINE

Dimensions shown in inches and (mm).



CONTROL FUNCTIONS

The HS 9410 Series contains control functions necessary to provide for microprocessor interface. All control functions are defined in Tables 1, 2, and 3.

Function	Definition	Function
R/$\overline{C}$	Read/Convert	1. ↓ initiates conversion. 2. Low (0) disconnects data bus. 3. High (1) initiates read.
A_0	Device Address	1. Selects conversion mode. 12-bits if low (0), 8-bits if high (1) when R/$\overline{C}$ ↓. 2. In read mode A_0 selects the output format. If low (0) then 8 MSB's (high and middle byte) or if high (1) then only low byte and trailing zeroes.
MA_0 MA_1 MA_2	Multiplexer Address	Select Channels 1-8 (see MUX Logic Table 3)

Table 1. Defining the Control Functions

PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	DB_{10}/DB_2	28	DB_9/DB_1
2	DB_{11}(MSB)/DB_3	27	DB_8/DB_0
3	A_0	26	DB_7
4	R/$\overline{C}$	25	DB_6
5	GROUND	24	DB_5
6	V_{LOGIC}	23	DB_4
7	V_{EE}	22	STS(STATUS)
8	MUX ADDRESS A_2	21	GAIN
9	MUX ADDRESS A_1	20	OFFSET
10	MUX ADDRESS A_0	19	V_{CC}
11	INPUT CH 1	18	INPUT CH 5
12	INPUT CH 2	17	INPUT CH 6
13	INPUT CH 3	16	INPUT CH 7
14	INPUT CH 4	15	INPUT CH 8

Control Inputs		Operation
R/$\overline{C}$	A_0	
↓	0	Initiates 12-bit conversion
↓	1	Initiates 8-bit conversion
1	0	Enables 8 MSB's (high byte)
1	1	Enables 4 LSB's (low byte) and 4 trailing zeros
0	X	Output data (DB) goes to high impedance state.

Table 2. Truth Table—Control Inputs

Mux Address Inputs			Channel Selected
A_2	A_1	A_0	
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

NOTES:
1. 1 indicates logic HIGH.
2. 0 indicates logic LOW.
3. X indicates don't care.
4. ↓ indicates operation commences on high to low transition.
5. MSB → XXXX (High Byte) XXXX (Middle Byte)
6. XXXX (Low Byte) ← LSB

Table 3. Truth Table—Multiplexer Address

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Common GND . . . . . 0 to + 16.5V
V_{EE} to Common GND . . . . . 0 to − 16.5V
V_{LOGIC} to Common GND . . . . . 0 to + 7V
Control Inputs (A_0, R/C) to
Common GND . . . . . − 0.5V to V_{LOGIC} + 0.5V
Power Dissipation 1.3W
Lead Temperature, Soldering . . . . . 300°C, 10Sec
Maximum Input Voltage . . . . . V_{CC} + 20V
Minimum Input Voltage . . . . . V_{EE} − 20V
Analog Input Maximum Current 25mA

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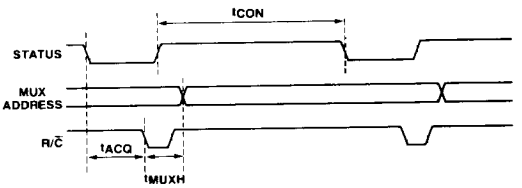
APPLICATIONS INFORMATION

TIMING

The timing diagrams are shown in Figures 1 through 6. Figures 1 and 2 show how the multiplexer addressing is related to the convert cycle, while Figures 3 and 4 show the timing sequence to start either a 12- or an 8-bit conversion. Figures 5 and 6 show how to read the multiplexed data from the internal register in the HS 9410.

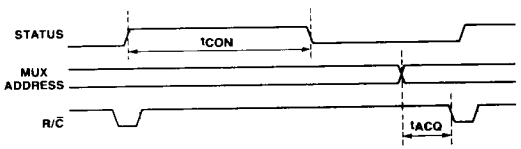
Figures 1 and 2

The multiplexer address can be changed either during or after a conversion, but care must be taken not to change the address within 1 microsecond after the convert command to insure that the sample/hold will not start to acquire the signal of the new channel. After the multiplexer address has been changed, you must allow the sample/hold at least 10 microseconds **in sample mode** to acquire the new input signal.



t_{MUXH}	Multiplexer address hold time after convert command	1μs min
t_{ACQ}	Minimum time between conversions (S/H acquisition time)	10μs min
t_{CON}	Conversion time for -12 bit resolution	25μs max
	- 8 bit resolution	19μs max

Figure 1. Timing Diagram 8/12-Bit Conversion, MUX Address Changes During Conversion

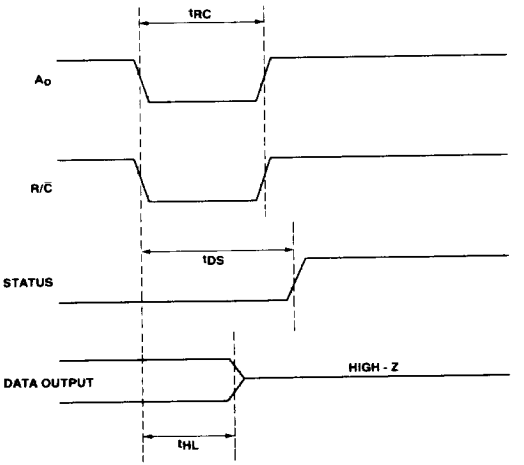


t_{ACQ}	Minimum time between MUX address change and convert command	10μs min
t_{CON}	Conversion time - Specifications, see Figure 1	

Figure 2. Timing Diagram 8/12-Bit Conversion, MUX Address Changes Between Conversions

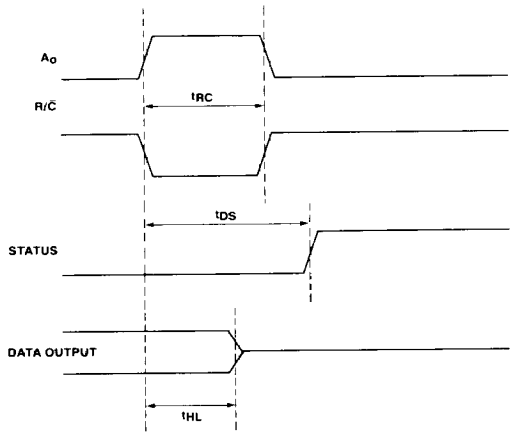
Figures 3 and 4

Figures 3 and 4 show how to start a convert cycle. The logic level of the A_0 line determines whether a 12- or 8-bit conversion will be initiated. If A_0 is low during the start convert command, a 12 bit conversion will be started; if A_0 is high, an 8-bit conversion will occur. The A_0 line has to be setup when the R/$\overline{C}$ line goes to logic '0' and must remain in the desired level for at least 150 ns. The R/$\overline{C}$ line is used both to start a conversion and to read the output data. If R/$\overline{C}$ is going low a conversion is initiated. This is indicated by the STATUS line going high. A second start convert command during a conversion will be ignored. The R/$\overline{C}$ pulse must have a minimum width of 150 ns. For optimum performance the rising edge of the R/$\overline{C}$ pulse should not occur during a conversion if the conversion has been in progress for more than 1.5 microseconds, i.e., the negative R/C pulse should be either shorter than 1.5 microseconds or longer than the conversion time.



t_{RC}	R/C pulse width, A_0 pulse width (Note 1)	50 ns min
t_{DS}	Status delay from R/$\overline{C}$	200 ns max
t_{HL}	Output float delay	150 ns max

Figure 3. Timing Diagram to Start a 12-Bit Conversion

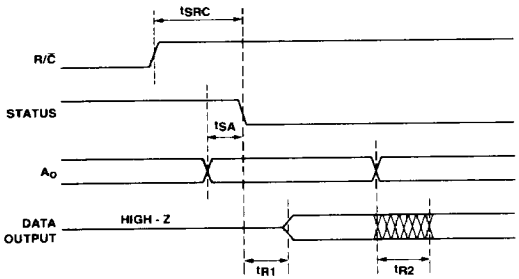


t_{RC}	R/C pulse width, A_0 pulse width (Note 1)	50 ns min
t_{DS}	Status delay from R/$\overline{C}$	200 ns max
t_{HL}	Output float delay	150 ns max

Figure 4. Timing Diagram to Start an 8-Bit Conversion

Figures 5 and 6

If a conversion is in progress the data output lines are disabled and in the high-impedance state. Data can be enabled by bringing the R/$\overline{C}$ line high after a conversion is complete (this is indicated by the STATUS line going low; Fig. 6). If R/$\overline{C}$ has been returned high during a conversion the data outputs will be enabled automatically after STATUS goes low (Fig. 5). The A_0 line is used to address either the 8 upper data bits or the 4 lower data bits followed by 4 trailing zeros. If an 8-bit conversion has been performed the lower 4 bits will always be '0'. After an 8-bit conversion, it is not necessary to read the lower 4 bits prior to starting a new conversion. Note that A_0 only controls the address of the two data bytes while the high impedance state of the output buffers is controlled by the R/$\overline{C}$ and STATUS line. The output buffers will not return to the high impedance state when A_0 is changed to address the second data byte.

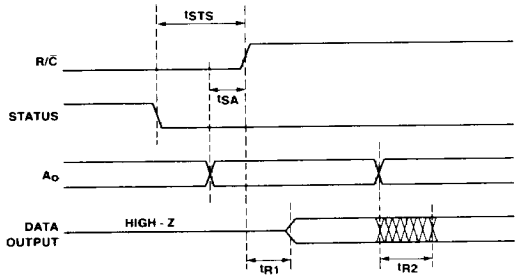


t_{SRC}	R/C set-up time prior to status going low	0 ns min
t_{SA}	A_0 set-up time prior to status going low (Note 2)	100 ns min
t_{R1}	Access time, 1st data byte (from status)	125 ns max
t_{R2}	Access time, 2nd data byte (from A_0)	225 ns max

Figure 5. Timing Diagram Read Cycle, R/$\overline{C}$ Going High During Conversion

NOTES:

1. For optimum performance the positive edge of the R/C pulse should not occur during a conversion if the conversion has been started for more than 4.5 microseconds. The negative R/C pulse should be longer than the 4.5 microseconds before STATUS goes high.
2. If the set-up time for A_0 cannot be met, the access time for the first data byte will be increased. In that case the first data byte will become valid 225 ns max after the change of the A_0 line.



t_{STS}	Status going low prior to R/C going high	0 ns min
t_{SA}	A_0 set-up time prior to R/C going high (Note 2)	100 ns min
t_{R1}	Access time, 1st data byte (from R/C)	125 ns max
t_{R2}	Access time, 2nd data byte (from A_0)	225 ns max

Figure 6. Timing Diagram Read Cycle, R/$\overline{C}$ Going High After Conversion

USING THE A_0 LINE

The state of A_0 at the start of a conversion places the DAS in either a full 12-bit conversion or in an 8-bit 'short cycle' mode. During a READ at the end of a conversion A_0 is used to format the data as follows:

	MODE
1. Prior to Conversion (WRITE)	
$A_0 = 1$	Short cycle 8-bit conversion
$A_0 = 0$	Full 12-bit conversion
2. After Conversion (READ)	
$A_0 = 1$	Data = Low Byte (LSB) followed by zeros
$A_0 = 0$	Data = High Byte (MSB's) followed by middle byte.

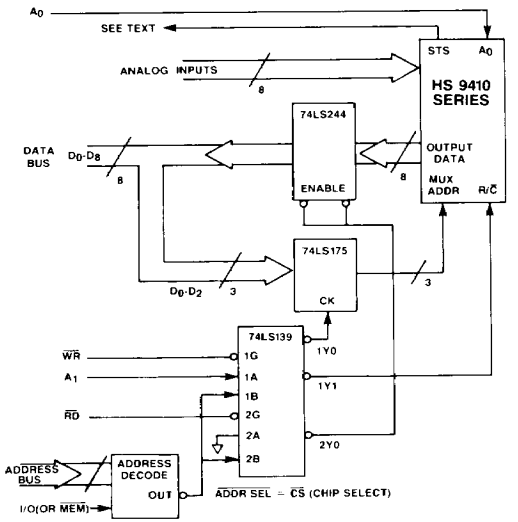
In a μP application A_0 can be considered a pair of $\overline{W/R}$ locations as follows:

	MODE
1. Prior to Conversion (WRITE)	
$\overline{W/R} = 0$ in low address ($A_0 = 0$)	Full 12-bit conversion
$\overline{W/R} = 0$ in high address ($A_0 = 1$)	Short cycle 8-bit conversion
2. After Conversion (READ)	
$\overline{W/R} = 1$ in high address ($A_0 = 1$)	LSB's & zeros
$\overline{W/R} = 1$ in low address ($A_0 = 0$)	8 MSB's only

MICROPROCESSOR INTERFACE

The HS 9410 Series DAS can be interfaced with most popular 8-bit microprocessors. The DAS may be either positioned in a memory location (memory map) or as an I/O device. In the case of memory mapping, the DAS acts as a static RAM where READ and WRITE instructions are given to the selected address. When the DAS is connected as an I/O device, the I/O enable can be substituted for the $\overline{MEMR}$ or $\overline{MEMW}$ command. Figure 7 shows a typical scheme to implement this interface.

STS is not used in this example; the μP must read data 30μs after conversion starts. This delay can be generated with NOP or other instructions inserted between the WRITE and READ functions. The STS line can also be used to cause the processor to WAIT or HALT or can be used as an interrupt line such as IREQ (in the case of 6800 or 6502).



A_0	A_1	WR	RD	ADDR SEL	HS 9410 Function Read/Write	Operation
X	0	↓	1	0	WRITE	MUX ADDRESS
0	1	↓	↑	0	WRITE	START 12-BIT CONV.
1	1	↓	1	0	WRITE	START 8-BIT CONV.
0	X	1	0	0	READ	HIGH BYTE (8 MSB's)
1	X	1	0	0	READ	LOW BYTE (4 LSB's)

NOTES:
1. 1 indicates logic HIGH. 2. 0 indicates logic LOW. 3. X indicates don't care.
4. ↓ indicates operation commences on low to high transition.
5. ↓ indicates operation commences on high to low transition.

Figure 7. Interfacing the HS 9410 Series

INPUT EXPANSION

The DAS is configured with an 8 channel high level multiplexer input. This was done to optimize package size (28 pin DIP) and cost. In the event the user wishes to increase the number of input channels, a double rank MUX input is recommended (series connected). This typical configuration is shown in Figure 8.

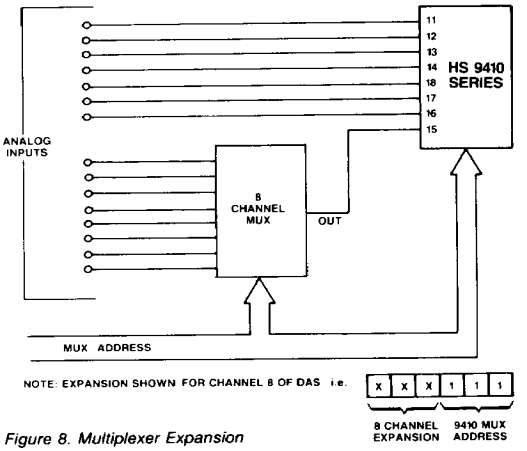


Figure 8. Multiplexer Expansion

ZERO AND GAIN CONNECTIONS

The DAS is normally used with external zero and gain calibration potentiometers. However, if maximum accuracy is not required, they may be omitted. The zero control has a range of about ± 20LSB, and the gain control has a range of about ± 13LSB.

Proper gain and zero calibration requires great care and the use of extremely sensitive and accurate instruments. The voltage source used as a signal input must be very stable. It also should be capable of being set to within 1/10LSB at both ends of its range.

The DAS's zero and gain adjustments are independent of each other if the zero (or offset) adjustment is made first.

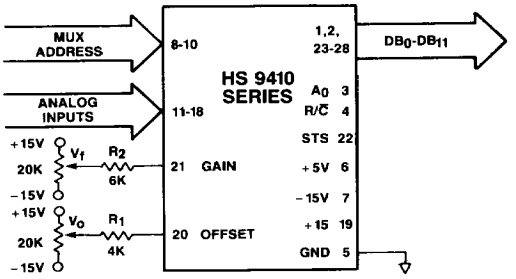


Figure 9. Gain and Offset Input Connections

ZERO ADJUSTMENT PROCEDURE

1. For unipolar ranges:
   a) Set input voltage precisely to +½LSB.
   b) Adjust zero control until converter is switching from 000000000000 to 000000000001.
2. For bipolar ranges:
   a) Set input voltage precisely to ½LSB above –F.S.
   b) Adjust zero control until converter is switching from 000000000000 to 000000000001
3. When offset adjust is not used, tie pin 20 to ground.

GAIN ADJUSTMENT PROCEDURE

1. Set input voltage precisely to ½LSB less than 'all bits on' value. Note that this is 1½LSB less than nominal full scale.
2. Adjust gain control until converter is switching from 111111111110 to 111111111111.
3. When gain adjust is not used, tie pin 21 to ground.

Table 4 summarizes the zero and gain adjustment procedure, and shows the proper input test voltages used in calibrating the DAS.

Input Voltage Range	Adjustment	Input Voltage	Adjust input to point where converter is just on the verge of switching between the two codes shown.[1]
0 to +10V	ZERO	1.22mV	0000 0000 0000
	GAIN	9.9963V	1111 1111 1110
±5V	ZERO	–4.9988V	0000 0000 0000
	GAIN	4.9963V	1111 1111 1110
±10V	ZERO	–9.9976V	0000 0000 0000
	GAIN	9.9927V	1111 1111 1110

[1]Codes shown are natural binary for unipolar input ranges and offset binary for bipolar ranges.

0 = transition between a logic 0 and a logic 1 state. All gain, offset and linearity measurements are performed using the transition test method.

Table 4. Calibration Data

POWER SUPPLY CONSIDERATION

Power supplies used for the DAS should be selected for low noise operation. In particular they should be free of high frequency noise. Unstable output codes may result with noisy power sources. It is important to remember that 2.44mV is 1LSB for a 10 volt input.

Decoupling capacitors are recommended on all power supply pins located as close to the converter as possible. Suitable decoupling capacitors are 10μF tantalum type in parallel with 0.1μF disc ceramic type.

GROUNDING CONSIDERATIONS

The common at pin 5 is the ground reference point for the internal reference and is thus the high quality ground for the DAS. In order to achieve all of the high accuracy performance available from the DAS in an environment of high digital noise content, care should be taken when handling analog and digital grounds, as follows. Where analog and digital grounds are run separately on the PCB, these should be connected together at the package (pin 5). However, if the grounds are connected separately in the system for other reasons, then only the analog ground should be connected at the package to pin 5. If digital common contains high frequency noise beyond 200mV, this noise may feed through the converter, so that some caution will be required.

It is also important in the layout to carefully consider the placement of digital lines. It is recommended that digital lines not be run directly under the DAS. For optimum system performance, if space permits, a ground plane is advised under the DAS. This should be connected to a digital ground. In packaging the assembled DAS, the designer should also try to minimize any capacitive coupling that might occur at the top to the device. Parallel runs between analog and digital signals should be avoided. A star system ground is the most preferred layout method. See Figure 10.

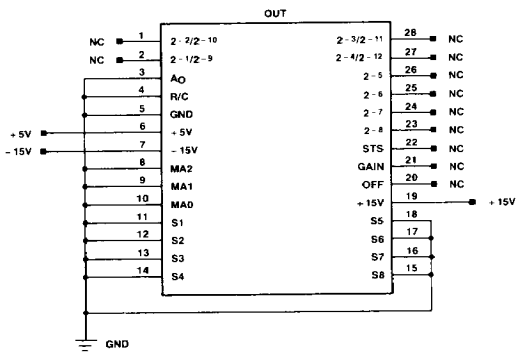


Figure 10. HS 9410 Burn-In Schematic

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ORDERING INFORMATION

Model Number[1]	Input Range	System Accuracy (% FSR)	Full Scale T.C. (ppm/°C)	Temp. Range	MIL Screening
HS 94XXJ	SEE NOTE 1	±0.025	50.0	0°C to +70°C	—
HS 94XXK		±0.012	20.0	0°C to +70°C	—
HS 94XXS		±0.025	50.0	−55°C to +125°C	—
HS 94XXT		±0.012	25.0	−55°C to +125°C	—
HS 94XXS/B		±0.025	50.0	−55°C to +125°C	883C
HS 94XXT/B		±0.012	25.0	−55°C to +125°C	883C

NOTES:

1 HS 94XX

MODEL SUFFIX	INPUT RANGE
10	0 to +10V
11	±5V
12	±10V

Add letter suffix as required above.

Specifications subject to change without notice.

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electro-static fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed. Devices should be handled at static safe workstations only. Unused digital inputs must be grounded or tied to the logic supply voltage. Unless otherwise noted, the voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below −0.5 volts. If this condition cannot be maintained, limit input current on digital inputs by using series resistors or contact Hybrid Systems for technical assistance.