T-67-21-55

LC74HC138M

3035A

CMOS High-Speed Standard Logic
LC74HC Series

3 to 8-Line Decoder

E2100A

Features

- The LC74HC138M decodes a three-bit address to one-of-eight active-low outputs.
- Uses CMOS silicon gate process technology to achieve operating speeds similar to LS-TTL (74LS138) with the low power dissipation and high noise margin of standard CMOS IC's.
- Has buffered outputs, improving the output transition characteristics.
- All inputs and outputs are protected from damage.
- The LC74HC138M is functionally as well as pin-out compatible with the standard 54LS/74LS TTL logic family.

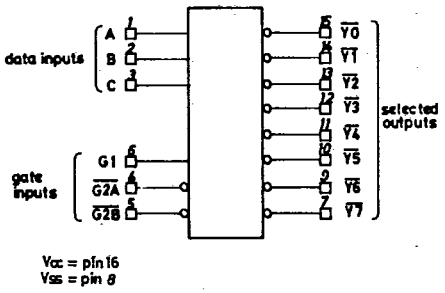
Absolute Maximum Tatings/Ta=25±2°C, V_{SS}=0V

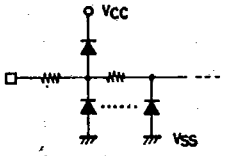
				unit
Maximum Supply Voltage	V_{CC} max		V_{SS}-0.5 to V_{SS}+7.0	V
Maximum Input Voltage	V_{IN} max		V_{SS}-0.5 to V_{CC}+0.5	V
Maximum Output Voltage	V_{OUT} max		V_{SS}-0.5 to V_{CC}+0.5	V
Maximum Output Current	I_{OUT}	Per output	±25	mA
Current Dissipation	I_{CC}/I_{Gnd}		±50	mA
Clamp Diode Current	I_K	Per input pin (Input protector)	±20	mA
Allowable Power Dissipation	Pd max	Per Package Ta≦85°C	150	mW
Storage Temperature	Tstg		−65 to +150	°C
Lead Temperature and Time	Tsol	t=10sec	260	°C

Allowable Operating Conditions/V_{SS}=0V

			unit
Supply Voltage	V_{CC}	2.0 to 6.0	V
Input Voltage	V_{IN}	0 to V_{CC}	V
Output Voltage	V_{OUT}	0 to V_{CC}	V
Operating Temperature	Topg	−40 to +85	°C
Input Rise/Fall Time	tr, tf	0 to 500	ns

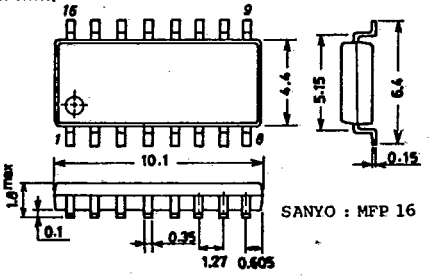
Equivalent Circuit and Logic Diagram





Input Protector

Case Outline 3035A-M161C
(unit: mm)



For details, refer to the description of the LC74HC138.