Dec 1998 Version1.0

General Description

The AL2007LA is a Phase-Locked Loop (PLL) frequency synthesizer constructed in CMOS on single monolithic structure.
The PLL macrofunctions provide frequency multiplication capabilities.
The output clock frequency Fout is related to the reference input clock frequency Fin by the following equation:

$$Fout = (m*Fin) / (p* 2^{s})$$

Where,
Fout is the output clock frequency.
Fin is the reference input clock frequency.
m,p and s are the values for programmable dividers.
AL2007LA consists of a phase/Frequency Detector(PFD), a Charge Pump an External Loop Filter, a Voltage Controlled Oscillator(VCO), a 6bit Pre-divider, an 8bit Main divider and 2bit Post Scaler as shown in Figure1.

Features

- **0.35um CMOS device technology**
- **3.3 Volt Single power supply**
- **Output frequency range: 20~ 170 MHz**
- **Jitter ±150ps**
- **Duty ratio 40% to 60% at 170MHz**
- **Frequency changed by programmable divider**
- **Power down mode**

IMPORTANT NOTICE
- Please contact SEC application engineer to confirm the proper selection of M,P,S value.

FUNCTIONAL BLOCK DIAGRAM

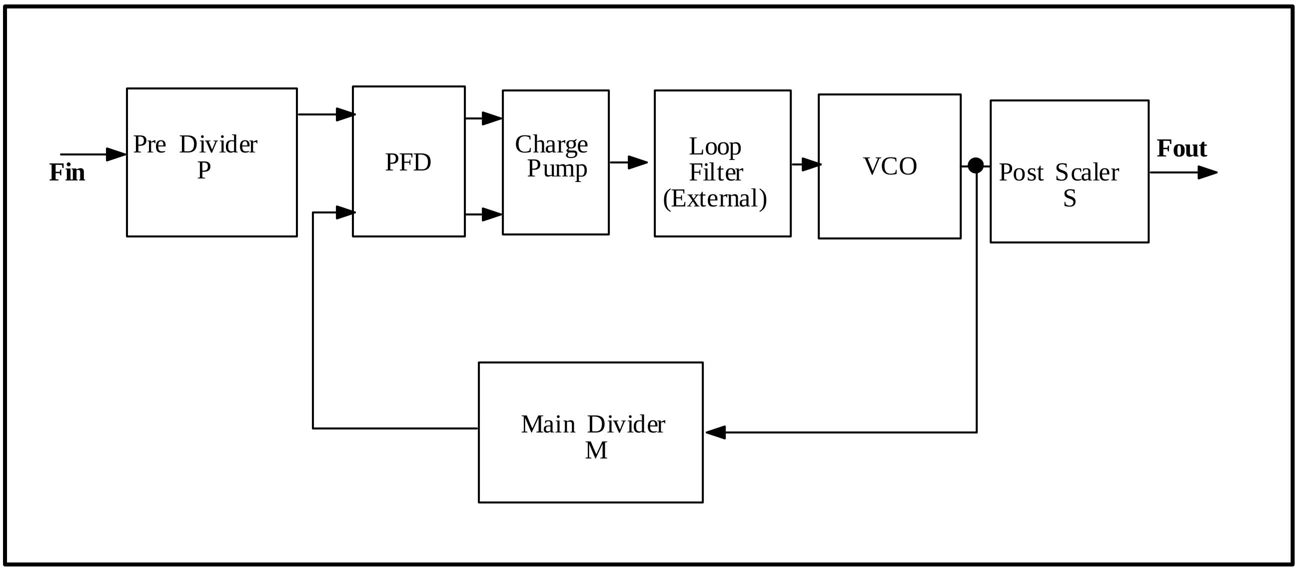


Figure 1. Phase Lockd Loop Block Diagram

CORE PIN DESCRIPTION

NAME	I/O TYPE	I/O PAD	PIN DESCRIPTION
VDD	DP	vddd	Digital power supply
VSS	DG	vssd	Digital ground
VDDA	AP	vdda	Analog power supply
VSSA	AG	vssa	Analog ground
VBB	AB/DB	vbba	Analog/Digital sub bias Power
FIN	DI	picc_bb	PLL clock input
FILTER	AO	poar50_bb	. Pump out is connected to Filter . A capacitor is connected between the pin and analog ground
FOUT	DO	pot12_bb	20MHz~170MHz clock output
PWRDN	DI	picc_bb	FSPLL clock power down. -PWRDN is High, PLL do not operating under this condition. -If isn't used this pin, tied to VSS.
P[5:0]	DI	picc_bb	The values for 6bit programmable pre-divider.
M[7:0]	DI	picc_bb	The values for 8bit programmable main divider.
S[1:0]	DI	picc_bb	The values for 2bit programmable post scaler.

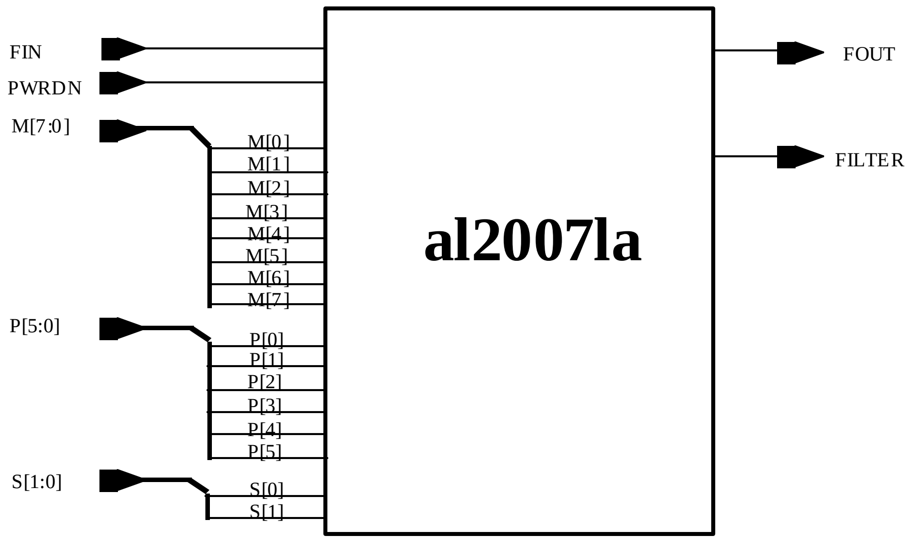
I/O TYPE ABBR.

- AI : Analog Input
- DI : Digital Input
- AO : Analog Output
- DO : Analog Output

- AP : Analog Power
- AG : Analog Ground
- AB : Analog Sub Bias
- DP : Digital Power
- DG : Digital Ground
- DB : Digital Sub Vias

- BD : Bidirectional Port

CORE CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

	Symbol	Value	Unit	Applicable pin
Supply Voltage	VDD VDDA	-0.3 to 3.8	V	VDD,VDDA,VSS,VSSA
Voltage on Any Digital Pin	Vin	Vss-0.3 to Vdd+0.3	V	P[5:0],M[7:0],S[1:0] PWRDN
Storage Temperature	Tstg	-45to 125	°C	-

NOTES
1. ABSOLUTE MAXIMUM RATING specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions is not implied.
2. All voltages are measured with respect to VSS unless otherwise specified.
3. 100pF capacitor is discharged through a 1.5K resistor (Human body model)

Recommended Operating Conditions

	Symbol	Min	Typ	Max	Unit
Supply Voltage Differential	VDD - VDDA	-0.1	0	+0.1	V
Oscillator Frequency	Fosc	10		40	Mhz
External Loop Filter Capacitance	L_F		820		pF
Operating Temperature	Topr	0		70	°C

NOTES
1. It is strongly recommended that all the supply pins (VDDA, VDD) be powered from the same source to avoid power latch-up.

DC ELECTRICAL CHARACTERISTICS

	Symbol	Min	Typ	Max	Unit
Operating Voltage	VDD/VDDA	3.15	3.3	3.45	V
Digital Input Voltage High	Vih	2.0			V
Digital Input Voltage Low	Vil			0.8	V
Dynamic Current (CORE Level without I/O Cell)	Idd			3.5	mA
Power Down Current	Ipd			120	uA

AC ELECTRICAL CHARACTERISTICS

	Symbol	Min	Typ	Max	Unit
Input Frequency	F_{IN}	2	14.318	40	MHz
Output Clock Frequency	F_{OUT}	20		170	Mhz
Input Clock Duty Cycle	T_{ID}	40		60	%
Output Clock Duty Cycle	T_{OD}	40		60	%
Input Glitch Pulse Width	T_{IGP}	1			ns
Locking Time	T_{LT}			150	us
Cycle to Cycle Jitter	T_{JCC}	-150		+150	ps

Functional Description

A PLL is the circuit synchronizing an output signal (generated by an VCO) with a reference or input signal in frequency as well as in phase.

In this application, it includes the following basic blocks.

. The voltage-controlled oscillator to generate the output frequency
. The divider P devides the reference frequency by p
. The divider M devides the VCO output frequency by m
. The divider S divides the VCO output frequency by s
. The phase frequency detector detects the phase difference between the reference frequency and the output frequency (after division) and controls the charge pump voltage.
. The loop filter removes high frequency components in charge pump voltage and does smooth and clean control of VCO

The m, p, s values can be programmed by 16bit digital data from the external source. So the PLL can be locked in the desired frequency.

Fout = m * Fin / p*s

If Fin = 14.318MHz, and m=M+8 , p=P+2, s=2^S
Digital data format:

Main Divider	Pre Divider	Post Scaler
M7,M6,M5,M4,M3,M2,M1,M0	P5,P4,P3,P2,P1,P0	S0,S1

NOTES
. S[1] - S[0] : Output Frequency Scaler
. M[7] - M[0] : VCO Frequency Divider
. P[5] - P[0] : Reference Frequency Input Divider

OUTPUT FREQUENCY EQUATION & TABLE

Frequency Equation : $$F_{OUT} = \frac{(M+8)}{(P+2) \times 2^S} \times F_{IN}$$

Table 1. Example of Divider Ratio

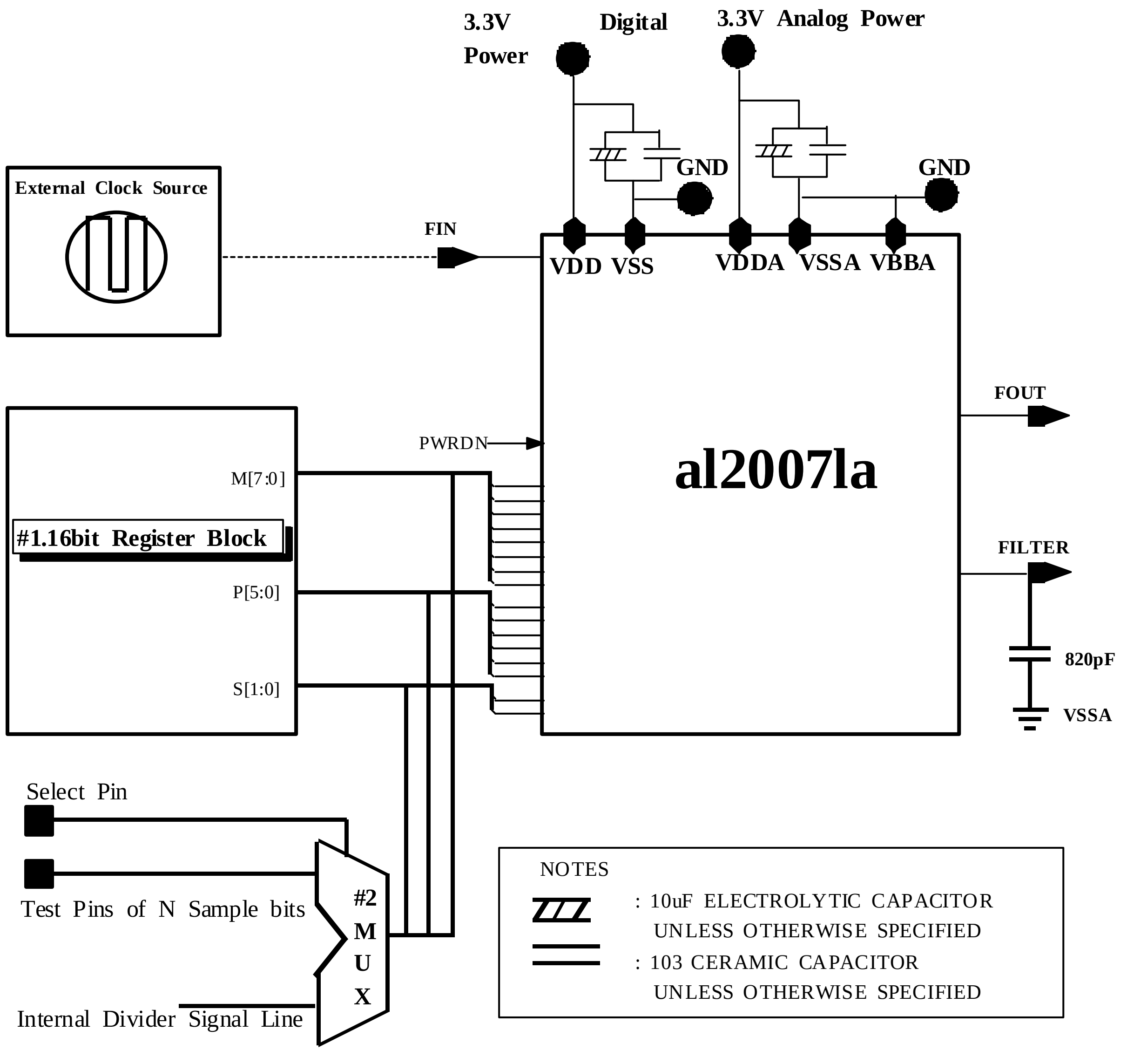
M7	M6	M5	M4	M3	M2	M1	M0	M	m (M+8)	P6	P5	P4	P3	P2	P1	P0	P	p (P+2)	S1	S0	2^S
0	1	0	1	0	1	0	1	85	93	0	1	0	1	0	1	0	42	44	0	0	1

IMPORTANT NOTICE
- Please contact SEC application engineer to confirm the proper selection of M,P,S value.

CORE EVALUATION GUIDE

For the embedded PLL, we must consider the test circuits for the embedded PLL core inmultiple applications. Hence the following requirements should be satisfied.

- The FILTER and FOUT pins must be bypassed for external test.
- For PLL test (Below 2 examples),
  it is needed to control the dividers - M[7:0],P[5:0] and S[1:0] -that generate multiple clocks.
  Example #1. Registers can be used for easy control of divider values.
  Example #2. N sample bits of 16-bit divider pins can be bypassed for test using MUX.



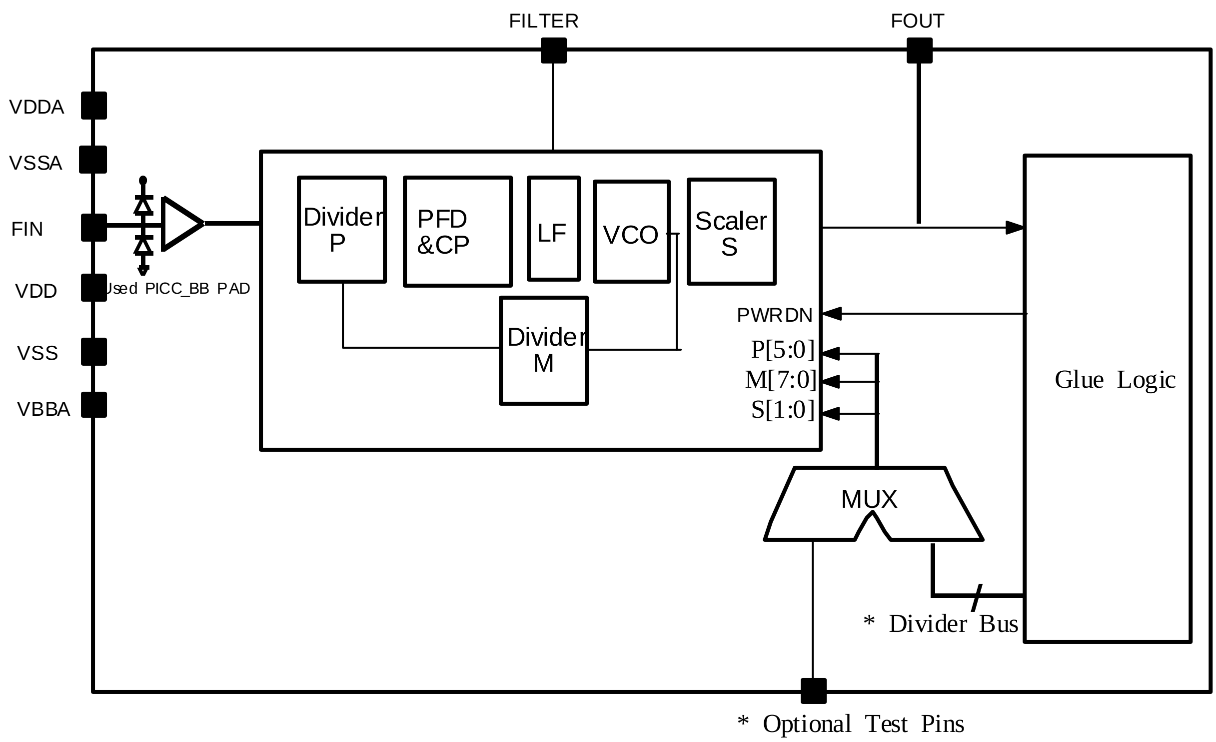
CORE LAYOUT GUIDE

- The digital power(VDD,VSS) and the analog power(VDA,VSSA) must be dedicated to PLL only and seperated. If the dedicated VDD and VSS is not allowed that of the least power consuming block is shared with the PLL.
- The PIA pad is used as a FILTER pad that contains only ESD production diodes without any resistors and buffers.
- The FOUT and FILTER pins must be placed far from the internal signals in order to avoid overlapping signal lines.
- The blocks having a large digital switching current must be located away from the PLL core.
- The PLL core must be shielded by guardring.
- For the FOUT pad, you can use a custom drive buffer or POT12 buffer considering the drive current.

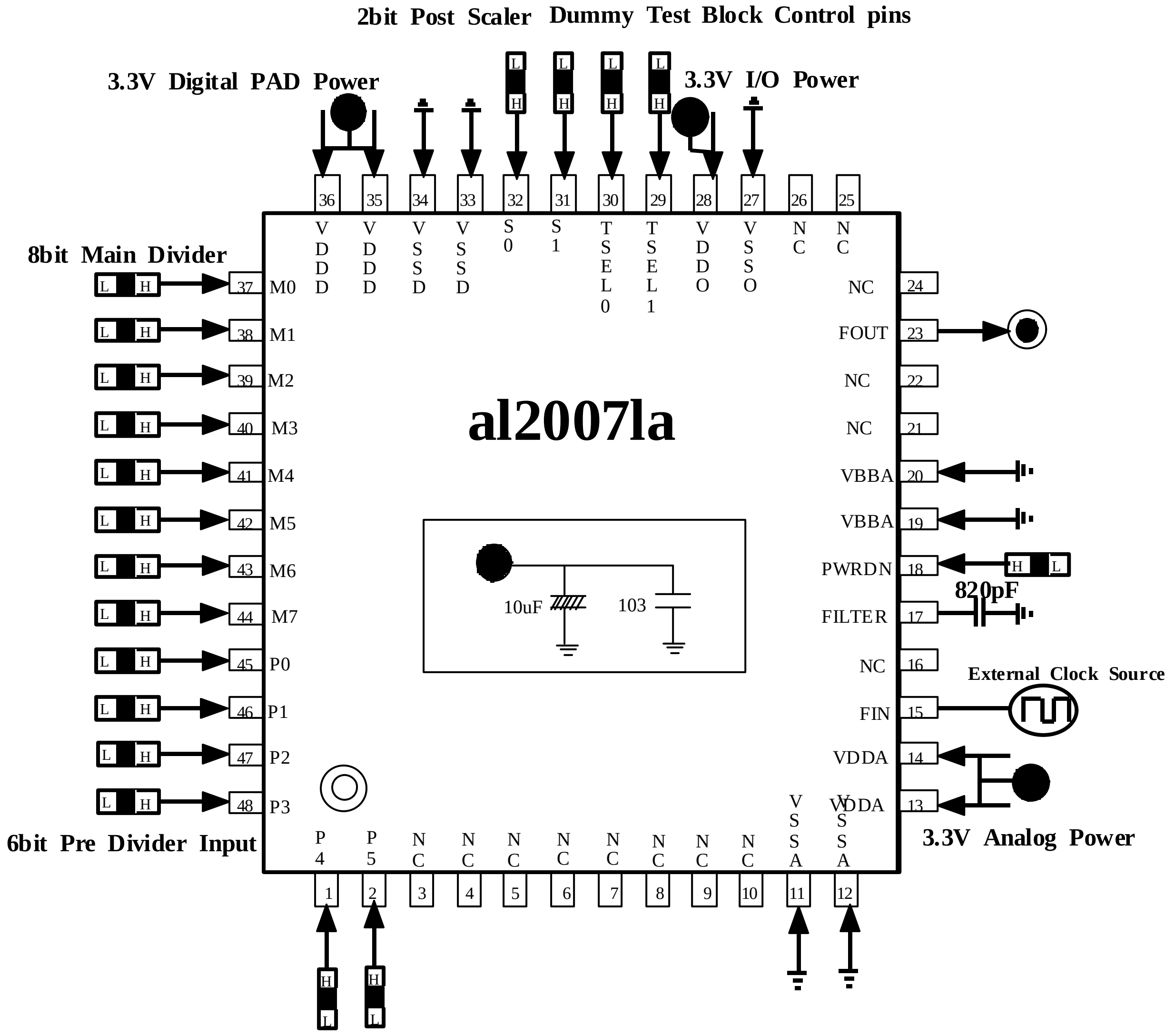
WITHOUT XTAL-DRIVER USERS GUIDE

- There are two crystal driver cell (XTAL-OSC and PSOSCM2) options for the AL2007LA PLL core.
  1. If the crystal component not used , an external clock source is applied to the FIN
     *Please contact an SEC application engineer when using a crystal.
  2. If the crystal component not used , an external clock I/O Buffer offered from Samsung's STD90 library is recommanded for use
  - When implementing an embedded PLL block, the following pins must be bypassed externally for testing the PLL locking function:
  * Without Xtal-driver : FIN,FILTER,FOUT,VDDA,VSSA,VDD and VSS.

Figure2. The example of PLL block without crystal component (Normal Case)



PACKAGE CONFIGURATION



NOTES
* TSEL0,TSEL1 pins are internal dummy block test pins.
* NC is Noconnection pin

PACKAGE PIN DESCRIPTION

NAME	PIN NO	I/O TYPE	PIN DESCRIPTION
VDDD	35,36	DP	Digital power supply
VSSD	33,34	DG	Digital ground
PWRDN	18	DI	FSPLL clock power down -PWRDN is High, PLL do not operating under this condition. - If isn't used this pin, tied to VSS.
P[0]~P[5]	1,2,45~48	DI	Pre-Divider Input(LSB)
VDDA	13,14	AP	Analog power supply
VSSA	11,12	AG	Analog ground
VBBA	19,20	AB/DB	Analog / Digtal Sub Bias Power
FIN	15	AI	Crystal input or external F_{REF} input
FOUT	22	DO	20MHZ~170MHz clock output
FILTER	17	AO	Pump out is connected to the FILTER. A 820pF Capcitor is connected between the pin and analog pin
TSEL0	30	DI	FOUT divide control pins. -End users used not this pins, tied to VDD or VSS
TSEL1	29	DI	FOUT divide control pins. -End users used not this pins, tied to VDD or VSS
S[0]~S[1]	31,32	DI	Post scaler input
M[0]~M[7]	37~44	DI	8bit main divider input
VDDO	28	PP	I/O PAD Power
VSSO	27	PG	I/O PAD Ground

NOTES
1. I/O TYPE PP and PG denote PAD power and PAD ground respectively.

PLL Components

Figure1 is block diagram of the components of a PLL: phase frequency detector, chrge pump, voltage controlled oscillator, and loop filter.
In SEC technology, the loop filter is implemented as external components close to chip.

Phase detector : The phase dectector monitors the phase dfference between the Fref and Fvco,and generates a control signal when it detects difference between the two.
If the Fref frequency is higher than the Fvco frequency, its falling edge occures before(lead) the falling edge of the Fvco output. When this occures the phase detector signals the VCO to increase the frequency of the on-chip clock. If the falling edge of the Fref occures after(lag) the falling edge of the Fvco output, the detector signals the VCO to decrease on-chip clock frequency. Figure7 illustrates the lead and lag conditions. If the frequencies of the Fref and Fvco are the same, the detect or does not generate a control signal, so the frequencies remain the same.

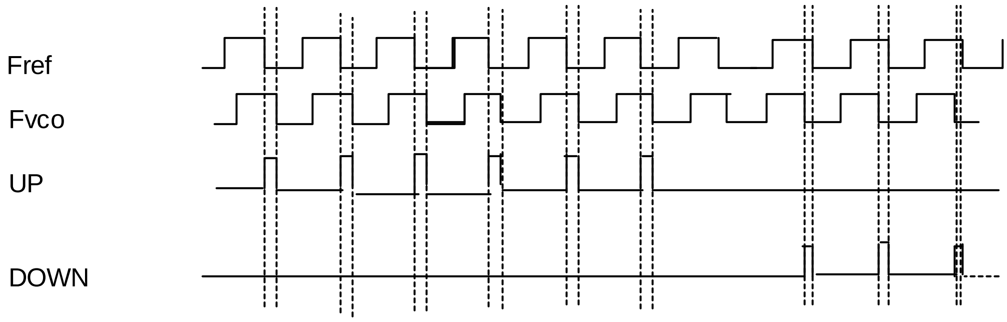


Figure3. Lead and Lag Clocking Relationships

Charge Pump : The charge pump converts the phase detector control signal to a charge in voltage across the external filter that drives the VCO. As the vcoltage Controlled Oscillator decreases, or increases, If the voltage remains constant, the frequency of the oscillator remains constant.

Loop Filter : The control signal that the phase detector generates for the charge pump may generate large excursions(ripples) each time the VCO output is compared to the system clock. To avoid overloading the VCO, a low pass filter samples and filters the high-frequency components out of the control signal. the filter is typically a single-pole RC filter consisting of a resistor and capacitor.

Voltage Controlled Oscillator(VCO) : The output voltage from the loop filter drives the VCO, causing its oscillation frequency to increas or decrease as a function of variations in voltage. When the VCO output matches the system clock in frequency and phase, the pahse detector stops sending a control signal to the charge pump, which in turn stabilizes the input voltage to the loop filter. The VCO frequency then remains constant, and the PLL remains locked onto the system clock

Frequency Synthesis

Frequency synthesis uses the system clock as a base frequency to generate higher/lower frequency clocks for internal logic.
For high speed applications in high-end designs, transmission line effects cause problems because of parastics and impedance mismatch among various on-board components.
These problems can be eliminated by moving the high frequency to the chip level.
On-chip clocks that are faster than the external system clock can be synthesized by inserting a divider in the feedback path. The divider is placed after voltage controlled oscillator, as illustrated in Figure1. The signal is running at M times the system clock frequency, so the PLL matches the divider signal output to the system clock. This configuation reduces the problem of interfacing to the system clock on the board, and it reduces the noise generated by the system clock oscillator and driver for all the components in the system

Design Considerations

The following design consideratios apply:

* Phase tolerance and jitter are independent of the PLL frequency.
* Jitter is affected by the noise frequency in the power(VDD/VSS,VDDA/VSSA) . It increases when the noise level increases.
* A CMOS-level input reference clock is recommend for signal compatibility with the PLL circuit. Other levels such as TTL may degrade the tolerances.
* The use of two, or more PLLs requires special design considerations. Please consult your application engineer for more information.
* The following apply to the noise level, which can be minimized by using good analog power and ground isolation techniques in the system:
  - Use wide PCB traces for POWER(VDD/VSS, VDDA/VSSA) connections to the PLL core. Seperate the traces from the chip's VDD/VSS,VDDA/VSSA supplies.
  - Use proper VDD/VSS,VDDA/VSSA de-coupling.
  - Use good power and ground sources on the board.
  - Use Power VBB for minimize substrate noise
* The PLL core should be placed as close as possible to the dedicated loop filter and analog **Power and ground pins.**
* It is inadvisable to locate noise-generating signals, such as data buses and high-current outputs, near the PLL I/O cells.
* Other related I/O signals should be placed near the PLL I/O but do not have any pre-defined placement restriction

PLL Specification

We appreciate your interest in our products. If you have further questions, please specify in the attached form. Thank you very much.

Parameter	Min	Typ	Max	Unit	Remarks
Supply Voltage					
Output frequency range					
Input frequency range					
Cycle to Cycle Jitter					
Lock up time					
Dynamic current					
Stand by current					
Output clock duty ratio					
Long term jitter					
Output slew rate					

- Do you need XTAL driver buffer in PLL Core?
  If you need it, what's the crystal frequency range? If not, What's the input frequency range?

- Do you need the lock detector?
- Do you need the I/O cell of SEC?
- Do you need the external pin for PLL test?
- What's the main frequency & frequency range?
- How many FSPLLs do you use in your system?
- What's output loading?
- Could you external/internal pin configurations as required?

Specially requested function list :