AN1126
APPLICATION NOTE

CURRENT SHARING OF THE L4973 IN A MULTIPHASE APPLICATION

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INTRODUCTION

The L4973 family is a 3.5A monolithic step-down dc-dc converter, available in POWERDIP18(12+3+3) and SO20L (12+4+4) plastic packages. The operating input supply voltage range is from 8V to 55V, and the output ranges from 3.3V (L4973D3.3) and 5.1V(L4973D5.1) to 40V. Other regulated outputs below 3.3V are also possible (See Application Note AN938).

Using two L4973D is possible to deliver up to 7A with a good sharing between the two sections or a redundant 3.5A. The two devices work at a switching frequency of 200kHz. At Vcc = 24V, Vo = 5.1V at 7A the efficiency is 87%. At 3.5A output, the efficiency is 90%.

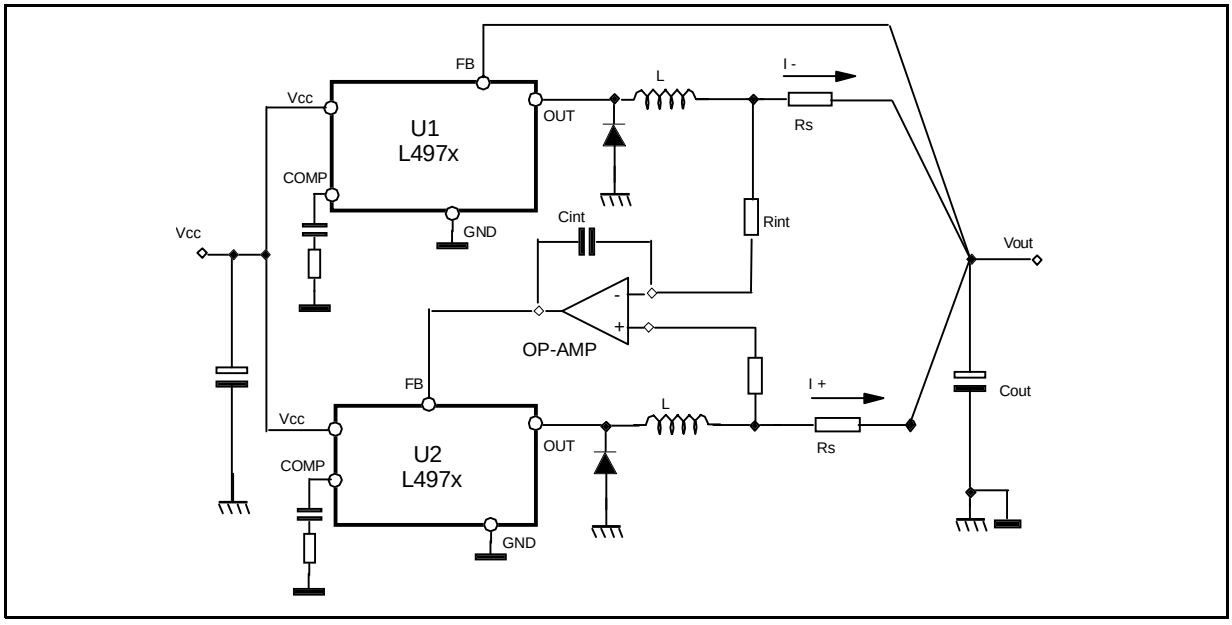
Electrical Specifications

Input Voltage range	8V-30V
Output Voltage	5.1V ±3% (Line, Load and Temperature)
Output Voltage Ripple	47mV (0.92%/Vo)
Output Current range	0 to 7A
Max Output Ripple current	15%
Min Iomax Current limit	8A
Switching frequency	200kHz

Current Sharing Operating Principle

The current sharing configuration, shown in fig. 1, is based upon two L497x devices U1 and U2. Any device in the L497x family can be used for this purpose.
The U1 regulator acts as a master which regulates the output voltage.
The second section U2 works as a current follower. Its task is to deliver an output current equal to the

Figure 1. Current Sharing Operating Principle



current delivered from the first section. An op-amp compares the voltage drop through Rs which is proportional to the current delivered from the U2 section with the voltage drop across Rs proportional to the current delivered from the U1 section. The Cin and Rin components introduce a pole and a zero in the current loop which allows integration of the error signal. The current loop regulates I^+ equal to I^- . As a result the output current delivered to the load is Iout = 2I- = 2I+ for every load condition.

Current Sharing Accuracy

The accuracy of the current sharing between the two sections depends on the op-amp offset voltage, Voff, and the value of Rs and its accuracy . The offset voltage introduce an error in the sensing voltage , Vs=Rs Iout/2 . The relative percentage current error due to the offset is given by :

$$e\% = (\Delta I/I) \cdot 100 = (Voffset \cdot 100) / (Rs \cdot Iout)$$

This error is minimum at maximum load. The larger the value of Rs, the smaller the error. Rs must be chosen as a compromise between error minimization and system efficiency.

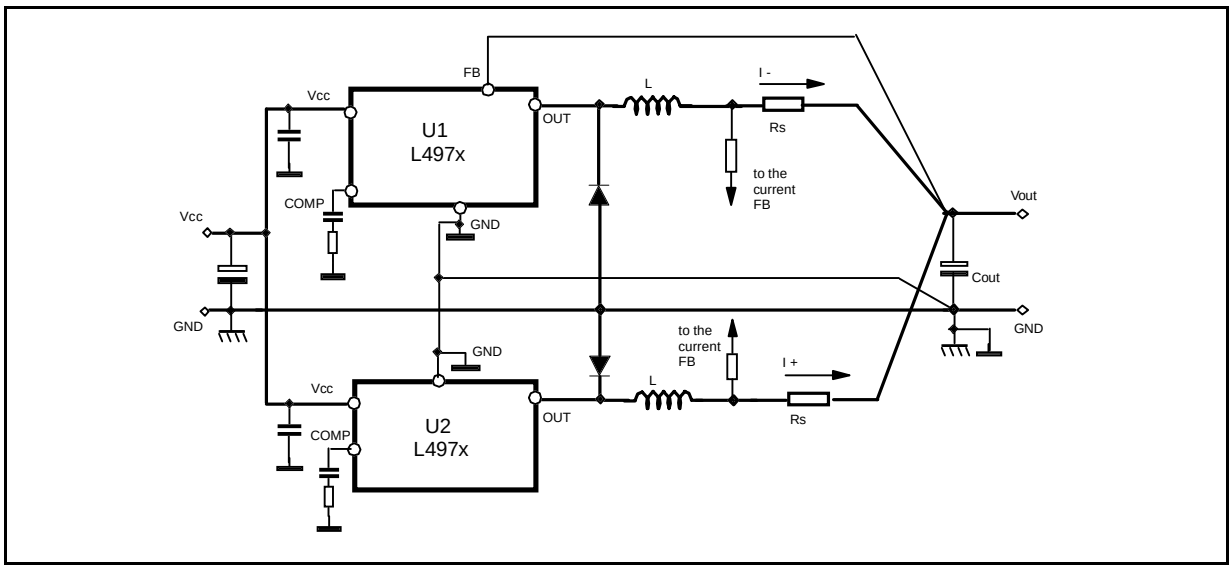
For example with Iout = 7A choosing Rs = 25mΩ ,considering a maximum offset voltage of 3mV (LM358A), the maximum relative percentage error is 1.7% (120mA @ Iout = 7A).

The total error is given by the sum of this error plus the error due to the sensing resistor (which corresponds to its accuracy of 1%). So the maximum error is 2.7% (190mA @Iout = 7A)

Layout Hints

The PCB layout requires some care. The power paths of the two sections must be as short and symmetrical as possible. The current sensing wires must be parallel and short to avoid induced noises. The sensing resistor must be non inductive. The ground pins of the two devices must be at the same voltage and connected to the output ground point.

Figure 2. Layout hints.



Syncronization or Multiphase

In a current sharing application the two sections can be synchronized. This permits a reduction of noise induced from one section to another. In this case a single RC network can be used for both the oscillators and the two SYNC pins are connected.

In many application, instead of synchronizing the two oscillator, it is useful to introduce a delay between the two PWM signals in order to achieve a multiphase application. The phase shift between the two PWM signals can be easily achieved by two methods :

Case 1) Programmable Phase Delay.

Fig. 3 shows how to program a phase delay with a monostable multivibrator whose on time is equal to the desired phase delay.

Case 2) Fixed Phase Delay.

Figure 3 shows a method of setting a delay time for the 2nd PWM section to be slightly larger than the ON-time of the 1st PWM section.

Figure 3. Case 1) Programmable Phase Delay.

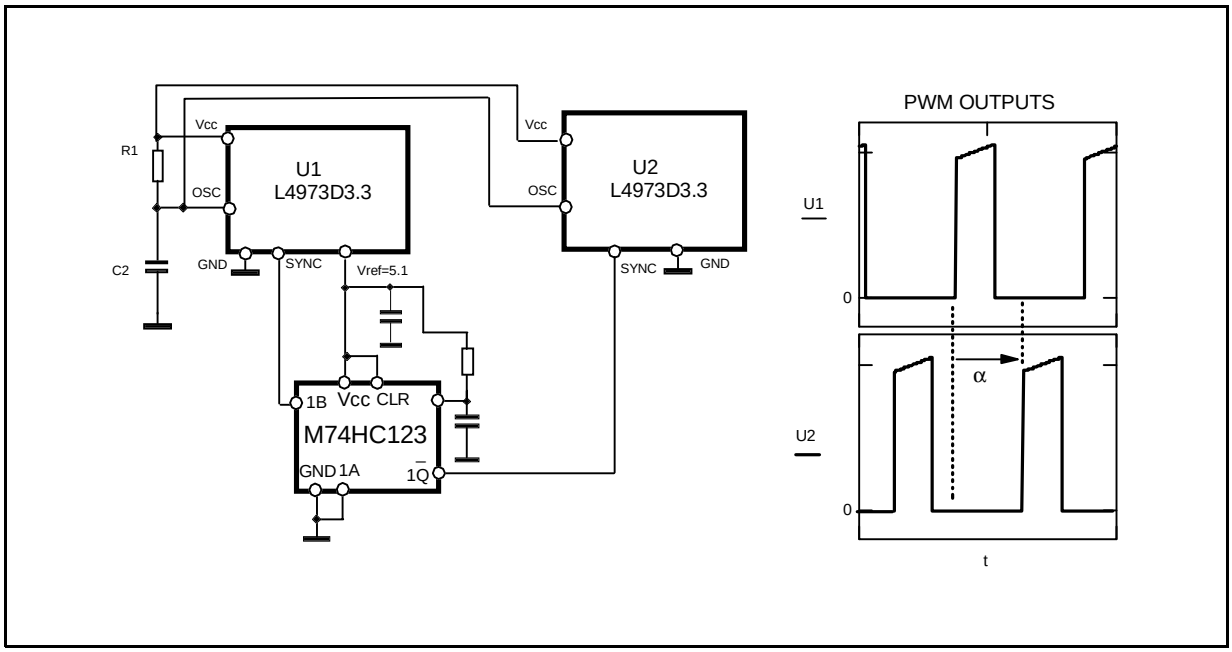
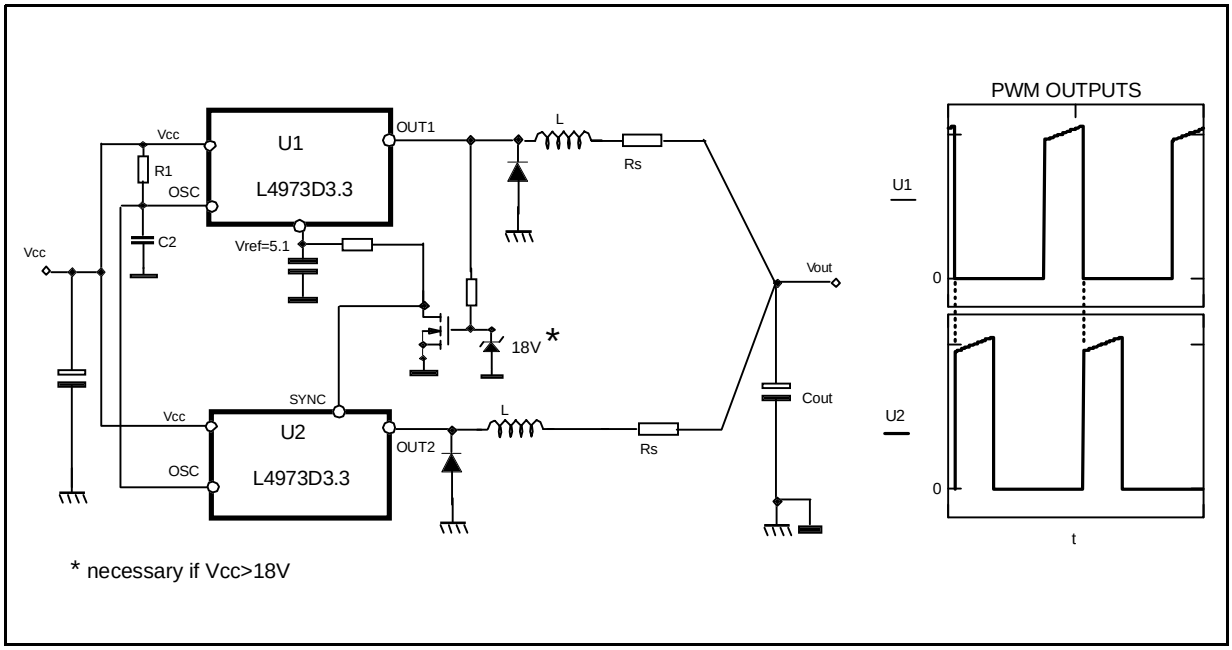


Figure 4. Case 2) Programmable Phase Delay.



Multiphase Benefits

The main benefits are :

- Minimization of the RMS current through the input capacitor therefore increasing of the efficiency and reducing of the capacitor cost and size.
- Minimization of ripple current through the output capacitor and ground path.
- Fast load transient response.
- Improved reliability /MTBF.

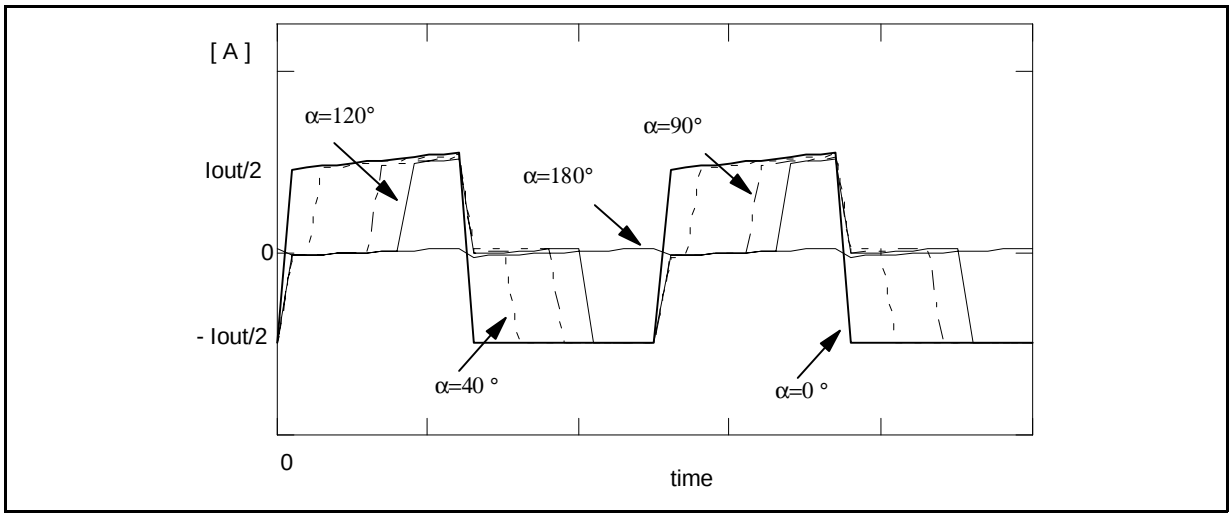
RMS current through the input capacitor are equivalent in Case 1) and Case 2). Even though the circuitry of Case 2) is simplifier than Case 1), Case 1) provides the opportunity to optimize this ripple current.

Minimization of the RMS Current Through the Input Capacitor.

In Case 1) , Figure 3 shows the RMS current through the input capacitor, referred to the output current (Iout), for various phase delays, α , of the two PWM sections. This assumes a duty cycle of 0.5 and a ripple current through the coil of 0.1· Iout.

For α equal to a half period (180 degrees of phase delay) the RMS current is approximately zero. If the two PWM signals are synchronized the RMS value is Irms = Iout/2. For example if Vout = 5V and Iout = 7A the Output Power is 35W. If the Input capacitor has an ESR of 100mOhm the phase delay allows a savings of 1.23W which corresponds to the 3.5% of the power delivered to the load.

Figure 5. RMS current through the input capacitor for a different phase delay, α , with a duty cycle of 0.5.



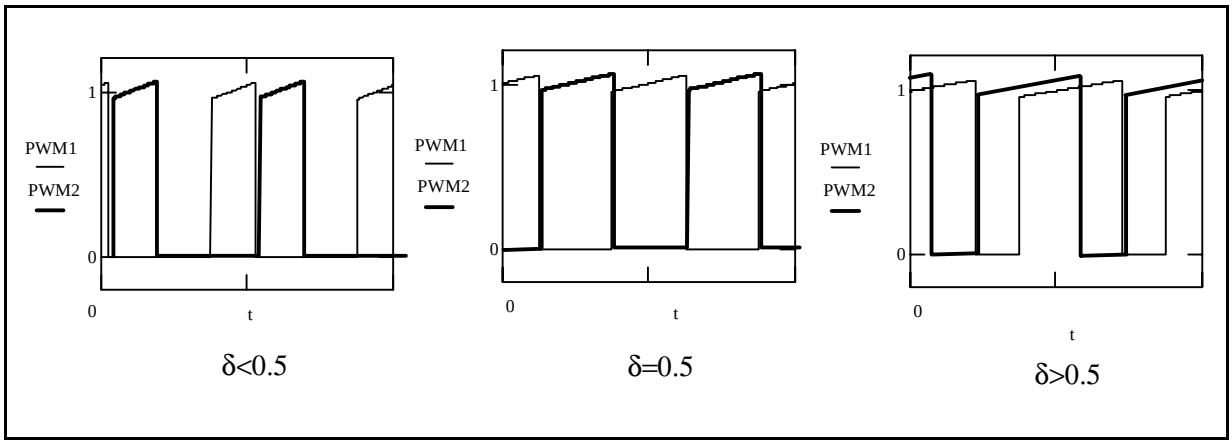
Assuming the same duty cycle for the two sections, the RMS Current through the input filter for different duty cycle, considering a phase delay of the second PWM signal equal to the Ton of the first section (Case 2)), is given approximately (the output current ripple can be negleted for this calculation) by the following formula:

$$I_{RMS}(\alpha) = \begin{cases} \sqrt{\left(\frac{Iout}{2}\cdot\sqrt{2\cdot\delta}\right)^2 - (Iout\cdot\delta)^2} & \text{if } \delta \le 0.5 \\ \sqrt{\left[\frac{Iout}{2}\cdot\sqrt{2\cdot(3\cdot\delta-1)}\right]^2 - (iout\cdot\delta)^2} & \text{if } \delta > 0.5 \end{cases} \qquad \text{Multiphase (1)}$$

where δ = duty cycle

Iout is the total output current equal to the sum of the individual output currents delivered from the two sections.

Figure 6. Input current of the two sections for different duty cycle.



If the PWM signals are synchronized without any delay, the RMS current through the input filter as a function of duty cycle is :

$$Irmssync(\delta) = \sqrt{(Iout \cdot \sqrt{\delta})^2 - (Iout \cdot \delta)^2} \qquad \text{synchronized} \quad (2)$$

Figure 7. RMS current through the input capacitor with synchronization and with multiphase.

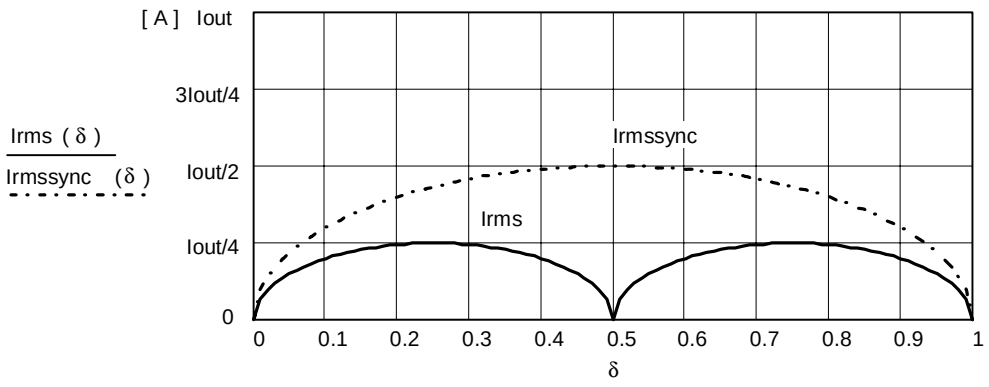


Figure 7 shows Equations (1) and (2) versus the duty cycle.

The maximum RMS current with synchronized PWMs is 1/2 of the total output current and it is obtained for $\delta = 0.5$.

In contrast, considering the multiphase PWM, **the RMS value is 0 with $\delta = 0.5$** and the max value of the RMS value is 1/4 of the total output current. **So the maximum RMS current with multiphased PWMs is a half of that syncronized PWMs.**

For every duty cycle condition the RMS current with multiphase application is lower than the case with synchronized PWMs and it is quite regular for different duty cycles.

It allows to optimize the input capacitor for the real working condition. In the synchronized case the input capacitor has to be dimensioned for the worst case of $\delta = 0.5$ that can be far from the real working conditions.

If Psync is the wasted power on the input capacitor with synchronized PWMs, given by :

$$Psync = ESR \cdot Irmssync^2$$

and Pmulti is the wasted power with multiphased PWMs, given by :

$$Pmulti = ESR \cdot Irms^2$$

the power saved using the multiphase instead of the synchronized method for various duty cycle is :

$$Psaved\ (\delta) = ESR \cdot (Irmssync^2\ (\delta) - Irms^2\ (\delta))$$

$$Psaved\ (\delta) = \begin{cases} \frac{ESR}{2} \cdot I_{out}{}^2 \cdot \delta & \text{if } \delta \leq 0.5 \\ \frac{ESR}{2} \cdot I_{out}{}^2 \cdot (1-\delta) & \text{if } \delta > 0.5 \end{cases}$$

For example considering an input capacitor ESR of 0.1 Ohm and an output current of 7A the power saved using the multiphase instead of the synchronized method for different duty cycle is shown in fig.8.

Figure 8. Power saved using the multiphase instead of the synchronized method for various duty cycle.

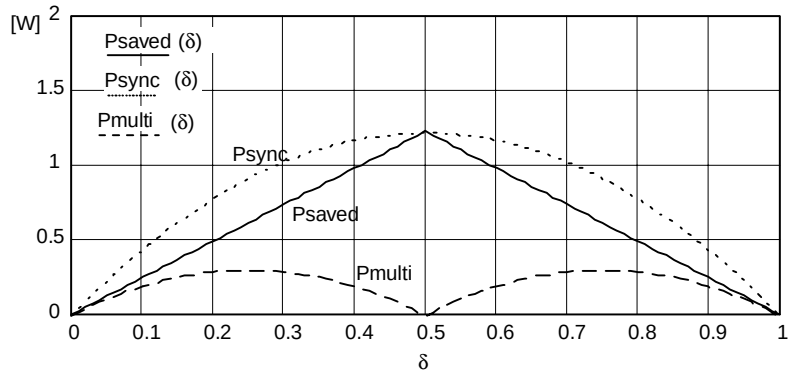


Figure 9. Power saved vs. Vout

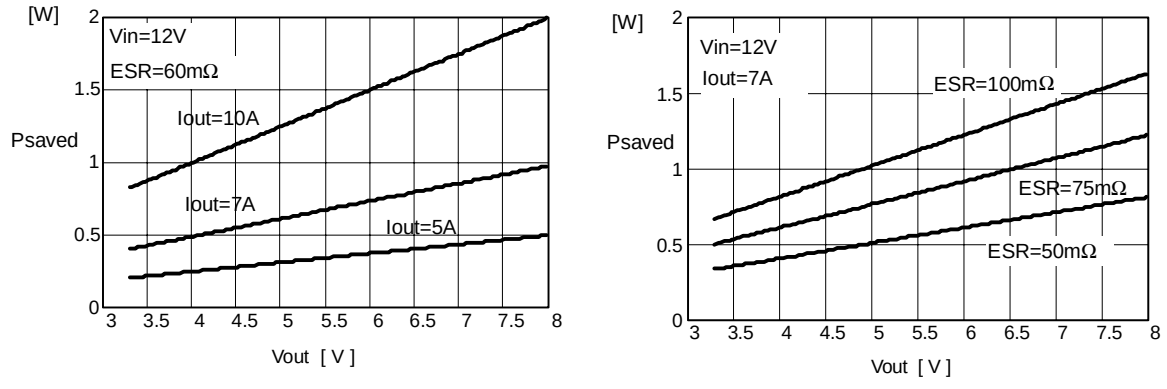
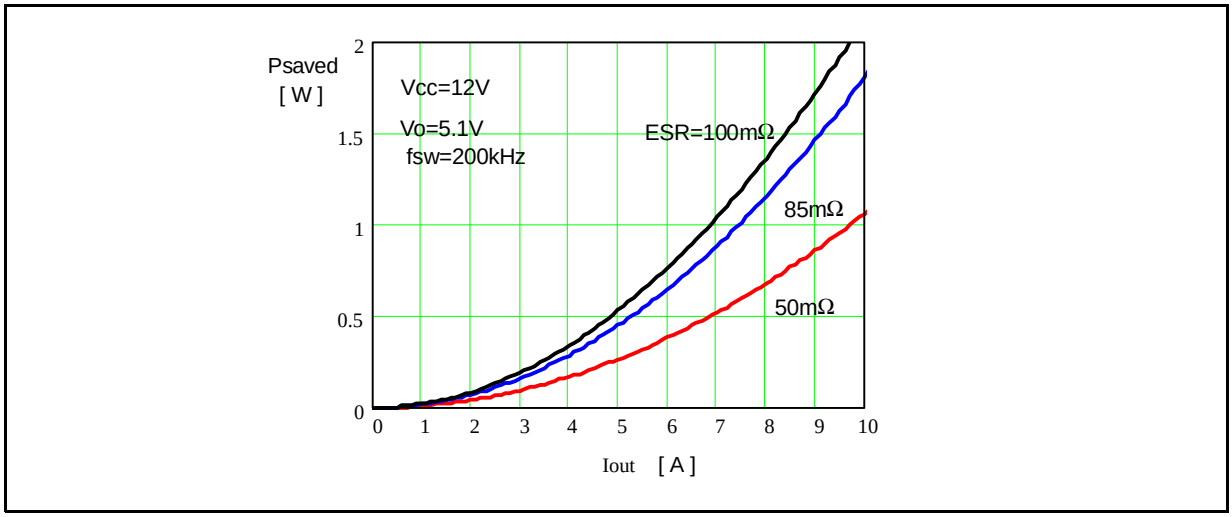


Figure 10. Power saved vs. Iout.



The gained power as a percentage of the output power using the multiphase PWMs instead of synchronized PWMs is :

$$\Delta P\%(\delta) = \frac{Psaved(\delta)}{Po} \cdot 100$$

$$\Delta P\%(\delta) = \frac{ESR}{2} \cdot \frac{Iout}{Vcc} \cdot 100$$

So the percentage gained power, ΔP%, for a fixed Iout, Vcc and ESR does not change with the output voltage.

For example if the input capacitor has an ESR of 100mOhm for a 12V/3.3V or 12V/5V power conversion, with Iout = 7A, there is in both cases a ΔP% gain of 3% .

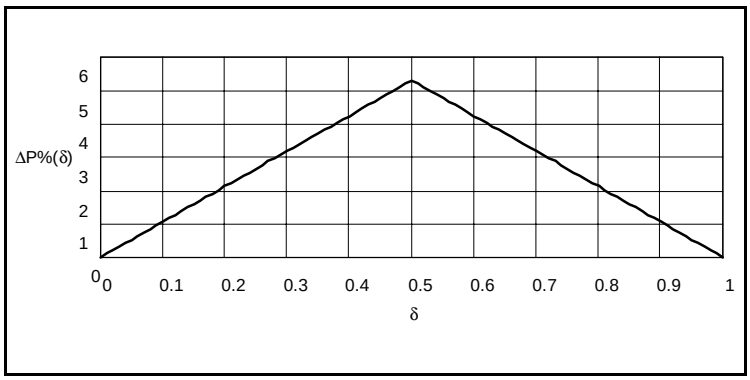
Table1 shows in details the major tips for different output voltages.

Table 1. Vcc = 12V , Iout = 7A, ESR=100mΩ.

Vo (V)	Irmssync (A)	Irmsmulti (A)	ΔIrms (A)	Psync (W)	Pmulti (W)	Psaved (W)	ΔP% Gained
3.3	3.13	1.74	1.39	0.98	0.3	0.68	3%
5.1	3.46	1.25	2.21	1.2	0.16	1.04	3%
6	3.5	0	3.5	1.23	0	1.23	3%

The gained power ΔP% versus duty cycle is shown in figure 10.

Figure 11. ΔP% vs. duty cycle.



The gained power ΔP% as a function of input voltage, output voltage, output current and input capacitor ESR is shown in figure 12.

Figure 12 shows the measured efficiency with the L4973D board , with Vin = 12V, Vout = 5.1V, fsw = 200kHz, using a input capacitor 470µF/50V ROE with an ESR = 85mΩ. Using the multiphase application with a phase delay, α, equal to half period, case1) , there is a gained efficiency of 2% compared to the synchronous application. So it is possible to maintain high efficiency values using low cost and size capacitor.

Figure 12. ΔP%

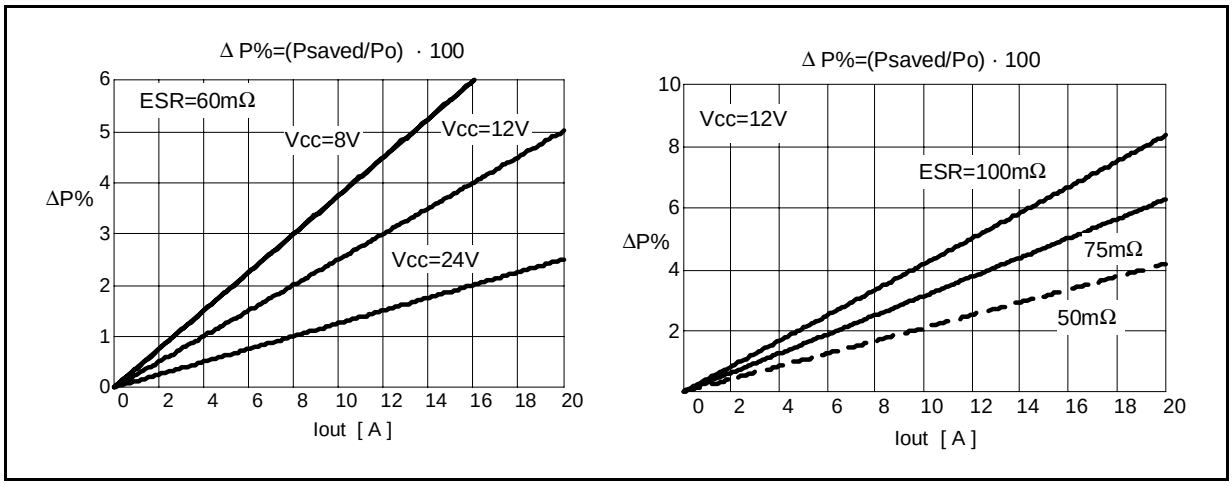
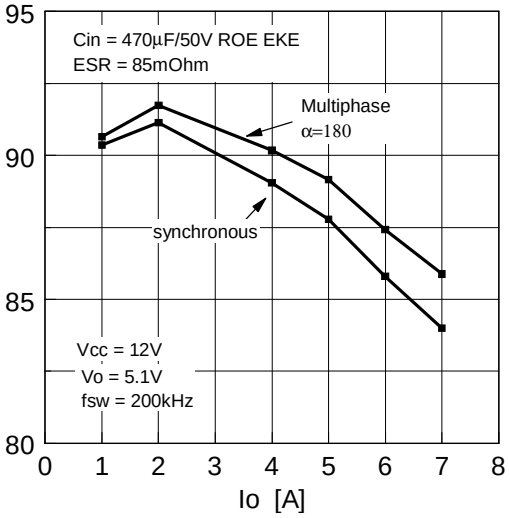


Figure 13. Efficiency vs. Output Current.

$$\eta = \frac{V_O \cdot I_O}{V_{IN} \cdot I_{IN}} \cdot 100 \quad [\%]$$



Conclusions

To sum up in application in which the duty cycle is between 0.2 and 0.8 there is a big advantage using the multiphase PWMs, in terms of dissipated power on the input capacitor compared with the added circuitry to achieve it. The more the output current is the more this advantage increases.

Applications with δ = 0.5, using a half period of multiphase phase delay, gives the best benefit because the RMS current through the input capacitor is approximately zero.

Minimization of the Ripple Current Through the Output Capacitor.

Figure 13 shows the current ripple through the output filter for different phase delay, α, of the two PWMs considering a duty cycle of 0.5.

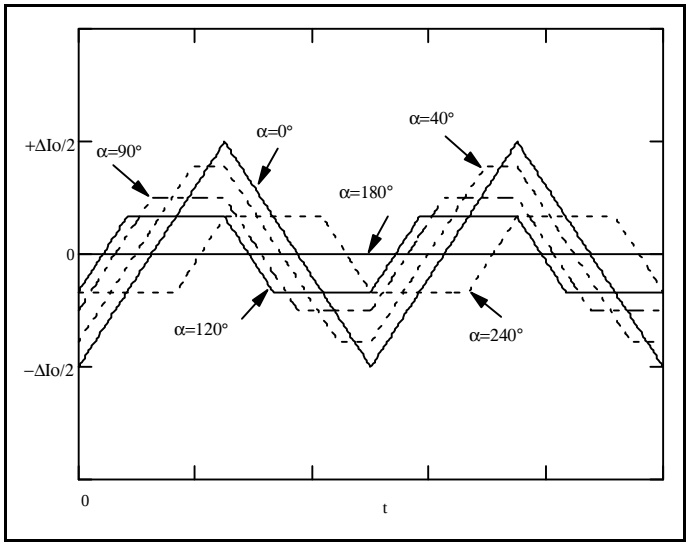
For α equal to half period (180 degrees of phase delay) the ripple current is approximately zero.

This allows to chose low cost output filtering capacitor. Or, with the same ESR, to reduce drastically the output voltage ripple.

The phase shift between the two PWM signals can be easily achieved in two way.

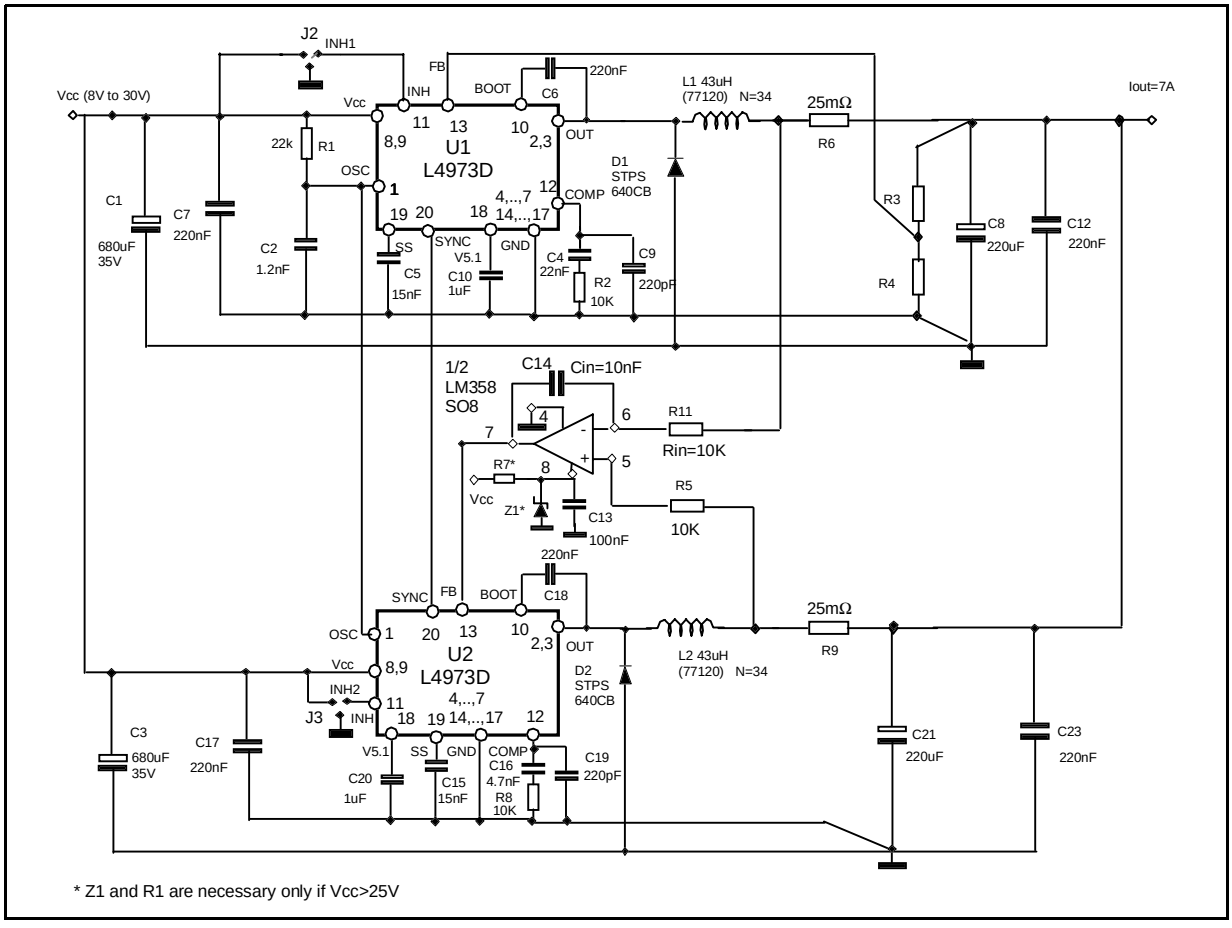
If the duty cycle is far from 0.5, the ripple current through the output capacitor is higher in Case 2 than in Case 1 in which the delay time can be programmed.

Figure 14. Ripple current through the output capacitor for different phase delay, α.



Current Sharing Evaluation Board for L4973D

Figure 15. Current sharing schematic diagram.



Electrical Specifications and Performance:

Input Voltage range	8V-30V
Output Voltage	5.1V ±3% (Line, Load and Temperature)
Output Voltage Ripple	47mV (0.92%/Vo)
Output Current range	0 to 7A
Max Output Ripple current	15%
Min Iomax Current limit	8A
Switching frequency	200kHz
Efficiency	87% @ 7A Vin = 24V

Figure 16. Board efficiency vs. output current.

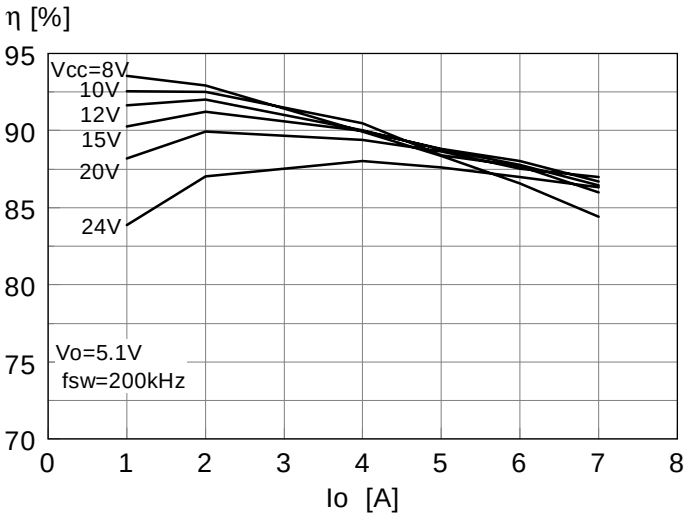


Table 2. Output voltage selection

L4973D3.3		
Vo (V)	**R3 (KΩ)**	**R4 (KΩ)**
3.3	0	4.7
5.1	2.7	4.7
L4973D5.1		
5.1	0	4.7

Main Components Description.

It follows a description of the chosen output and input capacitor and of the inductor for each of the two sections.

Input Capacitors

The input capacitors have to be able to support the maximum input operating voltage of the device and the maximum RMS input current.

At full load, Io = 7A and duty cycle of 50% the RMS current flowing through the input capacitors is maximum and is given by Io/2 . So the RMS current to be sustained is 3.5A.

The two selected capacitor, FA 680µF/50V Panasonic, are able to support this current.

Inductor Selection

The minimum duty cycle is:

$$Dmin = (Vo + Vf)/(Vin\ max + Vf) = 0.184$$

where Vf is the freewheeling diode forward voltage.

The inductor ripple current is fixed at 15% of Iomax and it is 0.525A.

The inductor needed for each of the two sections is:

$$L = \frac{(Vo + Vf) \cdot (1 - D_{min})}{\Delta I_o \cdot f_{sw}} = 43\mu H$$

The $L \cdot Io^2$ is 0.533 and the size core chose is 77120 (125µ) Magnetics KoolMµ material. In order to compensate a 40% reduction of inductance at full load due to the DC current level, it is necessary to wire 34 turns, which correspond to 84µH of inductance at light load.

With this choice the core losses are approximately 280mW. The temperature increasing of the core is 12°C approximately.

Output Capacitor

The selection of Cout is driven by the output ripple voltage required, 1% of Vo. This is defined by the ESR of the output capacitance and by the maximum ripple current (0.525A).

The maximum ESR is:

$$ESR = \Delta Vo/\Delta Io = 0.051/0.525 = 97m\Omega$$

The selected capacitance is 220µF/35V FA Panasonic with ESR = 90mW and the ripple voltage is 0.92% of Vo (47mV).

Bill of Material

C1, C3	680µF / 35V FA PANASONIC 16x15 Irms=1690mA
C2	1.2nF/35V SMD 1206
C4	22nF SMD 1206
C16	4.7nF SMD 1206
C13	100nF/35V SMD 1206
C5,C15	15nF/35V SMD 1206
C6,C7,C12,C17,C18,C23	220nF/50V SMD 10% Kemet 1206 X7R
C8,C21	220µF/35V FA PANASONIC 8x15
C10,C20	1µF/10V electrolitic (not SMD)
C11,C22	not used
C14	10nF/35V SMD 1206
C9,C19	220pF SMD 1206
U1,U2	L4973D3.3
R1	22k SMD 1% 1206, 0.25W
R2	9.1k SMD 1% 1206, 0.25W
R3,R10	2.7k SMD 1% 1206, 0.25W
R4,R12	4.7k SMD 1% 1206, 0.25W
R6,R9	0.025 Ohm 1W 1% DALE WSL-2512
R7	0 SMD 1206
R11,R5,R8	10K SMD 1% 1206, 0.25W
D1	STPS640CB (DPAK)
D2	STPS640CB (DPAK)
U3	LM358 SO8 ST
Z1	Diodo Zener 25V SOT23
L1,L2	43µH KoolMu Magnetics core 77120 34 Turns d(mm)=0.91 AWG19

Stability Analysis of the Current Loop.

In the current sharing configuration the U1 regulator acts as a master in order to regulate the output voltage. The second section U2 works as current follower. Its task is to deliver an output current equal to the current delivered from the first section. For the analysis of the stability, see Fig. 21, the current loop of the U2 section can be considered as a separated loop from the voltage loop of the U1 section, considering that the current loop is quite faster than the voltage one.

For the stability of the voltage loop see the AN938.

The open loop transfer functions is composed of the following blocks :

- Error amplifier and compensation block :

$$A_{(s)} = \frac{A_{vo} \cdot (1 + s \cdot R_c \cdot C_c)}{s^2 \cdot R_o \cdot C_o \cdot R_c \cdot C_c + s \cdot (R_o \cdot C_c + R_o \cdot C_o + R_c \cdot C_c) + 1}$$

in which Ro = 1.2MΩ and Co = 220pF are internal capacitance and resistance of the Error Amplifier while R_c and C_c are the compensation values.

Figure 17. Error Amplifier Compensation Circuit

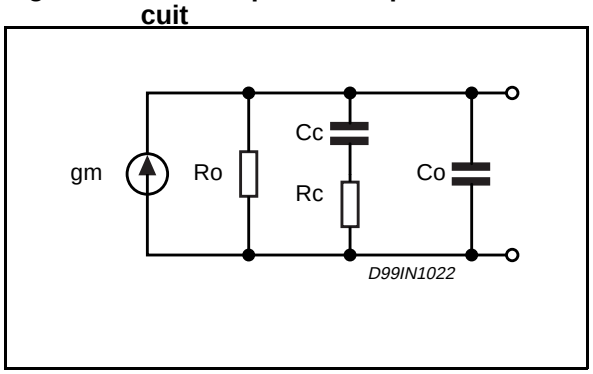
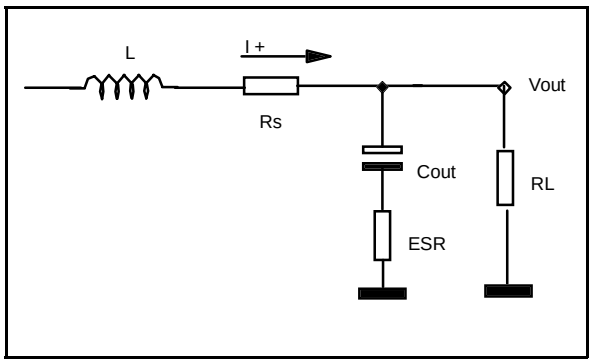


Figure 18. Output filter



- Output LC filter:

$$Gfil(s) = \frac{1}{RL + Rs} \cdot \frac{s \cdot Cout \cdot (RL + ESR) + 1}{s^2 \cdot Cout \cdot \frac{(ESR + RL) \cdot L}{RL + Rs} + s \cdot \left[\frac{Cout \cdot Rs \cdot (RL + ESR) + L + RL \cdot ESR \cdot Cout}{RL + Rs}\right] + 1}$$

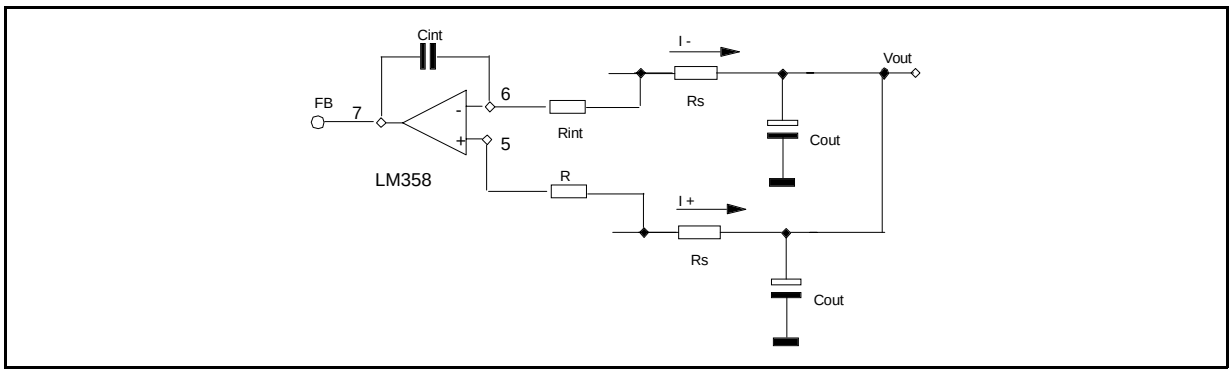
Rs is the sensing resistor, RL is the load resistance.

PWM gain:

$$Gpwm = Vcc/Vct = \frac{Vcc \cdot 6}{Vcc - 1} \approx 6$$

where Vct is the peak to peak saw tooth oscillator.

Figure 19. Current feedback.



The LM358 configured as an integrator introduces a gain given by Rs , a pole in Gint(s) and a zero in Z(s) :

$$Vfb = (Rs / s \cdot Cint \cdot Rint)[(I^{+}) \cdot (1 + s \cdot Cint \cdot Rint) - (I^{-})]$$

Assuming :

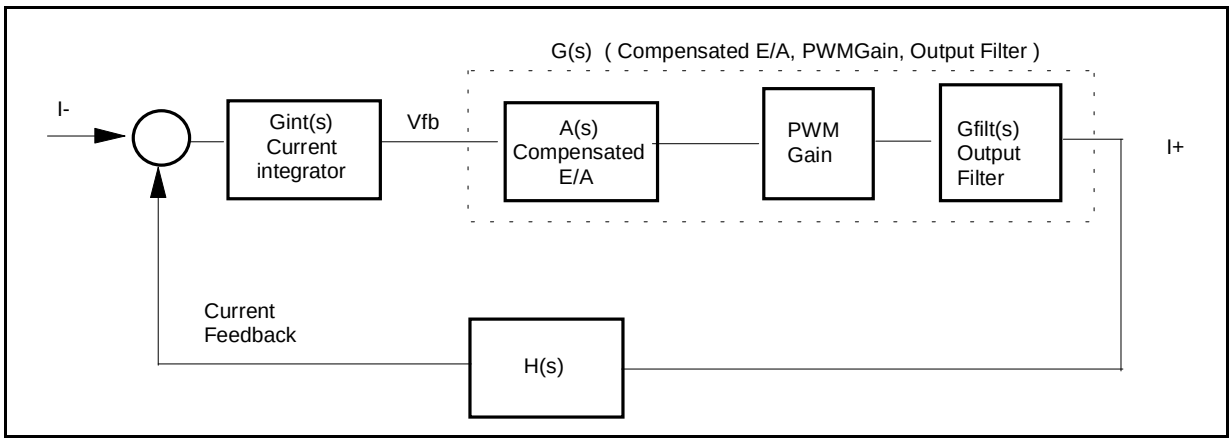
$$Gint(s) = Rs \cdot \frac{1}{s \cdot Rint \cdot Cint}$$

and :

$$H(s) = (1 + s \cdot Rint \cdot Cint)$$

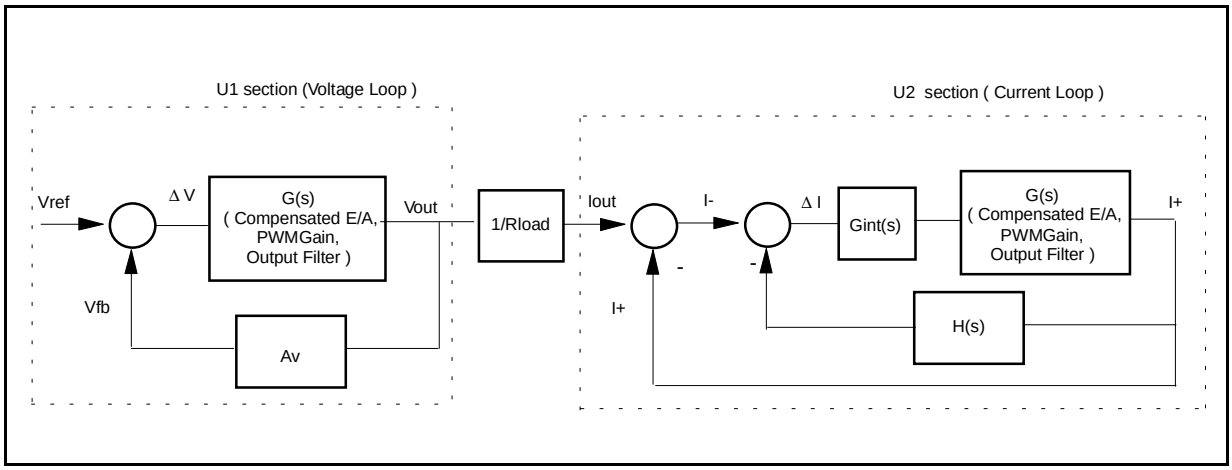
the current control loop block diagram can be considered as shown in Figure 20.

Figure 20. Block diagram of the current loop



The complete block diagram of the current sharing loop is shown is figure 21.

Figure 21. Complete block diagram of the current sharing loop



The open loop function of the current loop is given by :

$$F(s) := GpwmZint(s) \cdot Gfil(s) \cdot A(s)$$

In figures 22 and 23 are shown the open loop Gain and Phase Bode plot . The capacitor C5 does not influence the system stability but is useful only to reduce the noise. The cut off frequency and a phase margin are: Fc = 8KHz; Angle = 40°

Figure 22. Gain Bode open loop plot.

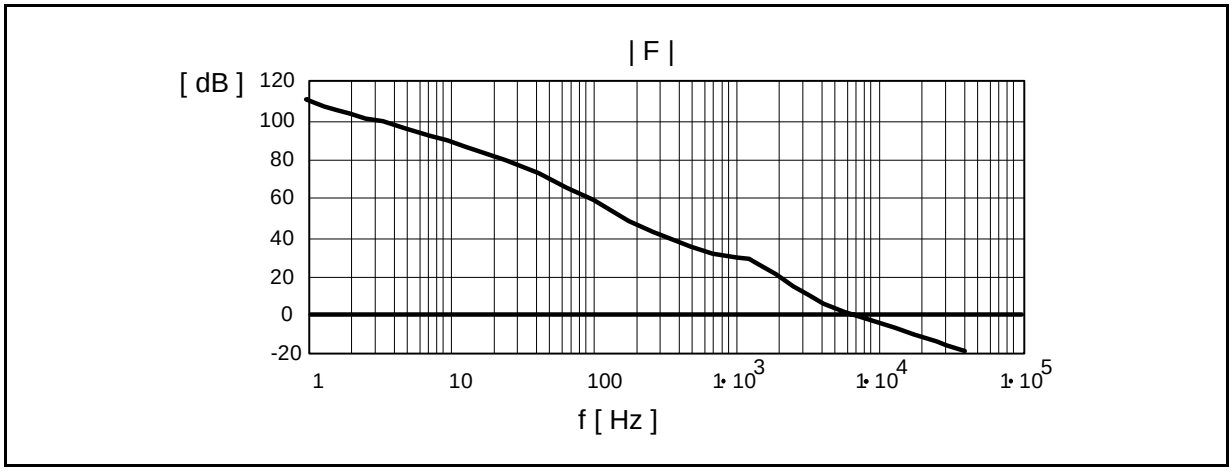


Figure 23. Phase Bode open loop plot.

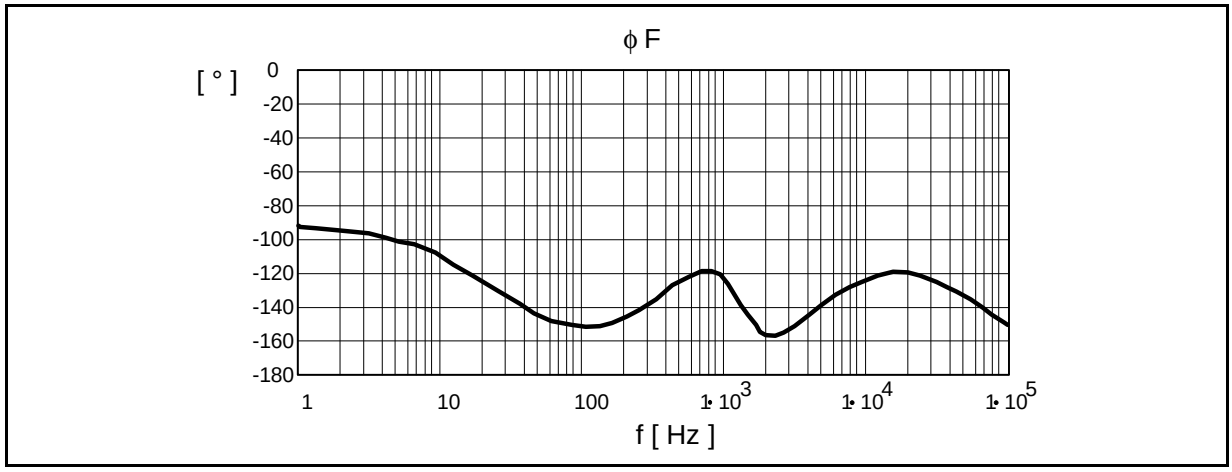
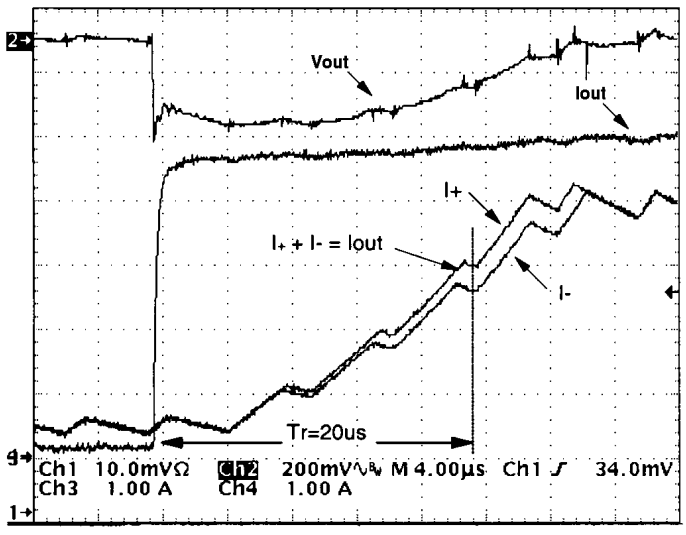


Figure 24. Load transient response.



Load Transient Response

Figure 24 shows the load transient behavior of the schematic circuit of Figure 15.

In Figure 24 are shown the current deliveder from the two sections, the load current and the drop voltage on the output . After 20µs the total current delivered from the two section is equal to the current required from the load. So the response time of the application is 20µs approximately for a load transient from 1A to 6A.

TEST CONDITIONS (fig 24):

Vin = 5V, Vout = 3.3V, Load transient form 1A to 6A, dIout/dt = 20A/µs.

Figure 25. PCB Layout top view: Silk, component side and bottom layer (1:1.25 scale).