9/28/04

Errata: CS42416 Rev. C

(Reference CS42416 data sheet revision DS602A2)

*All references to the CS42416 mentioned below shall be taken to refer to revision C of the CS42416 product. The hardware revision code can be found in the 12-character field printed on the last line below the part number of each chip. The letter that appears as the eighth character from the right is the revision code (e.g. YFTA**C**XAL0311 is a Revision C part).*

- Upon disabling the PDN bit, the ADC will startup in one of two modes that affect dynamic range. In one mode the ADC's dynamic range will meet data sheet specification while in the other, the ADC's dynamic range will exhibit a degradation by approximately 4 dB. Which mode the ADC will enter upon the release of PDN is indeterminate.
- When using the PLL loop filter components listed in the CS42416 data sheet, the PLL may take a long time to lock at low sample rates. Use of the following PLL components will ensure quick acquisition of lock at all specified sample rates.
  - Rfilt = 2.55 kΩ
  - Cfilt = 0.047 μF
  - Crip = 2200 pF

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