20MHz ~ 170MHz FSPLL PLL2013X

General Description

The PLL2013X is a Phase-Locked Loop (PLL) frequency synthesizer constructed in CMOS on single monolithic structure. The PLL macro-functions provide frequency multiplication capabilities.
The output clock frequency Fout is related to the input clock frequency Fin(XTALIN) by the following equation:

$$Fout=(m*Fin)/(p*2^{s})$$

Where, Fout is the output clock frequency.
Fin is the input clock frequency.
m,p and s are the values for programmable dividers.
PLL2013X consists of a phase/Frequency Detector(PFD), a Charge Pump an External Loop Filter, a Voltage Controlled Oscillator(VCO), a 6bit Pre-divider, an 8bit Main divider and 2bit Post Scaler as shown inFigure1.

Features

- **0.25mm CMOS device technology**
- **2.5 Volt single power supply**
- **Output frequency range: 20 ~ 170 MHz**
- **Jitter ±150ps at 170MHz**
- **Duty ratio 45% to 55%(All tuned range)**
- **Frequency changed by programmable divider**
- **Provision for 14.318Mhz crystal oscillator buffer - OPTION**
- **Power down mode**

IMPORTANT NOTICE
- Please contact SEC application engineer to confirm the proper selection of M,P,S value.

FUNCTIONAL BLOCK DIAGRAM

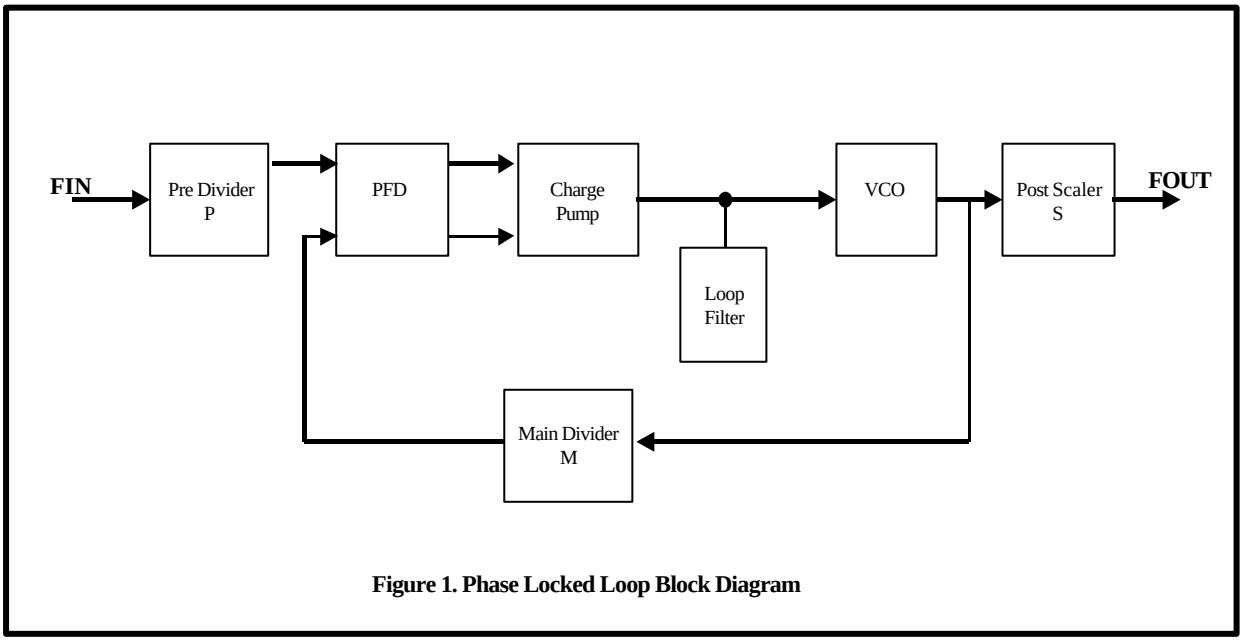


Figure 1. Phase Locked Loop Block Diagram

NOTE

- **Xtal oscillator is OPTIONAL block.**
  If customer concerns about this block - xtal buffer or lock detector, refer to next chapter.

Ver 2.3 (DEC. 1999)

CORE PIN DESCRIPTION

NAME	I/O TYPE	I/O PAD	PIN DESCRIPTION
VDD25A2	DP	vdd2t_abb	Digital power supply
VSS25A2	DG	vss2t_abb	Digital ground
VDD25A1	AP	vdd2t_abb	Analog power supply
VSS25A1	AG	vss2t_abb	Analog ground
VBBA	AB/DB	vbb_abb	Analog / Digital sub bias
FIN	DI	picc_abb	Reference Frequency Input
FILTER	AO	poar50_abb	. Pump out is connected to Filter . A capacitor is connected between the pin and analog ground
FOUT	DO	pot8_abb	20MHz~170MHz clock output
PWRDN	DI	picc_abb	FSPLL clock power down. -When PWRDN is High, PLL do not operate. -If Customer don't use this pin, Apply to VSS.
P[5:0]	DI	picc_abb	The values for 6bit programmable pre-divider.
M[7:0]	DI	picc_abb	The values for 8bit programmable main divider.
S[1:0]	DI	picc_abb	The values for 2bit programmable post scaler.

I/O TYPE ABBR.

- AI : Analog Input
- DI : Digital Input
- AO : Analog Output
- DO : Analog Output

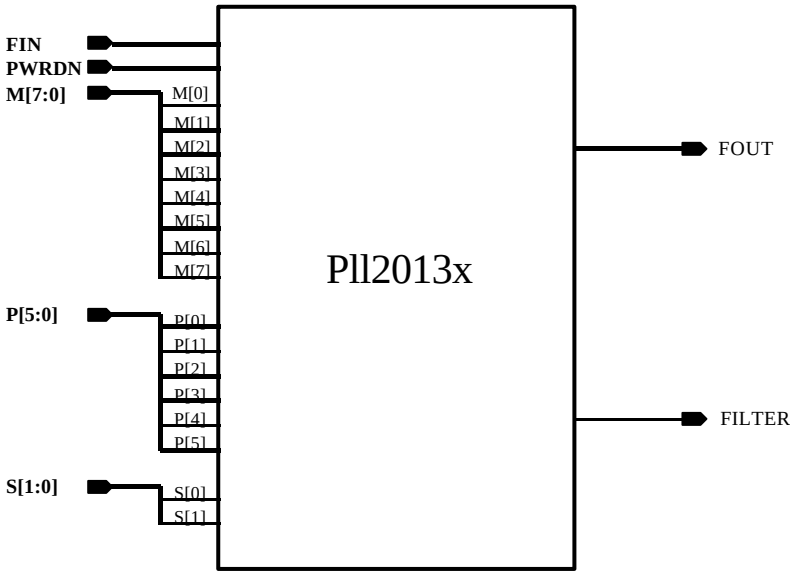
- AP : Analog Power
- AG : Analog Ground
- AB : Analog Sub Bias
- DP : Digital Power
- DG : Digital Ground
- DB : Digital Sub Vias

- BD : Bidirectional Port

NOTE

- SEC recommends customers to use power cell type - vdd2t_abb, vss2t_abb. When using the recommended power cells, customers must use slot cells for separating digital and analog power.
- Please contact SEC when customers can not use the recommended power cells or customer is to arrange this I/O cells in product..

CORE CONFIGURATION



Recommended Operating Conditions

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage Differential	VDD25A2-VDD25A1	-0.1		+0.1	V
Oscillator Frequency	Fosc		14.318		MHz
External Loop Filter Capacitance	LF		820		pF
Operating Temperature	Topr	0		70	°C

NOTES

1. It is strongly recommended that all the supply pins (VDD25A1, VDD25A2) be powered to the same supply voltage to avoid power latch-up.

DC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Operating Voltage	VDD25A2/VDD25A1	2.375	2.5	2.625	V
Digital Input Voltage High	V_{IH}	1.9			V
Digital Input Voltage Low	V_{IL}			0.5	V
Dynamic Current	I_{dd}			3	mA
Power Down Current	I_{pd}			10	uA

AC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Crystal frequency	F_{XTAL}		14.318		MHz
Input Frequency	F_{IN}	3		40	MHz
Output Clock Frequency	F_{OUT}	20		170	MHz
Input Clock Duty Cycle	T_{ID}	40		60	%
Output Clock Duty Cycle (at 170MHz)	T_{OD}	45		55	%
Input Glitch Pulse Width	T_{IGP}	1			ns
Locking Time	T_{LT}			150	us
Jitter,Cycle to Cycle	T_{JCC}	-150		+150	ps

NOTES

1. It is strongly recommended that input signal is not generated glitch, but if consumer cannot help generating glitch, Consumer must carefully considerate the specification.

Functional Description

A PLL is the circuit synchronizing an output signal (generated by an VCO) with a reference or input signal in frequency as well as in phase.

In this application, it includes the following basic blocks.

. The voltage-controlled oscillator to generate the output frequency
. The divider P devides the input frequency by p
. The divider M devides the VCO output frequency by m
. The divider S divides the VCO output frequency by s
. The phase frequency detector detects the phase difference between the reference frequency and the output frequency (after division) and controls the charge pump voltage.
. The loop filter removes high frequency components in charge pump voltage and does smooth and clean control of VCO

The m, p, s values can be programmed by **16bit digital data** from the external source. So the PLL can be locked in the desired frequency.

Fout = m * Fin / p*s

Fin = 14.318MHz, m=M+8 , p=P+2, s=2^S
Digital data format:

Main Divider	Pre Divider	Post Scaler
M7,M6,M5,M4,M3,M2,M1,M0	P5,P4,P3,P2,P1,P0	S1,S0

NOTES
. S[1] - S[0] : Output Frequency Scaler
. M[7] - M[0] : VCO Frequency Divider
. P[5] - P[0] : Reference Frequency Input Divider

OUTPUT FREQUENCY EQUATION & TABLE

Frequency Equation: $$F_{OUT} = \frac{(M+8)}{(P+2) \times 2^{s}} \times F_{IN}$$

Table 1. Example of Divider Ratio

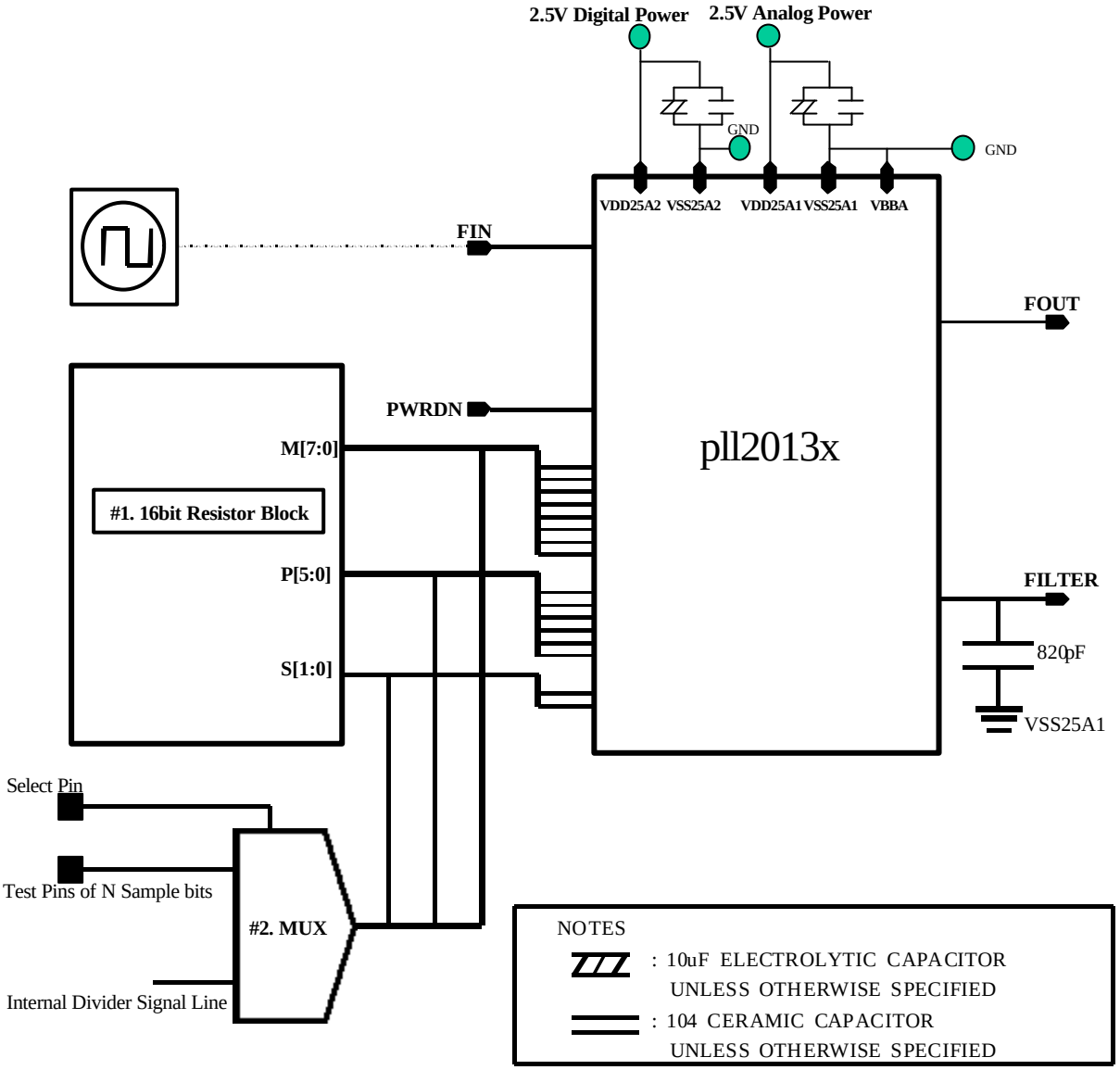
M7	M6	M5	M4	M3	M2	M1	M0	M	m (M+8)	P5	P4	P3	P2	P1	P0	P	p (P+2)	S1	S0	2^S
0	1	0	1	0	1	0	1	85	93	1	0	1	0	1	0	42	44	0	0	1

IMPORTANT NOTICE
- Please contact SEC application engineer to confirm the proper selection of M,P,S value.

CORE EVALUATION GUIDE

For the embedded PLL, we must consider the test circuits for the embedded PLL core in multiple applications. Hence the following requirements should be satisfied.

- The FILTER and FOUT pins must be bypassed for external test.
- For PLL test (Below 2 examples),
  it is needed to control the dividers - M[7:0],P[5:0] and S[1:0] -that generate multiple clocks.
  #1. Registers can be used for easy control of divider values.
  #2. N sample bits of 16-bit divider pins can be bypassed for test using MUX.



CORE LAYOUT GUIDE

- The digital power(VDD25A2,VSS25A2) and the analog power(VDD25A1,VSS25A1) must be dedicated to PLL only and seperated. If the dedicated VDD25A2 and VSS25A2 is not allowed that of the least power consuming block is shared with the PLL.
- The poar50_abb pad is used as a FILTER pad that contains only ESD production diodes with 50Ohm resistors.
- The FOUT and FILTER pins must be placed far from the internal signals in order to avoid overlapping signal lines.
- The blocks having a large digital switching current must be located away from the PLL core.
- For the FOUT pad, you can use a custom drive buffer or pot8_abb buffer considering the drive current.

OPTIONAL BLOCK USERS GUIDE

— There are crystal driver cell options for the PLL2013X core.

1. If the crystal component not used , an external clock source is applied to the FIN
   – If the crystal component not used , an external clock I/O Buffer offered from Samsung's STD110 library is recommanded for use
   – When implementing an embedded PLL block, the following pins must be bypassed externally for testing the PLL locking function:
     • Without Xtal-driver : FIN,FILTER,FOUT,VDD25A1,VSS25A1,VDD25A2 and VSS25A2,VBBA.
2. If the crystal componet and the Lock detector used, please contact an SEC application engineer
   – When implementing an embedded PLL block, the following pins must be bypassed externally for testing the PLL locking function:
     • With Xtal-driver : XTALIN,XTALOUT,LDOUT,FILTER,FOUT,VDD25A1,VSS25A1,VDD25A2 and VSS25A2,VBBA

Figure2. The example of PLL block without crystal component and Lock Detector

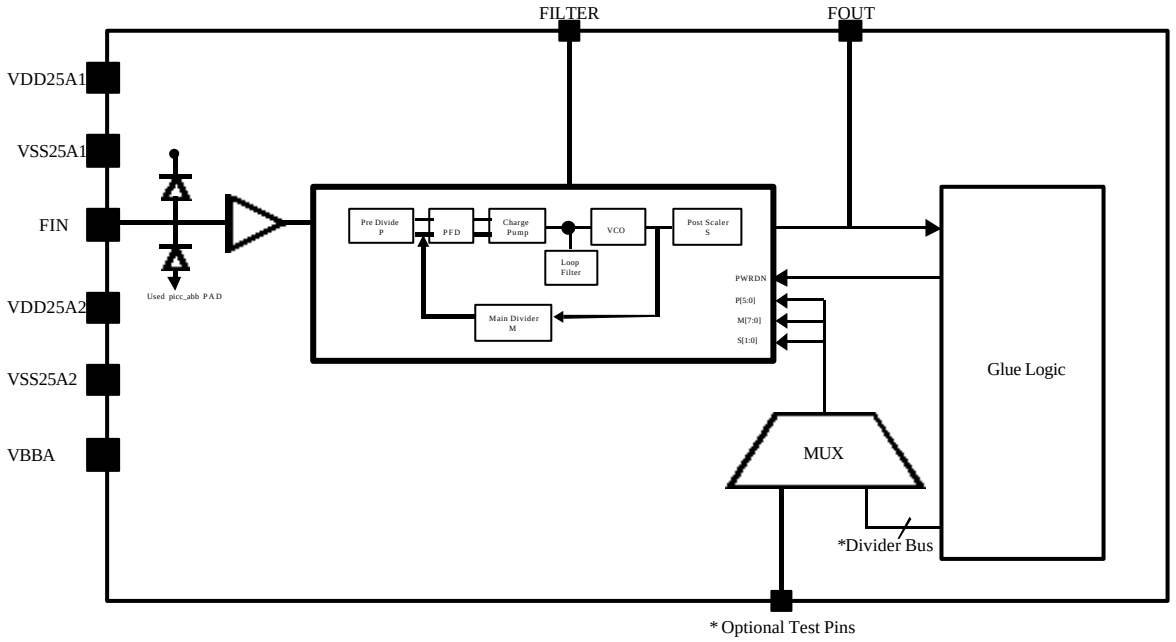
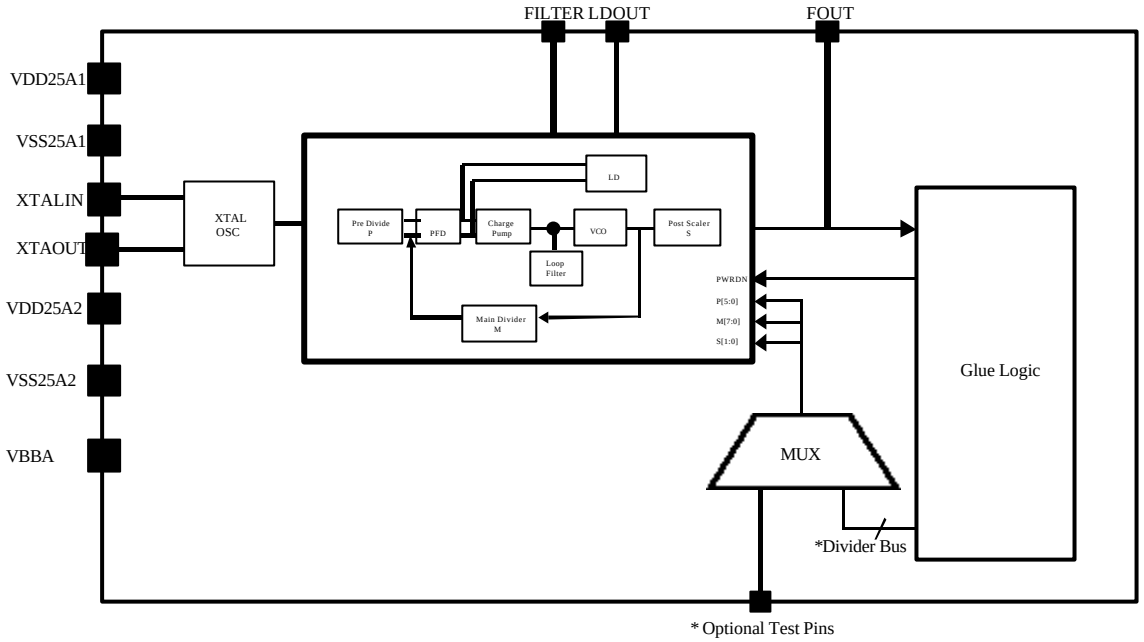


Figure3. The example of PLL block with dedicated XTAL-OSC and Lock Detector



XTAL Buffer Cell

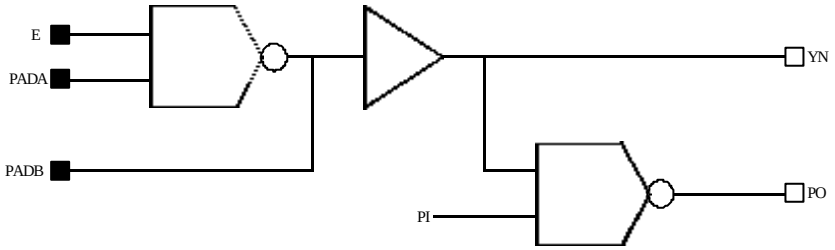


Figure4. Xtal buffer cell Symbol

- A XTAL Buffer cell for PLL is supported MDL110 databook of SEC
- The XTAL must be located between PADA and PADB.
  Enable pin(E) must be HIGH in normal operation.
- PI pin must be connected to VDD25A2 and the PO pin floated.

Lock Detector

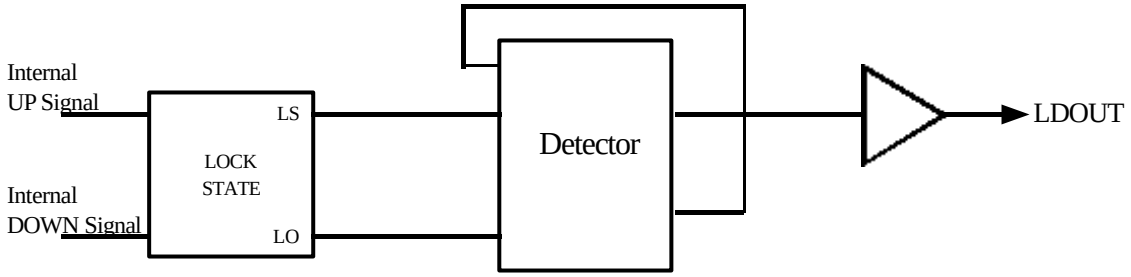


Figure5. Lock Detector Block

The built-in Lock Detector circuit will only work, When it is used in conjunction with PFD block output up/down signal. (Figure5).

We represent the output of lock detector in the timing diagram. (Figure6)

- Unlock State : LOW
- Lock State : HIGH

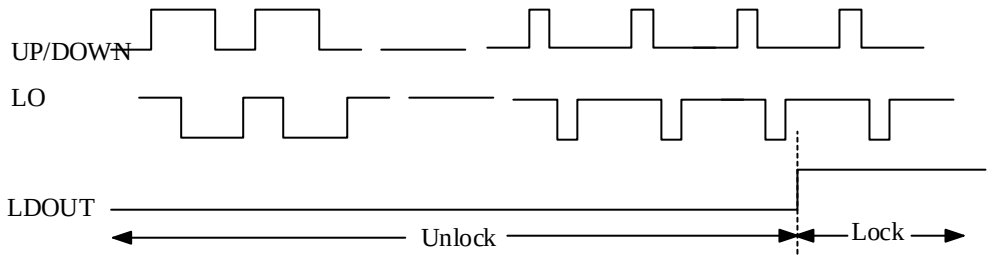
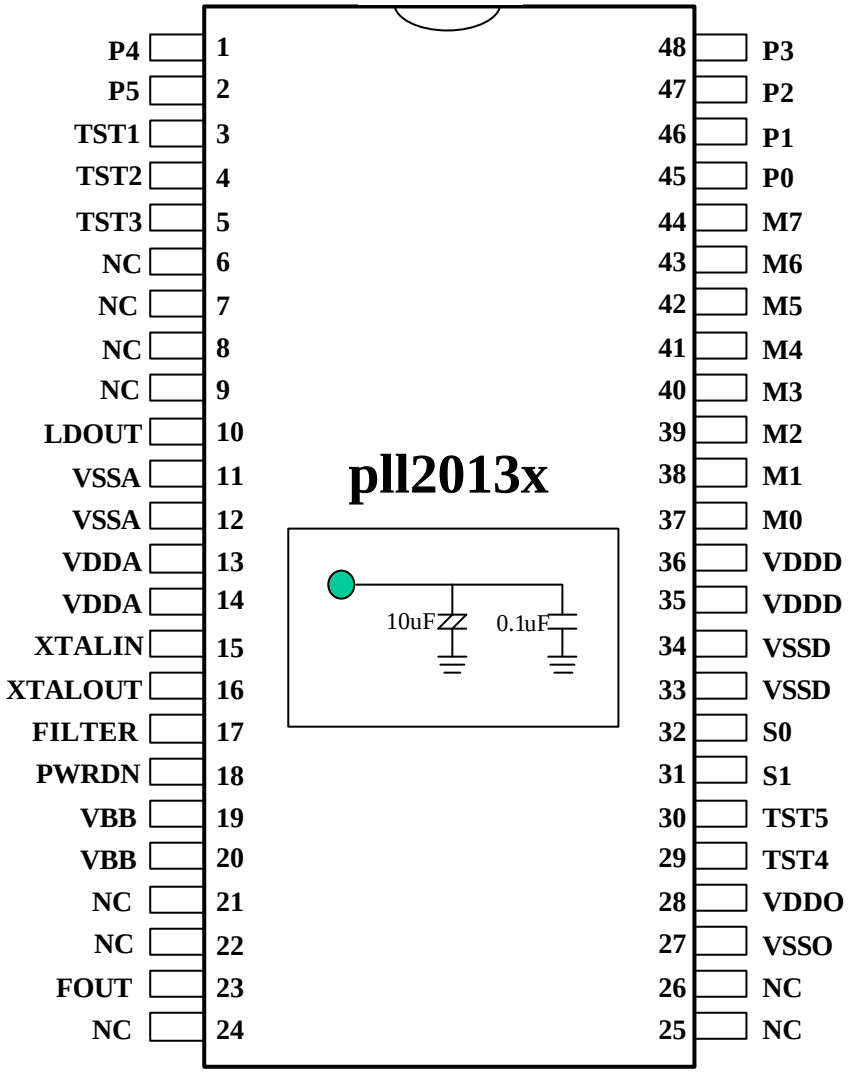


Figure6. Lock Detector Timing Diagram

PACKAGE CONFIGURATION



NOTES

*** NC is No connection pin**

PACKAGE PIN DESCRIPTION

NAME	PIN NO	I/O TYPE	PIN DESCRIPTION
VDDD	35,36	DP	Digital power supply
VSSD	33,34	DG	Digital ground
VBB	19,20	AB/DB	Analog / Digital Sub Bias
PWRDN	18	DI	FSPLL clock power down -PWRDN is High, PLL do not operating under this condition. - If isn't used this pin, tied to VSSD.
P[0]~P[5]	45~48,1,2	DI	Pre-Divider Input
VDDA	13,14	AP	Analog power supply
VSSA	11,12	AG	Analog ground
XTALIN	15	AI	Xtal external input, Load Cap : 25pF If Customer don't use the Xtal, use this pin to Input Port.
XTALOUT	16	AO	Xtal external output, Load Cap. : 25pF If Customer don't use the Xtal, Float this pin.
FOUT	23	DO	20MHZ~170MHz clock output
LDOUT	10	DO	Lock detector output
FILTER	17	AO	Pump out is connected to the FILTER. A 820pF Capacitor is connected between the filter pin and analog ground pin.
S[0]~S[1]	32,31	DI	Post scaler input
M[0]~M[7]	37~44	DI	8bit main divider input
TST1, TST3	3,5	DI	Test Pin, Apply to Analog vdda.
TST2,TST4,TST5	4,29,30	DI	Test Pin, Apply to Ground
VDDO	28	PP	I/O PAD Power
VSSO	27	PG	I/O PAD Ground

NOTES

1. I/O TYPE PP and PG denote PAD power and PAD ground respectively.
2. XTALIN, XTALOUT ,LDOUT is test pin for PLL in SEC

PLL Components

Figure1 is block diagram of the components of a PLL: phase frequency detector, chrge pump, voltage controlled oscillator, and loop filter.
In SEC technology, the loop filter is implemented as external components close to chip.

Phase detector : The phase dectector monitors the phase dfference between the Fref and Fvco,and generates a control signal when it detects difference between the two.
If the Fref frequency is higher than the Fvco frequency, its falling edge occures before(lead) the falling edge of the Fvco output. When this occures the phase detector signals the VCO to increase the frequency of the on-chip clock. If the falling edge of the Fref occures after(lag) the falling edge of the Fvco output, the detector signals the VCO to decrease on-chip clock frequency. Figure4 illustrates the lead and lag conditions. If the frequencies of the Fref and Fvco are the same, the detect or does not generate a control signal, so the frequencies remain the same.

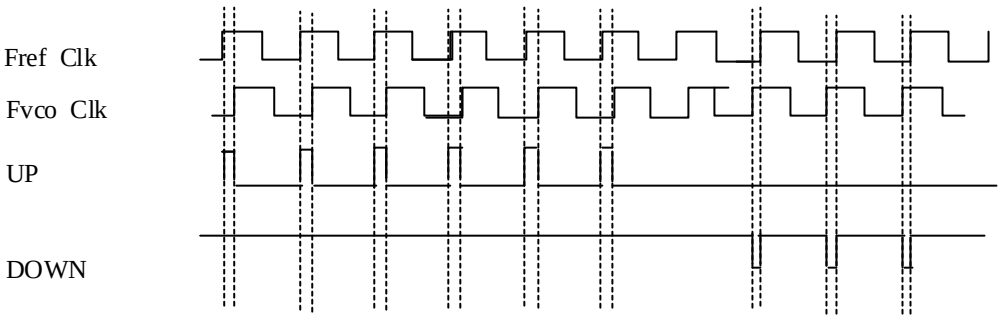


Figure4. Lead and Lag Clocking Relationships

Charge Pump : The charge pump converts the phase detector control signal to a charge in voltage across the external filter that drives the VCO. As the vcoltage Controlled Oscillator decreases, or increases, If the voltage remains constant, the frequency of the oscillator remains constant.

Loop Filter : The control signal that the phase detector generates for the charge pump may generate large excursions(ripples) each time the VCO output is compared to the system clock. To avoid overloading the VCO, a low pass filter samples and filters the high-frequency components out of the control signal. the filter is typically a single-pole RC filter consisting of a resistor and capacitor.

Voltage Controlled Oscillator(VCO) : The output voltage from the loop filter drives the VCO, causing its oscillation frequency to increas or decrease as a function of variations in voltage. When the VCO output matches the system clock in frequency and phase, the pahse detector stops sending a control signal to the charge pump, which in turn stabilizes the input voltage to the loop filter. The VCO frequency then remains constant, and the PLL remains locked onto the system clock

Frequency Synthesis

Frequency synthesis uses the system clock as a base frequency to generate higher/lower frequency clocks for internal logic.
For high speed applications in high-end designs, transmission line effects cause problems because of parastics and impedance mismatch among various on-board components.
These problems can be eliminated by moving the high frequency to the chip level.
On-chip clocks that are faster than the external system clock can be synthesized by inserting a divider in the feedback path. The divider is placed after voltage controlled oscillator, as illustrated in Figure1. The signal is running at M times the system clock frequency, so the PLL matches the divider signal output to the system clock. This configuation reduces the problem of interfacing to the system clock on the board, and it reduces the noise generated by the system clock oscillator and driver for all the components in the system

Design Considerations

The following design consideratios apply:.

* Jitter is affected by the power noise, substrate noise...etc.
  It increases when the noise level increases.
* A CMOS-level input reference clock is recommend for signal compatibility with the PLL circuit. Other levels such as TTL may degrade the tolerances.
* The use of two, or more PLLs requires special design considerations. Please consult your application engineer for more information.
* The following apply to the noise level, which can be minimized by using good analog power and ground isolation techniques in the system:
  - Use wide PCB traces for POWER(VDD25A2/VSS25A2, VDD25A1/VSS25A1) connections to the PLL core. Seperate the traces from the chip's VDD25A2/VSS25A2,VDD25A1/VSS25A1 supplies.
  - Use proper VDD25A2/VSS25A2,VDD25A1/VSS25A1 de-coupling.
  - Use good power and ground sources on the board.
  - Use Power VBBA for minimize substrate noise
* The PLL core should be placed as close as possible to the dedicated loop filter and analog **Power and ground pins.**
* It is inadvisable to locate noise-generating signals, such as data buses and high-current outputs, near the PLL I/O cells.
* Other related I/O signals should be placed near the PLL I/O but do not have any pre-defined placement restriction

Phantom Cell Information

- Pins of the core can be assigned externally(Package pins) or internally(internal ports) depending on design methods.
  The term "external" implies that the pins should be assigned externally like power pins.
  The term "internal/external" implies that these pins are user dependant

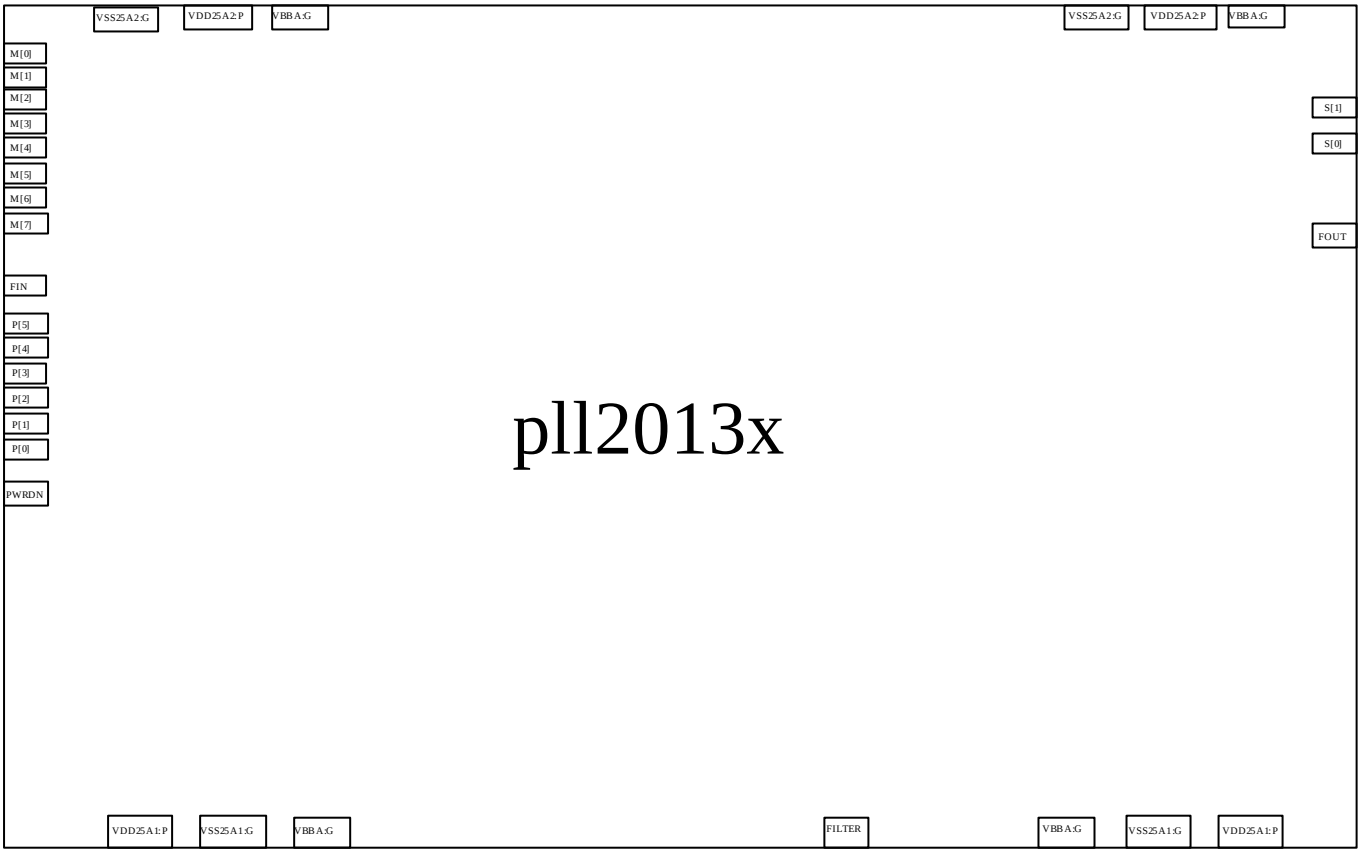


Figure. Phantom cell feature (Chip size : 631.46*422.16 um^2)

Pin Name	Pin Usage	Pin Layout Guide
VDD25A2	Extemal	-. Dedicated power/ground pins -. Power cuts are required to provide on-chip isolation => between dedicated PLL power/ground and all other power/ground -. Use good power and ground source on board
VSS25A2	Extemal	
VDD25A1	Extemal	
VSS25A1	Extemal	
VBBA	Extemal	
FIN	Extemal	-. Neighboring circuitry pads -. Use proper low jitter refernce clock
FOUT	Extemal	-. Neighboring circuitry pads -. Internal routing path should not be long, This will minimize loading effect. -. Fout signals should not be crossed by any signals and should not run next to digital signals. This will minimize capacitive coupling between the two signals.

Pin Name	Pin Usage	Pin Layout Guide
FILTER	External	-. Neighboring circuitry pads -. Ground Shielding -. The external loop filter pin is placed between the analog power to avoid stray coupling outside the chip and magnetic coupling via bond wires -. Closely placed Loop Filter components
PWRDN	Interanl/External	
M[7]~M[0]	Internal/External	
P[5]~P[0]	Internal/External	
S[1]~S[0]	Internal/External	

Table. Pin Layout Guide

PLL Specification

We appreciate your interest in our products. If you have further questions, please specify in the attached form. Thank you very much.

Parameter	Min	Typ	Max	Unit	Remarks
Supply Voltage					
Output frequency range					
Input frequency range					
Cycle to Cycle Jitter					
Lock up time					
Dynamic current					
Stand by current					
Output clock duty ratio					
Long term jitter					
Output slew rate					

- Do you need XTAL driver buffer in PLL Core?
  If you need it, what's the crystal frequency range? If not, What's the input frequency range?

- Do you need the lock detector?
- Do you need the I/O cell of SEC?
- Do you need the external pin for PLL test?
- What's the main frequency & frequency range?
- How many FSPLLs do you use in your system?
- What's output loading?
- Could you external/internal pin configurations as required?

Specially requested function list :

Version	Date	Modified Items	Comments
Ver 1.0	98.12.1	Original version published	
Ver 1.1	99.5.10	1. Change power name - VDDA -> VDD25A1 VSSA → VSS25A1 VDDD → VDD25A2 VSSD → VSS25A2 VBB → VBBA	
Ver 2.0	99.12.10	1. Font check	
Ver 2.1	00.3.29	1. Phantom Inform / Layout Guide 추가	
Ver 2.2	00.07.13	1. Pre-Divider Divisor ratio guide 2. Power Down시 current 재조정	
Ver 2.3	01.02.23	1. Power cell Guide 추가.	page 2> 참고.