ATAN Technology, Inc.

AT8985P 6 port 10/100 Mb/s Single Chip Ethernet Switch Controller

Preliminary Data Sheet

Revision 1.0

Feb 2002

Revision History

Revision Date	Revision	Description
April/2001	0.1	First ATAN version
May/2001	0.2	Change RXP, RXN, TXP, TXN
July/2001	0.3	Change hardware Setting pin from A1 version 1. ENDC16 Swap with Dual Color setting EEPROM 0x12h bit 15.. 2. Aging hardware setting change to EEPROM 0x10h bit7. Port7 FX select change to TXER power on latch. 3. At Dual Speed mode each port support 100/10 Full/Half
Aug/2001	0.4	Separate from AT8985P data sheet
Sep/2001	0.9	1. Remove PHY Register from Data Sheet 2. Add EEPROM read explain in Dupcol1 pin. 3. Modify LED display pin description.
Feb/2002	1.0	1. Add eeprom register 0x11h defaulted value as 0xff00h 2. Support By-pass Mode, register 0x11h bit5 3. Support Port-Base VLAN as default setting, Registger 0x11h Bit5 4. Special address forwarding 01 80 C2 00 00 00 DA Forwarding 01 80 C2 00 00 01 DA Filtering 01 80 C2 00 00 02 ~ 01 80 C2 00 00 0F DA Forwarding 5. Support Maximum Packet size as Bypass mode : Tag packet 1522Byte, Untag packet 1522byte Non-bypass mode : Tag packet 1526byte, Untag packet 1522byte 6. CFG0 pin86 must be externally connected to GND on PCB.

Notice:

This document contains preliminary information on new products under development.

The specifications are subject to change without any further notice.

Please contact ATAN sales to ensure the updated specifications before finalizing your own design.

1. Introduction

1.1 General Descriptions

The AT8985P is a high performance, low cost, highly integration (Controller, PHY and Memory) five-port 10/100 Mbps TX/FX plus one 10/100M MAC port Ethernet switch controller with all ports supporting 10/100 Mbps Full/Half duplex switch function. The AT8985P is intended for applications to stand alone bridge for low cost SOHO market such as 5Port switch or plus one CPU Router. AT8985P provide most advance function such as: 802.1p(Q.O.S.), 802.1q(VLAN), Port MAC address Locking, TP Auto MDIX , 25M Crystal & Extra sixth MII port function to meet customer request on Switch demand.

The AT8985P also supports Back-Pressure in Half-Duplex mode and 802.3x Flow Control Pause packet in Full-Duplex mode to prevent packet lost when buffer full. When Back Pressure is enabled, and there is no receive buffer available for the incoming packet, the AT8985P will issue a JAM pattern on the receiving port in Half Duplex mode and transmit the 802.3x Pause packet back to receiving end in Full Duplex mode.

The built-in 1Mbit SRAM used for packet buffer and address learning table is divided into 256 bytes/block to achieve the optimized memory utilization through complicated link list on packets with various lengths.

AT8985P also supports Port-Base, VLAN and IP TOS field checking for priority mapping. User can be easy to set as different priority mode in individual port, through a small low-cost micro controller to initialize or on-the-fly to configure. Each output port supports four queues in the way of fixed 8:4:2:1 fairness queuing to fit the bandwidth demand on various types of packet such as Voice, Video and data. 802.1Q, Tag/Untag, and up to 16 groups of VLAN also is supported. AT8985P learn last 4 bits of VLAN ID.

An intelligent address recognition algorithm makes AT8985P to recognize up to 2048 different MAC addresses and enables filtering and forwarding at full wire speed.

Port MAC address Locking function is also supported by AT8985P for customer used on Building Internet access to prevent multiple users share one port traffic.

1.2 Features

- ✓ Supports five 10M/100M auto-detect Half/Full duplex switch ports with **TX/FX** interfaces and one **MII** port.
- ✓ Built-in 16Kx64 SRAM.
- ✓ Supports 2048 MAC addresses table.
- ✓ Supports four queues for QOS at 8:4:2:1 rate.
- ✓ Supports priority features by Port-Based, 802.1p VLAN & IP TOS of packets.
- ✓ Supports Store & Forward architecture and performs forwarding and filtering at non-blocking full wire speed.
- ✓ Supports buffer allocation with 256 bytes per block
- ✓ Supports Aging function Enable/Disable.

- ✓ Supports per port Single/Dual color mode with Power On auto diagnostic.
- ✓ Supports 802.3x Flow Control pause packet for Full Duplex in case buffer is full.
- ✓ Supports Back Pressure function for Half Duplex operation in case buffer is full.
- ✓ Supports packet length up to 1522 bytes.
- ✓ Broadcast Storming Filter function.
- ✓ Supports 802.1Q VLAN. Up to 16 VLAN groups is implemented by the last four bits of VLAN ID.
- ✓ Supports TP interface **Auto MDIX** function for auto TX/RX swap by strapping-pin.
- ✓ 25M Crystal only for the whole system. Outputs, 25Mhz (for MII interface) clock for different applications.
- ✓ 128 QFP package with 2.25V/3.3V power supply.

1.3 Applications

AT8985P in 128-pin PQFP:

5 TX/FX + MII interface

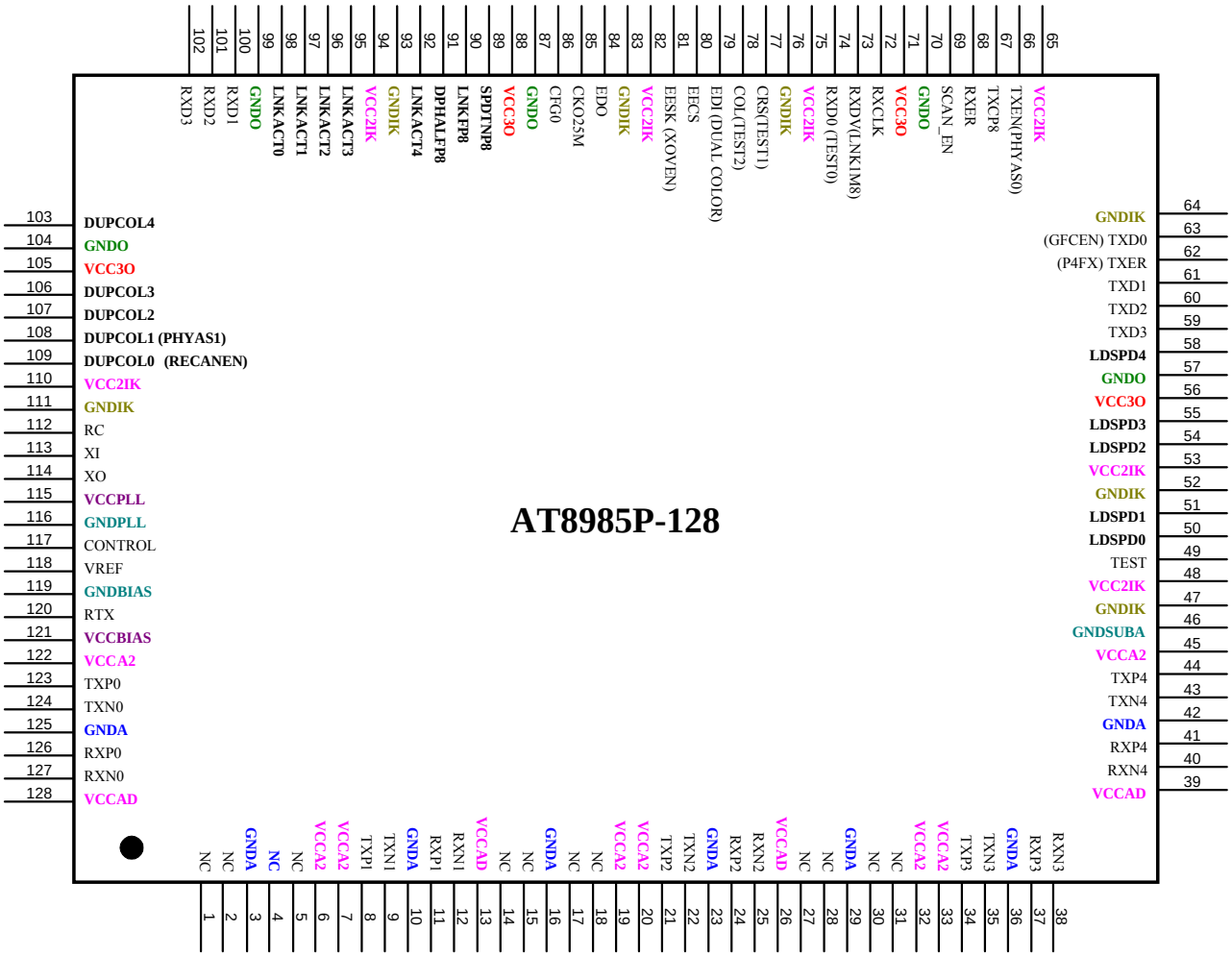
SOHO 5-port switch: 5-port switch + Router with MII CPU interface.

VoIP Phone with two10/100 TP and integrated-MII CPU.

Converter for HomePNA, powerline, and Ethernet.

2. Pinout

2.1 5 TP/FX PORT+ MII PORT 128 Pin Diagram



2.2 Pin Description

AT8985P-128 PINS(5TP+MII)

Pin Type I: Input, O: Output, I/O: Bi-directional, OD: Open drain, SCHE: Schmitt Trigger

PD : internal pull-down, PU : internal pull-up

Defaulted value of AT8985P :

Full-deplex, 100Mb/s, MDIX Off, auto-negotiation On, flow-control On, All TX mode, 5 TX+MII Mode.

Pin #	Pin Name	Pin Type	Pin Description
			Twisted Pair Interface, 32 pins
126, 11, 24, 37, 41	RXP[0:4]	I, Analog	**Twisted Pair Receive Input Positive.**
127, 12, 25, 38, 40	RXN[0:4]	I, Analog	**Twisted Pair Receive Input Negative.**
123, 8, 21, 34, 44	TXP[0:4]	O, Analog	**Twisted Pair Transmit Output Positive.**
124, 9, 22, 35, 43	TXN[0:4]	O, Analog	**Twisted Pair Transmit Output Negative.**
			6th Port(MII) Interfaces, 20 pins
63	TXD[0] /GFCEN	I/O, 8mA PU	**MII transmit data 0/Global Flow Control Enable.** At power-on-reset, latched as Flow control setting "1" to enable flow-control (defaulted), "0" to disable flow-control. For output mode, acts as MII transmit data TXD Synchronous to the rising edge of TXCLK Internally Pull-up.
59, 60, 61	TXD[3:1]	O, 8mA	**MII Transmit Data bit 3~1** Synchronous to the rising edge of TXCLK. These pins act as MII TXD[3:1].
62	TXER /P4FX	I/O 8mA PD	**MII transmit error/ P4FX** Indicator of PHY's transmitter error. Power-on-reset, signal latched as TX (if "0"), FX(if "1") mode at Port4. Internal pull down as Port4 at TX mode.
108,	DUPCOL1/ PHYAS1,	I/O 8mA PD	**Output mode :** **DUPCOL1, Duplex Collision LED for port1.** If pulled low , then acted as active high to drive "1" for full-duplex indication "0" for half-duplex and "blinking" for collision indication If pulled high, then acted as active low to drive "1" for half-duplex and "blinking" for collision indication "0" for full-duplex indication
66	TXEN/PHYAS0	I/O, 8mA PD	**TXEN, MII Transmit Enable.** **Input mode as strapping-pin :** **PHYAS1, PHYAS0** Recommend to set Value : 00 for Master mode: AT8985P will read 93C46 EEPROM first Bank.(00h~27h). Defaulted value : 00
102, 101, 100, 74	RXD[3:0]	I	**MII port receive data 3~0** These pins act as MII RXD[3:0]. Synchronous to the rising edge of RXCLK.
73	RXDV	I	**MII receive data valid**

68	RXER	I PD	**MII Port Receive Error**
78	COL	I PD	**MII Port Collision input** Internal pull down.
77	CRS	I PD	**MII Port Carrier Sense** Internal pull down.
72	RXCLK	I	**MII Port Receive Clock Input**
67	TXCLK	I	**MII Port Transmit clock Input**
91	DHALFP8	I PD	**MII Port Hardware Duplex input pin. Low: Full. High: Half. Internal pull down.**
90	LNKFP8	I PD	**MII Port Hardware Link input pin. Low: Link OK. High: Link Off. Internal pull down.**
89	SPDTNP8	I PD	**MII Port Hardware Speed input pins. Low: 100M. High: 10M. Internal pull down.**
			LED Interface, 15 pins
92, 95, 96, 97, 98	LNKACT[4:0]	O, 8mA	**LINK/Activity LED[4:0].** Active low "1" indicates no link activity on cable "0" indicates link okay on cable, but no activity and signals on idle stage. "blinking" indicates link activity on cable.
103, 106, 107 109	DUPCOL[4:2] DUPCOL[0]	O, 8mA	**Duplex/Collision LED[4:2,0].** Active low "1" for half-duplex and "blinking" for collision indication "0" for full-duplex indication
108	DUPCOL[1]	O, 8mA	**Duplex/Collision LED[1].** See "6thport MII interface" pin description for details.
109	DUPCOL0/ANEN	I/O, 8mA PU	**Duplex/Collision LED[0] / AutoNegotiation Enable.** On power-on-reset, latched as Auto Negotiation capability for all ports. "1" to enable AutoNegotiation (defaulted by pulled up internally), "0" to disable AutoNegotiation.
58, 55, 54, 51, 50	LDSPD[4:0]	O, 16mA	**Speed LED[4:0].** Used to indicate corresponding port's speed status. "0" for 100Mb/s, "1" for 10Mb/s
			EEPROM Interface,4 pins
84	EEDO	I, TTL,PU	**EEPROM Data Output.** Serial data input from EEPROM. This pin is internally pull-up.
80	EECS	O, 4mA,PD	**EEPROM Chip Select.** This pin is active high chip enable for EEPROM. When RESETL is low, it will be Tri-state. Internally Pull-down
81	EECK/ **XOVEN**	I/O, 4mA PD	**Serial Clock**. This pin is clock source for EEPROM. When RESETL is low, it will be tri-state. This pin is internal pull-down. **XOVEN.** On power-on-reset, latched as P4~0 Auto MDIX enable or not. "1" to disable MDIX (defaulted), "0" to enable MDIX. **Suggest externally pull up to enable MDIX for all ports.**
79	EEDI/Dual Color	I/O, 4mA PD	**EEPROM Serial Data Input.** This pin is output for serial data transfer. When RESETL is low, it will be tri-state. This pin is internal pull-down. **Dual Color.** On power-on-reset, latched as Dual Color mode or not. "0" to set Single color mode for LED. "1" to set Dual Color mode for LED.
			MISC., 9 pins
85	CKO25M	O, 8mA	**25M Clock Output for others.**
117	Control	O	**FET Control Signal.**

			The pin is used to control FET for 3.3V to 2.25V regulator.
120	RTX	Analog	**TX Resistor.**
118	VREF	Analog	**Analog Reference Voltage.**
112	RC	I, SCHE	**RC Input For Power On reset.**
113	XI	I, Analog	**25M Crystal Input.** 25M Crystal Input. Variation is limited to +/- 50ppm.
114	XO	O, Analog	**25M Crystal Output.** When connected to oscillator, this pin should left unconnected.
86	CFG0	I, TTL	Must Connected to GND.
49	TEST	I, TTL	**TEST Value.** At normal application connect to GND.
Power/Ground., 49 pins			
3, 10, 16, 23, 29, 36, 42, 125	GNDA		**Ground Used by AD Block.**
6, 7, 19, 20, 32, 33, 45, 122	VCCA2		**2.25V, Power Used by TX Line Driver.**
13, 26, 39, 128	VCCAD		**3.3V, Power Used by AD Block.**
46	GNDSUBA		**Ground Used by Analog Substrate**
119	GNDBIAS		**Ground Used by Bias Block**
121	VCCBIAS		**3.3V, Power Used by Bias Block.**
116	GNDPLL		**Ground used by PLL**
115	VCCPLL		**2.25V, Power used by PLL**
47, 52, 64, 76, 93, 83, 111	GNDIK		**Ground Used by Digital Core**
48, 53, 65, 75, 82, 94, 110	VCCIK		**2.25V, Power Used by Digital Core**
57, 70, 87, 99, 104	GNDO		**Ground Used by Digital Pad**
56, 71, 88, 105	VCC3O		**3.3V, Power Used by Digital Pad.**
69	ENSCAN/GND	I, TTL	**Scan Enable.** This pin will be used as the scan enable input for testing. Connect to GND at normal application.
NC pins, 12 pins			
1, 2, 4, 5, 14, 15, 17, 18, 27, 28, 30, 31	NC		**NC**

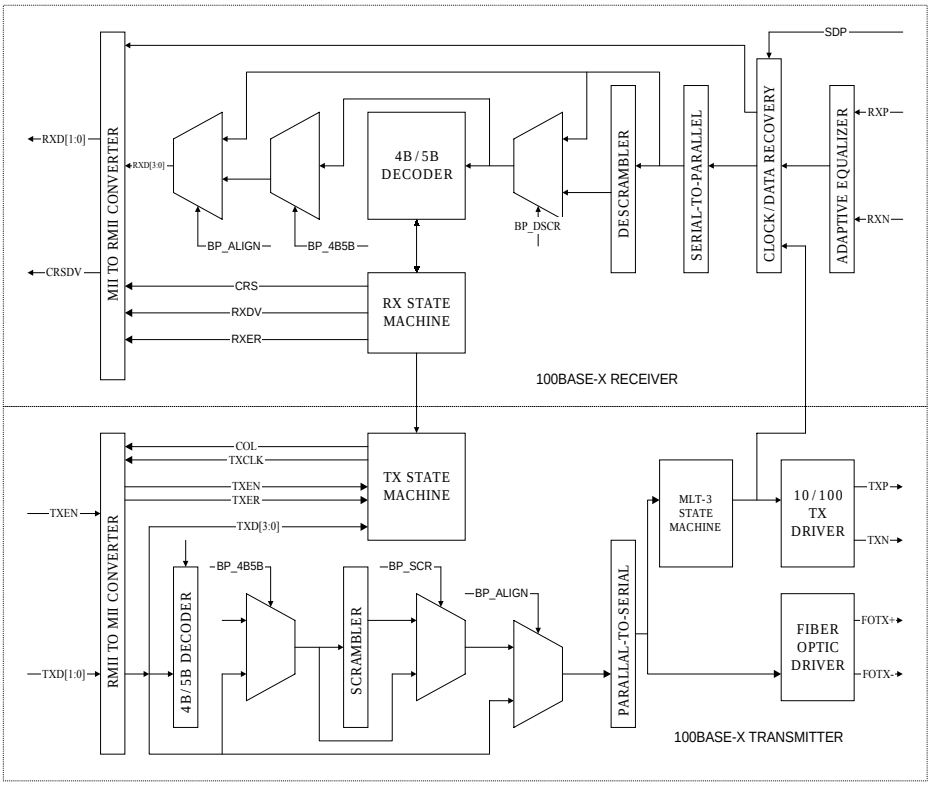
3. Descriptions

3.1 Functional Descriptions

The AT8985P integrates five 100Base-X physical sub-layer (PHY), 100Base-TX physical medium dependent (PMD) transceivers, five complete 10Base-T modules, 5 port 100/10 switch controller and one MII MAC and memory into a single chip for both 10 Mbits/s, 100 Mbits/s Ethernet switch operation. It also supports 100Base-FX operation through external fiber-optic transceivers. The device is capable of operating in either Full Duplex mode or Half-Duplex mode in either 10 Mbits/s or 100 Mbits/s operation. Operational modes can be selected by hardware configuration pins, software settings of management registers, or determined by the on-chip auto negotiation logic.

The AT8985P consists of three major blocks:

- 10/100M PHY Block
- Switch Controller Block
- Built-in 16Kx64 SSRAM



PHY Internal Block

The interfaces used for communication between PHY block and switch core is MII interface.
Auto MDIX function is supported in this block. This function can be Enable/Disable by hardware pin.

3.2 10/100M PHY Block

The 100Base-X section of the device implements he following functional blocks :

- 100Base-X physical coding sub-layer (PCS)
- 100Base-X physical medium attachment (PMA)
- Twisted-pair transceiver (PMD)

The 100Base-X and 10Base-T sections share the following functional blocks :

- Clock synthesizer module
- MII Registers
- IEEE 802.3u auto negotiation

3.2.1 100Base-X Module

The AT8985P implements 100Base-X compliant PCS and PMA and 100Base-TX compliant TP-PMD as illustrated in Figure 2. Bypass options for each of the major functional blocks within the 100Base-X PCS provides flexibility for various applications. 100 Mbits/s PHY loop back is included for diagnostic purpose.

3.2.2 100Base-X Receiver

The 100Base-X receiver consists of functional blocks required to recover and condition the 125 Mbits/s receive data stream. The AT8985P implements the 100Base-X receiving state machine diagram as given in ANSI/IEEE Standard 802.3u, Clause 24. The 125 Mbits/s receive data stream may originate from the on-chip twisted-pair transceiver in a 100Base-TX application. Alternatively, the receive data stream may be generated by an external optical receiver as in a 100Base-FX application.

The receiver block consists of the following functional sub-blocks :

- A/D Converter
- Adaptive Equalizer and timing recovery module
- NRZI/NRZ and serial/parallel decoder
- De-scrambler
- Symbol alignment block
- Symbol Decoder
- Collision Detect Block
- Carrier sense Block
- Stream decoder block

3.2.2.1 A/D Converter

High performance A/D converter with 125Mhz sampling rate converts signals received on RXP/RXN pins to 6 bits data streams; besides it possess auto-gain-control capability that will further improve receive performance especially under long cable or harsh detrimental signal integrity. Due to high pass characteristic on transformer, built in base-line-wander correcting circuit will cancel it out and restore its DC level.

3.2.2.2 Adaptive Equalizer and timing Recovery Module

All digital design is especial immune from noise environments and achieves better correlation between production and system testing. Baud rate Adaptive Equalizer/Timing Recovery compensates line loss induced from twisted pair and tracks far end clock at 125M samples per second. Adaptive Equalizer implemented with Feed forward and Decision Feedback techniques meet the requirement of BER less than 10-12 for transmission on CAT5 twisted pair cable ranging from 0 to 120 meters.

3.2.2.3 NRZI/NRZ and Serial/Parallel Decoder

The recovered data is converted from NRZI to NRZ. The data is not necessarily aligned to 4B/5B code group's boundary.

3.2.2.4 Data De-scrambling

The de-scrambler acquires synchronization with the data stream by recognizing idle bursts of 40 or more bits and locking its deciphering Linear Feedback Shift Register (LFSR) to the state of the scrambling LFSR. Upon achieving synchronization, the incoming data is XORed by the deciphering LFSR and de-scrambled.
In order to maintain synchronization, the de-scrambler continuously monitors the validity of the unscrambled data that it generates. To ensure this, a link state monitor and a hold timer are used to constantly monitor the synchronization status. Upon synchronization of the de-scrambler the hold timer starts a 722 us countdown. Upon detection of sufficient idle symbols within the 722 us period, the hold timer will reset and begin a new countdown. This monitoring operation will continue indefinitely given a properly operating network connection with good signal integrity. If the link state monitor does not recognize sufficient unscrambled idle symbols within 722 us period, the de-scrambler will be forced out of the current state of synchronization and reset in order to re-acquire synchronization.

3.2.2.5 Symbol Alignment

The symbol alignment circuit in the AT8985P determines code word alignment by recognizing the /J/K delimiter pair. This circuit operates on unaligned data from the de-scrambler. Once the /J/K symbol pair (11000 10001) is detected, subsequent data is aligned on a fixed boundary.

3.2.2.6 Symbol Decoding

The symbol decoder functions as a look-up table that translates incoming 5B symbols into 4B nibbles as shown in Table 1. The symbol decoder first detects the /J/K symbol pair preceded by idle symbols and replaces the symbol with MAC preamble. All subsequent 5B symbols are converted to the corresponding 4B nibbles for the duration of the entire packet. This conversion ceases upon the detection of the /T/R symbol pair denoting the end of stream delimiter (ESD). The translated data is presented on the internal RXD[3:0] signal lines with RXD[0] represents the least significant bit of the translated nibble.

3.2.2.7 Valid Data Signal

The valid data signal (RXDV) indicates that recovered and decoded nibbles are being presented on the internal RXD[3:0] synchronous to receive clock, RXCLK. RXDV is asserted when the first nibble of translated /J/K is ready for transfer over the internal MII. It remains active until either the /T/R delimiter is recognized, link test indicates failure, or no signal is detected. On any of these conditions, RXDV is de-asserted.

3.2.2.8 Receive Errors

The RXER signal is used to communicate receiver error conditions. While the receiver is in a state of holding RXDV asserted, the RXER will be asserted for each code word that does not map to a valid code-group.

3.2.2.9 100Base-X Link Monitor

The 100Base-X link monitor function allows the receiver to ensure that reliable data is being received. Without reliable data reception, the link monitor will halt both transmit and receive operations until such time that a valid link is detected. The AT8985P performs the link integrity test as outlined in IEEE 100Base-X (Clause 24) link monitor state diagram. The link status is multiplexed with 10 Mbits/s link status to form the reportable link status bit in serial management register 1h, and driven to the LNKACT pin.

When persistent signal energy is detected on the network, the logic moves into a Link-Ready state after approximately 500 us, and waits for an enable from the auto negotiation module. When receive, the link-up state is entered, and the transmission and reception logic blocks become active. Should auto negotiation be disabled, the link integrity logic moves immediately to the link-up state after entering the link-ready state.

3.2.2.10 Carrier Sense

Carrier sense (CRS) for 100 Mbits/s operation is asserted upon the detection of two noncontiguous zeros occurring within any 10-bit boundary of the received data stream.

The carrier sense function is independent of symbol alignment. In switch mode, CRS is asserted during either packet transmission or reception. For repeater mode, CRS is asserted only during packet reception. When the idle symbol pair is detected in the received data stream, CRS is de-asserted. In repeater mode, CRS is only asserted due to receive activity. CRS is intended to encapsulate RXDV.

3.2.2.11 Bad SSD Detection

A bad start of stream delimiter (Bad SSD) is an error condition that occurs in the 100Base-X receiver if carrier is detected (CRS asserted) and a valid /J/K set of code-group (SSD) is not received.

If this condition is detected, then the AT8985P will assert RXER and present RXD[3:0] = 1110 to the internal MII for the cycles hat correspond to received 5B code-groups until at least two idle code-groups are detected. Once at least two idle code groups are detected, RXER and CRS become de-asserted.

3.2.2.12 Far-End Fault

Auto negotiation provides a mechanism for transferring information from the Local Station to the link Partner that a remote fault has occurred for 100Base-TX. As auto negotiation is not currently specified for operation over fiber, the far end fault indication function (FEFI) provides this capability for 100Base-FX applications.

A remote fault is an error in the link that one station can detect while the other cannot. An example of this is a disconnected wire at a station's transmitter. This station will be receiving valid data and detect that the link is good via the link integrity monitor, but will not be able to detect that its transmission is not propagating to the other station.

A 100Base-FX station that detects such a remote fault may modify its transmitted idle stream from all ones to a group of 84 ones followed by a single 0. This is referred to as the FEFI idle pattern.

3.2.3 100Base-TX Transceiver

AT8985P implements a TP-PMD compliant transceiver for 100Base-TX operation. The differential transmit driver is

shared by the 10Base-T and 100Base-TX subsystems. This arrangement results in one device that uses the same external magnetic for both the 10Base-T and the 100Base-TX transmission with simple RC component connections. The individually wave-shaped 10Base-T and 100Base-TX transmit signals are multiplexed in the transmission output driver selection.

3.2.3.1 Transmit Drivers

The AT8985P 100Base-TX transmission driver implements MLT-3 translation and wave-shaping functions. The rise/fall time of the output signal is closely controlled to conform to the target range specified in the ANSI TP-PMD standard.

3.2.3.2 Twisted-Pair Receiver

For 100Base-TX operation, the incoming signal is detected by the on-chip twisted-pair receiver that consists of a differential line receiver, an adaptive equalizer and a base-line wander compensation circuits.
The AT8985P uses an adaptive equalizer that changes filter frequency response in accordance with cable length. The cable length is estimated based on the incoming signal strength. The equalizer tunes itself automatically for any cable length to compensate for the amplitude and phase distortions incurred from the cable.

3.2.4 10Base-T Module

The 10Base-T Transceiver Module is IEEE 802.3 compliant. It includes the receiver, transmitter, collision, heartbeat, loop back, jabber, wave shaper, and link integrity functions, as defined in the standard. Figure 3 provides an overview for the 10Base-T module.
The AT8985P 10Base-T module is comprised of the following functional blocks:

√ Manchester encoder and decoder
√ Collision detector
√ Link test function
√ Transmit driver and receiver
√ Serial and parallel interface
√ Jabber and SQE test functions
√ Polarity detection and correction

3.2.4.1 Operation Modes

The AT8985P 10Base-T module is capable of operating in either half-duplex mode or full-duplex mode. In half-duplex mode, the AT8985P functions as an IEEE 802.3 compliant transceiver with fully integrated filtering. The COL signal is asserted during collisions or jabber events, and the CRS signal is asserted during transmit and receive. In full duplex mode the AT8985P can simultaneously transmit and receive data.

3.2.4.2 Manchester Encoder/Decoder

Data encoding and transmission begins when the transmission enable input (TXEN) goes high and continues as long as the transceiver is in good link state. Transmission ends when the transmission enable input goes low. The last transition occurs at the center of the bit cell if the last bit is a 1, or at the boundary of the bit cell if the last bit is 0.
Decoding is accomplished by a differential input receiver circuit and a phase-locked loop that separate the Manchester-encoded data stream into clock signals and NRZ data. The decoder detects the end of a frame when no more

mid bit transitions are detected. Within one and half bit times after the last bit, carrier sense is de-asserted.

3.2.4.3 Transmit Driver and Receiver

The AT8985P integrates all the required signal conditioning functions in its 10Base-T block such that external filters are not required. Only one isolation transformer and impedance matching resistors are needed for the 10Base-T transmit and receive interface. The internal transmit filtering ensures that all the harmonics in the transmission signal are attenuated properly.

3.2.4.4 Smart Squelch

The smart squelch circuit is responsible for determining when valid data is present on the differential receive. The AT8985P implements an intelligent receive squelch on the RXP/RXN differential inputs to ensure that impulse noise on the receive inputs will not be mistaken for a valid signal. The squelch circuitry employs a combination of amplitude and timing measurements (as specified in the IEEE 802.3 10Base-T standard) to determine the validity of data on the twisted-pair inputs.
The signal at the start of the packet is checked by the analog squelch circuit and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) will be rejected. Once this first squelch level is overcome correctly, the opposite squelch level must then be exceeded within 150ns. Finally, the signal must exceed the original squelch level within an additional 150ns to ensure that the input waveform will not be rejected.
Only after all these conditions have been satisfied will a control signal be generated to indicate to the remainder of the circuitry that valid data is present.
Valid data is considered to be present until the squelch level has not been generated for a time longer than 200 ns, indicating end of packet. Once good data has been detected, the squelch levels are reduced to minimize the effect of noise, causing premature end-of-packet detection. The receive squelch threshold level can be lowered for use in longer cable applications. This is achieved by setting bit 10 of register address 11h.

3.2.5 Carrier Sense

Carrier Sense (CRS) is asserted due to receive activity once valid data is detected via the smart squelch function. For 10 Mbits/s half duplex operation, CRS is asserted during either packet transmission or reception. For 10 Mbits/s full duplex and repeater mode operations, the CRS is asserted only due to receive activity.

3.2.6 Jabber Function

The jabber function monitors the AT8985P output and disables the transmitter if it attempts to transmit a longer than legal sized packet. If TXEN is high for greater than 24ms, the 10Base-T transmitter will be disabled. Once disabled by the jabber function, the transmitter stays disabled for the entire time that the TXEN signal is asserted. This signal has to be de-

asserted for approximately 256 ms (The un-jab time) before the jabber function re-enables the transmit outputs. The jabber function can be disabled by programming bit 4 of register address 10h to high.

3.2.7 Link Test Function

A link pulse is used to check he integrity of the connection with the remote end. If valid link pulses are not received, the link detector disables the 10Base-T twisted-pair transmitter, receiver, and collision detection functions.

The link pulse generator produces pulses as defined in IEEE 802.3 10Base-T standard. Each link pulse is nominally 100ns in duration and is transmitted every 16 ms, in the absence of transmit data.

3.2.8 Automatic Link Polarity Detection

AT8985P's 10Base-T transceiver module incorporates an "automatic link polarity detection circuit". The inverted polarity is determined when seven consecutive link pulses of inverted polarity or three consecutive packets are received with inverted end-of-packet pulses. If the input polarity is reversed, the error condition will be automatically corrected and reported in bit 5 of register 10h.

3.2.9 Clock Synthesizer

The AT8985P implements a clock synthesizer that generates all the reference clocks needed from a single external frequency source. The clock source must be a TTL level signal at 25 MHz +/- 50ppm

3.3 Auto Negotiation

The Auto Negotiation function provides a mechanism for exchanging configuration information between two ends of a link segment and automatically selecting the highest performance mode of operation supported by both devices. Fast Link Pulse (FLP) Bursts provide the signaling used to communicate auto negotiation abilities between two devices at each end of a link segment. For further detail regarding auto negotiation, refer to Clause 28 of the IEEE 802.3u specification. The AT8985P supports four different Ethernet protocols, so the inclusion of auto negotiation ensures that the highest performance protocol will be selected based on the ability of the link partner.
Highest priority relative to the following list.

1. 100Base-TX full duplex (highest priority)
2. 100Base-TX half duplex
3. 10Base-T full duplex
4. 10Base-T half duplex (lowest priority)

3.4 Switch Functional Description

The AT8985P uses a "store & forward" switching approach for the following reason:
Store & forward switches allow switching between different speed media (e.g. 10BaseX and 100BaseX). Such switches require the large elastic buffer especially bridging between a server on a 100Mbps network and clients on a 10Mbps segment.
Store & forward switches improve overall network performance by acting as a "network cache"
Store & forward switches prevent the forwarding of corrupted packets by the frame check sequence (FCS) before forwarding to the destination port.

3.4.1 Basic Operation

The AT8985P receives incoming packets from one of its ports, searches in the Address Table for the Destination MAC Address and then forwards the packet to the other port within same VLAN group, if appropriate. If the destination address is not found in the address table, the AT8985P treats the packet as a broadcast packet and forwards the packet to the other ports which in same VLAN group.
The AT8985P automatically learns the port number of attached network devices by examining the Source MAC Address of all incoming packets at wire speed. If the Source Address is not found in the Address Table, the device adds it to the

table.

3.4.1.1 Address Learning

The AT8985P uses a hash algorithm to learn the MAC address and can learn up to 2K MAC addresses. Address is stored in the Address Table. The AT8985P searches for the Source Address (SA) of an incoming packet in the Address Table and acts as below:

If the SA was not found in the Address Table (a new address), the AT8985P waits until the end of the packet (non-error packet) and updates the Address Table. If the SA was found in the Address Table, then aging value of each corresponding entry will be reset to 0.

When the DA is PAUSE command, then the learning process will be disabled automatically by AT8985P.

3.4.1.2 Address Recognition and Packet Forwarding

The AT8985P forwards the incoming packets between bridged ports according to the Destination Address (DA) as below. All the packet forwarding will check VLAN first. Forwarding port must same VLAN with source port.

(1) If the DA is an UNICAST address and the address was found in the Address Table, the AT8985P will check the port number and acts as follows:

- If the port number is equal to the port on which the packet was received, the packet is discarded.
- If the port number is different, the packet is forwarded across the bridge.

(2) If the DA is an UNICAST address and the address was not found, the AT8985P treats it as a multicast packet and forwards across the bridge.

(3) If the DA is a Multicast address, the packet is forwarded across the bridge.

(4) If the DA is PAUSE Command (01-80-C2-00-00-01), then this packet will be dropped by AT8985P. AT8985P can issue and learn PAUSE command.

(5) AT8985P will forward the packet with DA of (01-80-C2-00-00-00), filter out the packet with DA of (01-80-C2-00-00-01), and forward the packet with DA of (01-80-C2-00-00-02 ~ 01-80-C2-00-00-0F)

3.4.1.3 Address Aging

Address aging is supported for topology changes such as an address moving from one port to the other. When this happens, the AT8985P internally has a 300 seconds timer will aged out (remove) the address from the address table. Aging function can enable/disable by user. Normally, disabling aging function is for security purpose.

3.4.1.4 Buffers and Queues

The AT8985P incorporates nine transmit queues and receive buffer area for the nine ETHERNET ports. The receive buffers as well as the transmitted queues are located within the AT8985P along with the switch fabric. The buffers are divided into 448 blocks of 256 bytes each. The queues of each port are managed according to each port's read/write pointer.

Input buffers and output queues are maintained through ATAN proprietary patent pending UNIQUE (Universal Queue management) scheme.

3.4.1.5 Back off Algorithm

The AT8985P implements the truncated exponential back off algorithm compliant to the 802.3 CSMA-CD standard. AT8985P will restart the back off algorithm by choosing 0-9 collision counts. The AT8985P resets the collision counter after 16 consecutive retransmit trials.

3.4.1.6 Inter-Packet Gap (IPG)

IPG is the idle time between any two successive packets from the same port. The typical number is 96 bits time. The value is 9.6us for 10Mbps ETHERNET, 960ns for 100Mbps fast ETHERNET and 96ns for 1000M. AT8985P provide option of 92 bit gap in EEPROM to prevent packet lost when turn off Flow Control and clock P.P.M. value difference.

3.4.1.7 Illegal Frames

The AT8985P will discard all illegal frames such as runt packet (less than 64 bytes), oversize packet (greater than 1518 or 1522 bytes) and bad CRC. Dribbling packing with good CRC value will accept by AT8985P. In case of bypass mode enabled, AT8985P will support tag and untagged packets with size up to 1522 bytes. In case of non-bypass mode, AT8985P will support tag packets up to 1526bytes, untagged packets up to 1522bytes.

3.4.1.8 Half Duplex Flow Control

Back Pressure function is supported for half-duplex operation. When the AT8985P cannot allocate a receive buffer for an incoming packet (buffer full), the device will transmit a jam pattern on the port, thus forcing a collision. Back Pressure is enabled by the BPEN set during RESET asserting. An ATAN proprietary algorithm is implemented inside the AT8985P to prevent back pressure function cause HUB partitioned under heavy traffic environment and reduce the packet lost rate to increase the whole system performance.

3.4.1.9 Full Duplex Flow Control

When full duplex port run out of its receive buffer, a PAUSE packet command will be issued by AT8985P to notice the packet sender to pause transmission. This frame based flow control is totally compliant to IEEE 802.3x. AT8985P can issue or receive pause packet.

3.4.1.10 Broadcast Storm filter

If Broadcast Storming filter is enable, the broadcast packets over the rising threshold within 50 ms will be discarded by the threshold setting. See EEPROM Reg.10h.

Broadcast storm mode after initial:

- time interval : 50ms

  the max. packet number = 7490 in 100Base, 749 in 10Base

Per Port Rising Threshold				
	00	01	10	11
All 100TX	Disable	10%	20%	40%
Not All 100TX	Disable	1%	2%	4%

Per Port Falling Threshold				
	00	01	10	11
All 100TX	Disable	5%	10%	20%
Not All 100TX	Disable	0.5%	1%	2%

3.4.2 Auto TP MDIX function

At normal application which Switch connect to NIC card is by one by one TP cable. If Switch connect other device such as another Switch must by two way. First one is Cross Over TP cable. Second way is use extra RJ45 which crossover internal TX+- and RX+- signal. By second way customer can use one by one cable to connect two Switch devices. All these effort need extra cost and not good solution. AT8985P provide Auto MDIX function which can adjust TX+- and RX+- at correct pin. User can use one by one cable between AT8985P and other device. This function can be Enable/Disable by hardware pin and EEPROM option.

3.4.3 Port Locking

Port locking function will provide customer simple way to limit per port user number to one. If this function is turn on then AT8985P will lock first MAC address in learning table. After this MAC address locking will never age out except Reset signal. Another MAC address which not same as locking one will be dropped. AT8985P provide one MAC address per port. This function is per port setting. When turn on Port Locking function, recommend customer turn off aging function.

3.4.4 VLAN setting & Tag/Untag & port-base VLAN

AT8985P supports bypass mode and untagged port as default setting while the chip is power-on. Thus, every packet with or without tag will be forwarding to the destination port without any modification by AT8985P. Meanwhile port-base VLAN could be enabled according to the PVID value (4bits to map 16 groups written at register 13 to register 22) of the configuration content of each port (port0 at register01, port1 at reg.03, port2 at reg.05, port3 at reg.07, port4 at reg.o8, MII port at reg. 09).

AT8985P also supports 16 VLAN groups. In VLAN four bytes tag include twelve VLAN ID as VID. AT8985P learn last four bits of VID. If user need to use this function, two EEPROM registers are needed to be programmed first :

* Port VID number at EEPROM register 0x1~0x9 bit 13~10: AT8985P will check coming packet. If coming packet is non VLAN packet then AT8985P will add four bytes VLAN tag to this packet. The LSB of VID will add these four bits value.

* VLAN Group Mapping Register. EEPROM register 013h~022h define VLAN grouping value. User use these register to define VLAN group.

User can define each port as Tag port or Untag port by Configuration register Bit 4. The operation of packet between Tag port and Untag port can explain by follow example:

Example1: Port receives Untag packet and send to Untag port.

AT8985P will check the port VLAN ID first then check VLAN group resister. If destination port same VLAN as receiving port then this packet will forward to destination port without any change. If destination port not same VLAN as receiving port then this packet will be dropped.

Example2: Port receives Untag packet and send to Tag port.

AT8985P will check the port VLAN ID first then check VLAN group resister. If destination port same VLAN as receiving port than this packet will forward to destination port with four byte VLAN Tag and new CRC. If destination port not same VLAN as receiving port then this packet will be dropped.

Example3: Port receives Tag packet and send to Untag port.

AT8985P will check the packet VLAN ID first then check VLAN group resister. If destination port same VLAN as receiving port than this packet will forward to destination port after remove four bytes with new CRC error. If destination port not same VLAN as receiving port then this packet will be dropped.

Example4: Port receives Tag packet and send to Tag port.

AT8985P will check the packet VLAN ID first then check VLAN group resister. If destination port same VLAN as receiving port than this packet will forward to destination port after remove without any change. If destination port not same VLAN as receiving port then this packet will be dropped.

3.4.5 Priority Setting

By the trend of data, voice and video will put on networking, Switch not only deal data packet but also provide service

of multimedia data. AT8985P provides four priority queues on each port with 8:4:2:1 rate. This priority function can set three ways as below:

* By Port Base: Set specific port at specific queue. AT8985P only check the port priority and not check VLAN and TOS.
* By VLAN first: AT8985P check VLAN three priority bit first then TOS priority bits.
* By IP TOS first: AT8985P check IP TOS three priority bit first then VLAN three priority bits.

User can set drop low priority queue (Q0, Q1 & Q2) when buffer full. This function is optional.

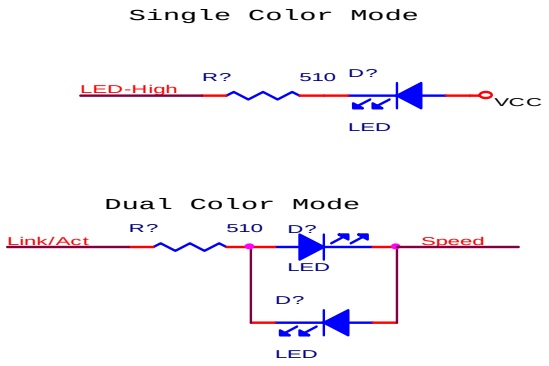
3.4.6 Buffer Management

By the trend of embedded memory in chip the packet buffer number is limited. AT8985P embedded 1M bit SSRAM. At normal application of real network operation most of packet size is under 256 bytes. AT8985P internal memory is 256 bytes/block. If receiving packet less than 256 bytes than this packet will occupied one block. If more than 256 bytes packet coming AT8985P will chain 2~6 block to store this packet. This buffer management will provide better memory utilization on limited memory size and get better performance on real network application.

3.4.7 LED Display

Three LED per port are provided by AT8985P. Link/Act, Duplex/Col & Speed are three LED display of AT8985P. Dual color LED mode also supported by AT8985P. For easy production purpose AT8985P will send test signal to each LED one by one at power on reset stage. EEPROM register 0x12h define LED configuration table.

AT8985P/GP LED is active Low signal. Dupcol0 & Dupcol1 will check external signal at Reset time. If external signal add pull high then LED will active Low. If external signal add pull down resister then LED will drive high.



3.5 EEPROM Content

EEPROM provides AT8985P many options setting such as:

* Port Configuration: Speed, Duplex, Flow Control Capability.
* VLAN & TOS Priority Mapping

* Broadcast Storming rate
* Fiber Select, Auto MDIX select
* VLAN Mapping
* Per Port Buffer number

EEPROM Registers

Register	Bit 15- 8	Bit 7 - 0	Default Value
0x00h	Signature	Signature	4154h
0x01h	Port 0 Configuration	Port 0 Configuration	40fh
0x02h	Reserve	Reserve	40fh
0x03h	Port 1 Configuration	Port 1 Configuration	40fh
0x04h	Reserve	Reserve	40fh
0x05h	Port 2 Configuration	Port 2 Configuration	40fh
0x06h	Reserve	Reserve	40fh
0x07h	Port 3 Configuration	Port 3 Configuration	40fh
0x08h	Port 4 Configuration	Port 4 Configuration	40fh
0x09h	MII Port Configuration	MII Port Configuration	40fh
0x0ah	Configuration	Configuration	0h
0x0bh	Customized MII Register for MII Port	Customized MII Register for Port 0~4	8000h
0x0ch	Reserve	Reserve	fa50h
0x0dh	Reserve	Reserve	fa50h
0x0eh	VLAN priority Map High	VLAN priority Map Low	fa50h
0x0fh	TOS priority Map High	TOS priority Map Low	fa50h
0x10h	Miscellaneous Configuration 0	Miscellaneous Configuration 0	aa40h
0x11h	Reserved	VLAN mode select	ff00h
0x12h	Miscellaneous Configuration 1	Miscellaneous Configuration 1	3600h
0x13h	VLAN 0 outbound Port Map	VLAN 0 outbound Port Map	1ffh
0x14h	VLAN 1 outbound Port Map	VLAN 1 outbound Port Map	1ffh
0x15h	VLAN 2 outbound Port Map	VLAN 2 outbound Port Map	1ffh
0x16h	VLAN 3 outbound Port Map	VLAN 3 outbound Port Map	1ffh
0x17h	VLAN 4 outbound Port Map	VLAN 4 outbound Port Map	1ffh
0x18h	VLAN 5 outbound Port Map	VLAN 5 outbound Port Map	1ffh
0x19h	VLAN 6 outbound Port Map	VLAN 6 outbound Port Map	1ffh

0x1ah	VLAN 7 outbound Port Map	VLAN 7 outbound Port Map	1ffh
0x1bh	VLAN 8 outbound Port Map	VLAN 8 outbound Port Map	1ffh
0x1ch	VLAN 9 outbound Port Map	VLAN 9 outbound Port Map	1ffh
0x1dh	VLAN 10 outbound Port Map	VLAN 10 outbound Port Map	1ffh
0x1eh	VLAN 11 outbound Port Map	VLAN 11 outbound Port Map	1ffh
0x1fh	VLAN 12 outbound Port Map	VLAN 12 outbound Port Map	1ffh
0x20h	VLAN 13 outbound Port Map	VLAN 13 outbound Port Map	1ffh
0x21h	VLAN 14 outbound Port Map	VLAN 14 outbound Port Map	1ffh
0x22h	VLAN 15 outbound Port Map	VLAN 15 outbound Port Map	1ffh
0x23h	Reserve	P0 Buffer Threshold	0h
0x24h	Reserve	P1 Buffer Threshold	0h
0x25h	Reserve	P2 Buffer Threshold	0h
0x26h	P4 Buffer Threshold	P3 Buffer Threshold	0h
0x27h	Threshold Sel / Total Buffer Threshold	MII Port Buffer Threshold	0h

Signature Register:0x00h

Configuration	Description
Bit [15:0]	The value must be 4154h(AT)

Configuration Registers: Register 0x01h ~ 0x09h

Configuration	Description
Bit 0	802.3x Flow control command ability
Bit 1	Auto negotiation Enable. High enable, Low disable
Bit 2	Speed. High 100TX, Low 10 Base-T
Bit 3	Duplex. High Full, Low Half
Bit 4	VLAN Tag : ‘1’ or UnTag Port : ‘0’ default
Bit 5	Reserve
Bit 6	TOS over VLAN priority
Bit 7	Enable port-base priority
Bit [9:8]	Port-base priority
Bit [13:10]	PVID. Port base VLAN ID
Bit[14]	Select FX

Bit [15]	Crossover auto-detect enable

Register 0x0ah: Reserve

Configuration	Description
Bit [7:0]	Reserve
Bit 8	Reserve
Bit 9	Enable Replace VLAN ID 0 &1 by PVID
Bit [15:10]	Reserved

Customized MII Address Register: Register 0x0bh

Configuration	Description
Bit [4:0]	Port 0~4 MII Register Address
Bit 5	Port 0~4 MII Write Enable. High Active
Bit 6	Enable IPG leveling
Bit 7	Enable Trunk Port
Bit [12:8]	Reserve
Bit 13	Reserve
Bit 14	Reserve
Bit 15	Reserve

Register 0x0ch: Reserve

Configuration	Description
Bit [15:0]	Reserve

Register 0x0dh: Reserve

Configuration	Description
Bit [15:0]	Reserve

VLAN(TOS) priority Map: Register 0x0eh (VLAN), 0x0fh(TOS)

Configuration	Description
Bit [1:0]	Mapped priority of tag value(VLAN, TOS) 0
Bit [3:2]	Mapped priority of tag value(VLAN, TOS) 1

Bit [5:4]	Mapped priority of tag value(VLAN, TOS) 2
Bit [7:6]	Mapped priority of tag value(VLAN, TOS) 3
Bit [9:8]	Mapped priority of tag value(VLAN, TOS) 4
Bit [11:10]	Mapped priority of tag value(VLAN, TOS) 5
Bit [13:12]	Mapped priority of tag value(VLAN, TOS) 6
Bit [15:14]	Mapped priority of tag value(VLAN, TOS) 7

00: lowest priority queue. Q0

01: lower priority queue. Q1

10: higher priority queue. Q2

11: highest priority queue. Q3

The weight ratio is Q0: Q1: Q2: Q3=1: 2: 4: 8. The default is Q1 for un-tag packet and none IP frame.

Miscellaneous Configuration: Register 0x10h

Configuration	Description
Bit [1:0]	Broadcast Storming Threshold[1:0]
Bit [2]	Broadcast Storming Enable
Bit [3]	Reserve
Bit [4]	XCRC (0/XCRCCHK, enable CRC Check)
Bit [5]	Reserve
Bit [6]	SWCLK (switch rxclk to txclk for 7-wire)
Bit [7]	Aging Disable
Bit [15:8]	Reserve

VLAN mode select Register: Register 0x11h, default value is 0xff00h

Configuration	Description
Bit [4:0]	Reserved, default value 0
Bit [5]	VLAN mode select, default 0 0 : by-pass mode with port-base VLAN 1 : VLAN ID base VLAN.
Bit [7:6]	Reserved. Default value 0
Bit [15:8]	Reserved, default value 1

Miscellaneous Configuration: Register 0x12h

Configuration	Description			
Bit [8:0]	Unilrn8~0 (for security mode)			
Bit [10:9]	Reserve			
Bit [11]	Reserve			
Bit [13:12]	Power Saving Select			
EDI, Bit [14]	Recommend LED variety			
		Lnkact	Speed	Dupcol (always single color)
	00	Single color	Single color	Duplex/col
	01	Single color	Single color	duplex
	10	Dual color	Dual color	Duplex/col
	11	Dual color	Dual color	duplex

VLAN mapping table register: 0x13h~0x22h

Configuration	Description
Bit [8:0]	VLAN mapping table.

Per Port Buffer Threshold: 0x23h~0x26h

Configuration	Description
Bit [13:8], Bit [5:0]	Port Buffer Threshold (available buffers are 8 times of the value)

Total Buffer Threshold: 0x27h

Configuration	Description
Bit [5:0]	Total Buffer Threshold for all ports
Bit 7	1: Enable EEPROM Threshold value, 0: default Threshold value

4. EEPROM Content Description

4.1 EEPROM Register Description:

Register 0x00h: Signature. Default value is 4154h. AT8985P will check register 0 value before read EEPROM content. If this value not match with 4154h then other values in EEPROM will be useless. AT8985P will use internal defaule value.

Register 0x01h~0x09h: Port 0~5 configuration register.

Bit 0: 802.3X Flow Control capability. 1: Enable; 0: Disable.

Bit 1: Auto Negotiation capability Enable. 1: Enable; 0: Disable.

Bit 2: Speed Capability when Bit 1 Enable. 1: 100; 0: 10.

Bit 3: Duplex Capability when Bit 1 Enable. 1: Full; 0: Half.

Bit 4: VLAN Tag Port. 1: set to Tag port; 0: set to Untag port.

Bit 5: Reserve.

Packet. Lower priority packets are Q0, Q1 & Q2.

Bit 6: TOS over VLAN Priority. Define AT8985P priprity source when VLAN & TOS existed in the packet. 1: TOS

priority level higher than VLAN; 0(default): VLAN priority level higher than TOS.

Bit 7: Enable Port Based Priority. 1: Enable; 0: Disable. If this bit turn on then AT8985P willnot check TOS or VLAN

as priority reference. AT8985P will check port base priority only.

Bit[9:8]: Port base priority number. From 0~3 mapping to Q0~Q3.

Bit[13~10]: Port Base VLAN ID when packet without 4 bytes VLAN tag. If packet with 4 bytes VLAN then AT8985P will not add this VLAN ID to packet content. ID is from 0-15.

Bit[14]: Select FX interface. 1: FX; 0: TP;

Bit[15]: Auto MDIX enable. 1: Enable; 0: Disable.

Register 0x0ah: Configuration Register

Bit[7~0]: Reserve

Bit 8: Reserve

Bit 9: Enable replace VLAN ID 0 & 1 by PVID. 1: Enable; 0: Disable. If this bit enable then AT8985P will check VLAN Id. If this VLAN ID is 0 or 1 then AT8985P will replace this ID by PVID.

Bit[15~10]: Reserved.

Register 0x0bh: Custom Register

Bit[4~0]: Reserve.

Bit 5: Reserve.

Bit 6: Enable IPG Leveling. 1/Enable. 0/Disable. When this bit is enable AT8985P will transmit packet out at 96 bit or 92 bit to clean buffer. If disable this function AT8985P will transmit packet at 96 bit.

Bit 7: Trunk port enable. 1/Enable, 0/Disable. If enable Trunk port function, these Trunk ports must at same VLAN. The Trunk port speed should run at 100M Full Duplex.

Bit[12~8]:Reserve.

Bit 13: Reserve.

Bit 14: Reserve.

Bit 15: Reserve.

Register 0x0ch: Reserve.

Register 0x0dh: Reserve.

Register 0x0eh: VLAN priority map

Value 00~11 are Q0~Q3 respectively.

Bit[1:0]: Mapped priority of VLAN tag value 0

Bit[3:2]: Mapped priority of VLAN tag value 1

Bit[5:4]: Mapped priority of VLAN tag value 2

Bit[7:6]: Mapped priority of VLAN tag value 3

Bit[9:8]: Mapped priority of VLAN tag value 4

Bit[11:10]: Mapped priority of VLAN tag value 5

Bit[13:12]: Mapped priority of VLAN tag value 6

Bit[15:14]: Mapped priority of VLAN tag value 7

Register 0x0fh: TOS priority map

Value 00~11 are Q0~Q3 respectively.

Bit[1:0]: Mapped priority of TOS value 0

Bit[3:2]: Mapped priority of TOS value 1

Bit[5:4]: Mapped priority of TOS value 2

Bit[7:6]: Mapped priority of TOS value 3

Bit[9:8]: Mapped priority of TOS value 4

Bit[11:10]: Mapped priority of TOS value 5

Bit[13:12]: Mapped priority of TOS value 6

Bit[15:14]: Mapped priority of TOS value 7

Register 0x10h: Miscellaneous Configuration Register.

Bit[1:0]: Broadcast Storming threshold. See Broadcast Threshold table.

Bit 2: Broadcast Storming Enable. 0/Disable. 1/Enable.

Bit 3: Reserve.

Bit 4: CRC check disable. 1/ Disable. 0/Enable.

Bit 5: Reserve.

Bit 6: Switch RXCLK to TXCLK at GPSI interface. 1/Enable. 0/Disable.

Bit 7: Aging Disable. 1/Disable. 0/Enable.

Bit[15:8]: Reserve.

Register 0x11h:

Bit 5: VLAN mode select, default is “0”. “0”, By-pass mode with port-base VLAN. “1”, VLAN ID base VLAN.

Bit [15:6] : Reserve value “1”,

Bit [4:0] : Reserve value “0”.

Register 0x12h: Miscellaneous Configuration Register

Bit [8:0]: Port Locking enable. Learn one MAC ID when enable. 1/Enable. 0/Disable.

Bit [10:9]: Reserve.

Bit 11: Reserve.

Bit [13:12]: Power Saving. 1/Enable. 0/Disable.

Bit[14]: LED selection. See EEPROM content.

Bit[15]: ENDC16 select excessive collision drop packet. 1/drop. 0/no drop.

Register 0x22h~0x13h: VLAN group 15~0 outbound port map. Default value 1ffh. Each register mapping to port

Bit0: Port0

Bit2: Port1

Bit4: Port2

Bit6: Port3

Bit7: Port4

Bit8: MII Port

Select the VLAN group ports is to set the corresponding bits to 1.

Register 0x26h~0x23h: Bit[5:0] Port 7~0 Buffer Threshold when register 0x27h bit 15=1. Normal value is 03h.

Register 0x27h:

Bit[5:0]: MII Port buffer Threshold.

Bit[12:8]: total buffer Threshold.

Bit 15: Threshold selection enable. 1: Enable; 0: Disable. When set at ”1”, AT8985P will set buffer threshold by the value of register0x26h~0x23h.

Packet with Priority:

Normal packet content

Ethernet Packet from Layer 2

Preamble/SFD	Destination (6 bytes)	Source (6 bytes)	Packet length (2 bytes)	Data (46-1500 bytes)	CRC (4 bytes)
	Byte 0~5	Byte 6~11	Byte 12~13	Byte 14~	

VLAN Packet

AT8985P will check packet byte 12 &13. If byte[12:13]=8100h then this packet is a VLAN packet

Tag Protocol TD 8100	Tag Control Informatipn TCI	LEN Length	Routing Information
Byte 12~13	Byte14~15	Byte 16~17	Byte 18

Byte 14~15: Tag Control Information TCI

Bit[15:13]: User Priority 7~0

Bit 12: Canonical Format Indicator (CFI)

Bit[11~0]: VLAN ID. The AT8985P will use bit[3:0] as VLAN group.

TOS IP Packet

AT8985P check byte 12 &13 if this value is 0800h then AT8985P knows this is a TOP priority packet.

Type 0800	IP Header
Byte 12~13	Byte 14~15

IP header define

Byte 14

Bit[7:0]: IP protocol version number & header length.

Byte 15: Service type

Bit[7~5]: IP Priority (Precedence) from 7~0

Bit 4: No Delay (D)

Bit 3: High Throughput

Bit 2: High Reliability (R)

Bit[1:0]: Reserve

4.2 EEPROM Access

Customer can select AT8985P read EEPROM contents as chip setting or not. AT8985P will check the signature of EEPROM to decide read content of EEPROM or not.

RESETL & EEPROM content relationship

RESETL	CS	SK	DI	DO
0	High Impedance	High Impedance	High Impedance	High Impedance
Rising edge 0→1 (30ms)	Output	Output	Output	Output
1 (after 30ms)	Input	Input	Input	Input

Keep at least 30ms after RESETL from 0→1. AT8985P will read data from EEPROM. After RESETL if CPU update EEPROM that AT8985P will update configuration registers too.

When CPU programming EEPROM & AT8985P, AT8985P recognizes the EEPROM WRITE instruction only. If there

is any Protection instruction before or after the EEPROM WRITE instruction, CPU needs to generate separated CS signal cycle for each Protection & WRITE instruction.

CPU can directly program AT8985P after 30ms of Reset signal rising edge with or without EEPROM

5. DC Characteristics

5.1 Absolute Maximum Rating

Symbol	Parameter	Rating	Units
V_{CC}	Power Supply	-0.3 to 3.63	V
Vcca2	TX line driver	-0.3 to 2.75	V
Vccpll	PLL voltage	-0.3 to 2.75	V
Vccik	Digital core voltage	-0.3 to 2.75	V
V_{IN}	Input Voltage	-0.3 to V_{CC} + 0.3	V
Vout	Output Voltage	-0.3 to Vcc + 0.3	V
TSTG	Storage Temperature	-55 to 155	°C
PD	Power Dissipation	3	W
ESD	ESD Rating	2KV	V

5.2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc	Power Supply	3.135	3.3	3.465	V
Vcca2	TX line driver		2.25		V
Vccpll	PLL voltage		2.25		V
Vccik	Digital core voltage		2.25		V
Vin	Input Voltage	0	-	Vcc	V
PC	Power consumption		2		W
Tj	Junction Operating Temperature	0	25	125	°C

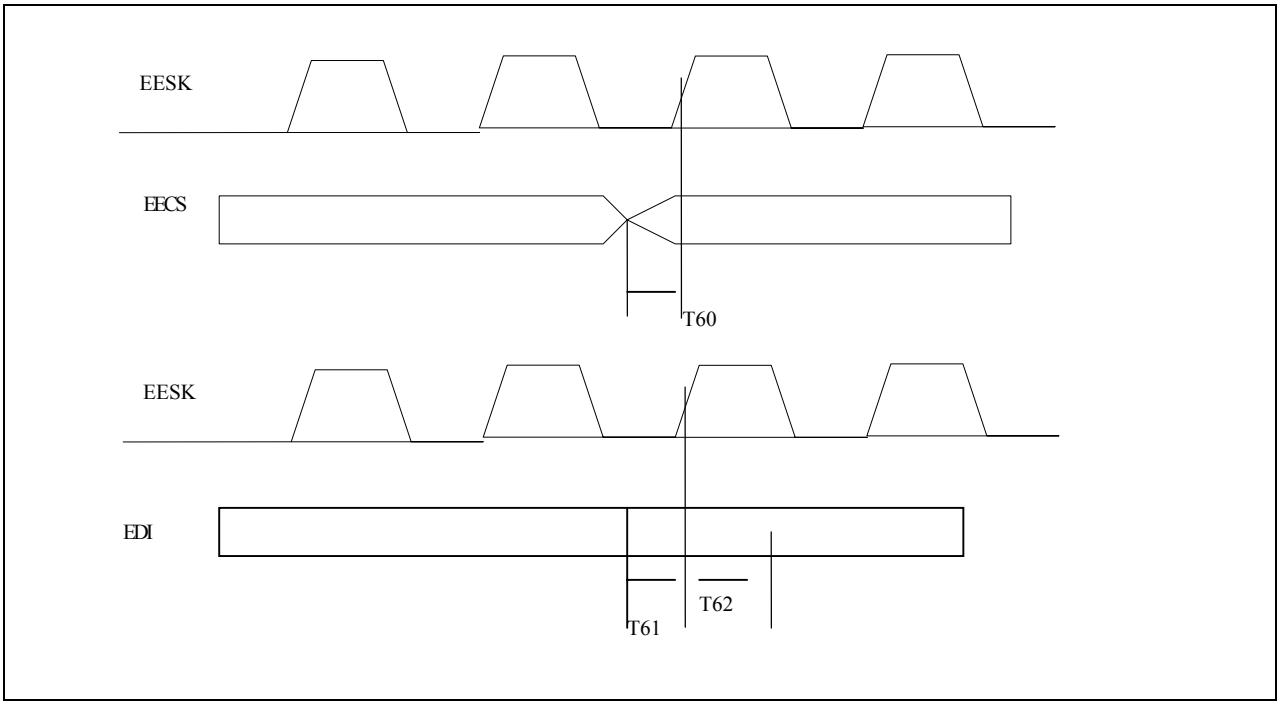
5.3 DC Electrical Characteristics for 3.3V Operation

Under Vcc=3.0V~3.6V, Tj= 0 °C ~ 115 °C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VIL	Input Low Voltage	CMOS			0.3 * Vcc	V
VIH	Input High Voltage	CMOS	0.7 * Vcc			V
VOL	Output Low Voltage	CMOS			0.4	V
VOH	Output High Voltage	CMOS	0.7 * Vcc			V
RI	Input Pull_up/down Resistance	VIL=0V or VIH = Vcc		100		KΩ

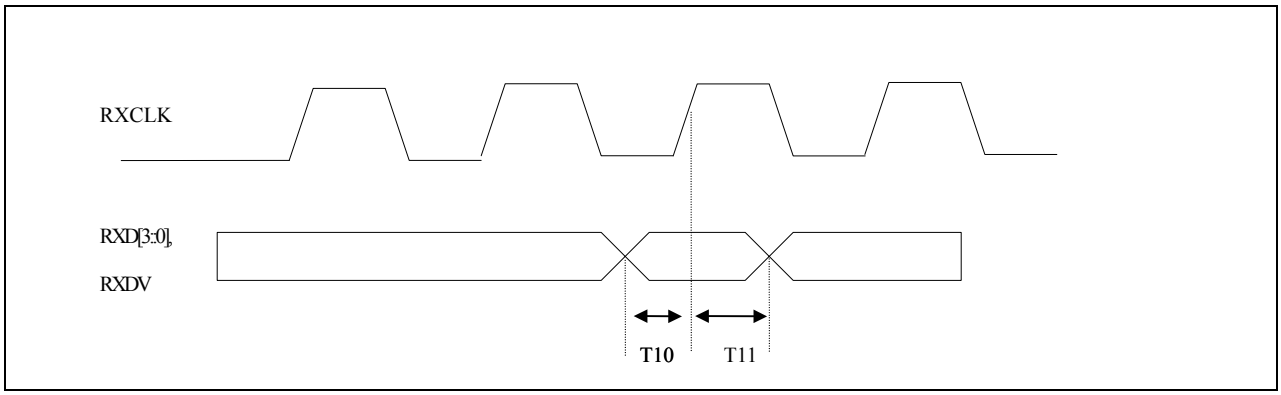
6. AC Characteristics

6.1 EECS, EESK and EDI Signals Timing



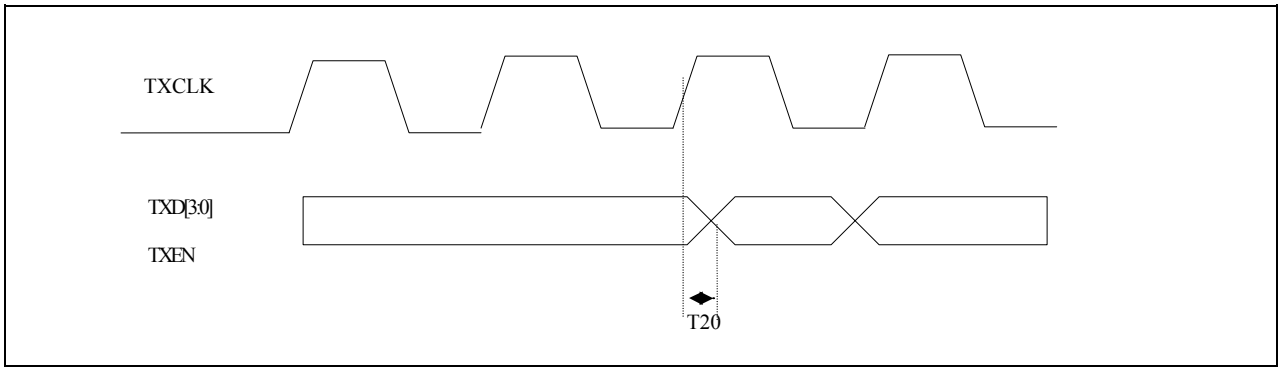
Name	Parameter	Min	Max	Units
T60	EECS to EESK setup time	10		ns
T61	EDI to EESK setup time	10		ns
T62	EDI to EESK hold time	10		ns

6.2 MII Receive Signals Timing



Name	Parameter	Min	Max	Units
T10	Setup Time to Rising RXCLK	4		ns
T11	Hold Time to Rising RXCLK	2		ns

6.3 MII Transmit Signals Timing



Name	Parameter	Min	Max	Units
T20	Data Valid Delay after Rising TXCLK	3	10	ns

7. Package

128 Pin PQFP Outside Dimension